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Analysis of trap states in AlGaN/GaN self-switching diodes via impedance measurements

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A B S T R A C T

The presence of trap states in self-switching diodes (SSD) based on an AlGaN/GaN heterojunction has been identified by means of their AC characterization between 75 kHz to 30 MHz in a wide temperature range, from 80 K to 300 K. Measurements allow us to determine two different characteristic energies of the traps, 12 meV and 61 meV, being associated to a distribution of surface states and one discrete bulk trap, respectively. The impact of the trapping effects on microwave detection at zero-bias has also been analyzed in the same temperature range, the measured responsivity showing an unusual enhancement and a low-frequency roll-off at low temperatures.

1. Introduction

In the last few years, devices based on the AlGaN/GaN heterostructure have received considerable attention thanks to their material properties, including wide bandgap, high electron mobility and high density of two-dimensional electron gas (2DEG), making them one of the best choices for high-power and high-frequency applications. However, the presence of several traps of different nature, either in the bulk or at the surface, hinder the performance of these devices, originating undesirable changes in their behavior and limiting their reliability [1]. Trapping effects in GaN devices are significant for two fundamental reasons. First, they can deplete the 2DEG by capturing electrons, resulting in a reduction of the current. Second, their slow nature causes frequency dispersion, thus limiting their dynamic performance. Recently, a wide variety of techniques have been used to investigate the behavior of trapping mechanisms [2–4], one of the most popular methods consisting of impedance measurements, allowing to find the activation energy (E_a) of charge traps. Both surface and bulk traps in transistors are usually modelled as an *RC* circuit, either in parallel or in series with the classic small-signal equivalent circuit, thus capturing the frequency dispersion of the output impedance of the devices. In order to determine the parameters of the traps, such AC characterization must be made in a wide range of temperatures, first, because the impact of trapping mechanisms increases when decreasing the temperature, and second, because one can observe the thermal activation of the charge release.

The objective of this work is to analyze the impact of traps on Self-Switching Diodes (SSDs), which are planar nanodiodes fabricated by the etching of two L-shaped insulating trenches (as sketched in Fig. 1) on a heterolayer, defining conductive asymmetric nanochannels [5]. By breaking the symmetry of a narrow channel (see Fig. 1) this device provides a nonlinear I-V curve (based on surface and electrostatic effects) without the use of any doping junction or barrier. Taking advantage of such non-linearity, SSDs fabricated with different technologies have already shown experimentally extraordinary capabilities for submillimeter-wave and THz detection. GaAs SSDs have demonstrated room temperature detection at 1.5 THz [6]. Even if GaN SSDs cannot compete in high-frequency performance with other high mobility semiconductors like InGaAs [7] or InAs [8], successful results have been obtained up to 690 GHz with GaN [9]. GaN based SSDs can also handle very high input RF power, so that their practical application as power detectors of ultra-high-power sub-mm wave sources seems feasible. Some niche applications could be nuclear magnetic resonance appliances or electronic countermeasure.

Moreover, in order to design continuous wave sub-mm wave emitters based on Gunn oscillations [10], SSDs can also be used instead of using "classical" vertical n^+nn^+ junctions. Remarkably, in GaN SSDs, the strategic combination of the SSD geometry with the presence of negative differential mobility, high electrical strength, high saturation velocity and low energy relaxation time, offers an optimal environment for the generation of very high frequency Gunn oscillations [11]. However, in spite of the efforts made in recent years [12,13], no clear

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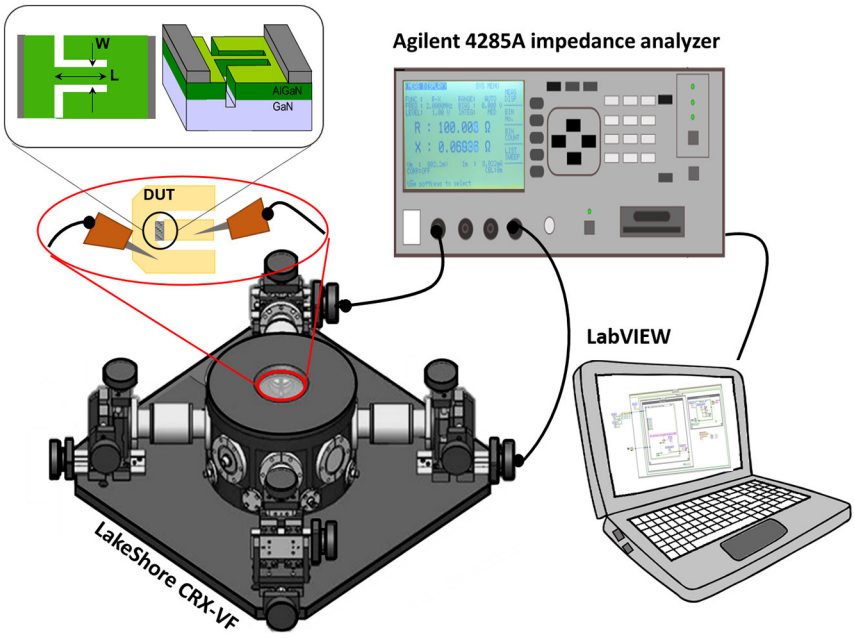

Fig. 1. Schematic diagram for the setup of trapping characterization. A cryogenic probe station connects the device to an Agilent 4285A LCR meter. All system is controlled by means of a LabView code to stabilize the temperature and record the impedance measurements.

experimental evidence of THz oscillations was found so far in GaN manufactured devices. In any case, the good performances of GaN SSDs as detectors of submillimeter-wave signals [14] combined with their planar geometry, which allows for a better free space coupling and a flexibility in the design (for an optimum thermal dissipation and reduction of parasitic effects), enables them to operate not only as detectors but also opens the possibility to develop a completely integrated emitter/detector submillimeter-wave working at room temperature and motivates our study of the behavior of traps in GaN SSDs. In fact the existence of traps in these devices has already been evidenced, being of special relevance those originated by the etching process at the sidewalls of the channel due to the high surface-to-volume ratio of the device [15]. On the other hand, lattice defects, like vacancies, dislocations, impurities, etc., create the well-known GaN-bulk traps, typically reported in high electron mobility transistors (HEMTs) [5,15].

In this work, by means of an impedance analysis in a wide temperature range, we identify and estimate the characteristic energy of surface and bulk traps present in the SSDs. In addition, since most trap effects can also be observed in DC and high-frequency characteristics, we will demonstrate their influence on the DC curves and the zero-bias microwave responsivity.

2. Experimental setup and device under test

The SSD under study was fabricated on an AlGaN/GaN heterostructure grown on a Si substrate. The epitaxial stack consists of a 25 nm $Al_{35}Ga_{65}N$ layer on a 1.5 μm GaN layer. The fabrication process is very similar to that presented in [14], where dry etching technology has been used to define the trenches. The device under test consists of a single channel, 1 μm long and 100 nm wide. On-wafer measurements were carried out using a cryogenic probe station (LakeShore CRX-VF) in a temperature range from 80 K to 300 K.

The experimental setup used for the AC characterization is displayed in Fig. 1. An Agilent 4285A precision LCR meter was connected through a DC/RF probe to the SSD to perform continuous variable temperature measurements without the need to re-land the needles once the temperature is settled, and the real and imaginary parts of the impedance were recorded using a LabVIEW code. Short/open calibration allows to compensate the residual impedance of the test fixture and cables. A sinusoidal signal of 30 V_{rms} in the frequency band between 75 kHz and 30 MHz was used in the impedance measurements. The *I-V* curves in the DC regime were measured by means of a B2900A Source Measure Unit (SMU).

Finally, the setup employed for the RF characterization consisted of a vector network analyzer (Agilent N52444A PNA-X) working as a RF power generator in the frequency range from 0.1 GHz to 40 GHz, together with a SMU in order to bias the SSD with zero-current and record the output voltage ΔV (voltage difference between RF signal on and off). The input frequency-dependent power losses were taken into account by adjusting the power output of the VNA so that a constant value of −5 dBm was injected as input power to the device, P_{in}. More details of the setup can be found in [16].

3. Results

As mentioned above, traps capture electrons from the 2DEG which deplete the channel, causing a decrease in the drain current, reflected in the DC measurements. The asymmetric shape of the SSD provides a non-linear *I-V* curve, which was measured over a temperature range from 80 K to 300 K, as shown in Fig. 2. Unexpectedly, when lowering the temperature, the resistance increases despite the higher mobility of electrons. The inset of Fig. 2 reveals a monotonous increase of resistance ($R = \partial V/\partial I$) when decreasing temperature (T). The current decrease is attributed to a smaller effective width of the channel at lower T originated by the increasing presence of trapped charge at the sidewalls of the trenches. After an in depth-analysis of several geometries at room temperature, it was found that the depletion region caused by the surface traps at each side of the channel is about 35 nm, what means that at lower temperature the channel could be nearly completely closed owing to an increased charge trapped at the sidewalls. Another remarkable fact is the change in the bowing of the *I-V* curve, from a concave shape ($\partial^2 I/\partial V^2 < 0$) at low T to a convex one ($\partial^2 I/\partial V^2 > 0$) for T above 250 K, as observed in the bowing coefficient ($\gamma = R{\cdot}\partial^2 I/\partial V^2$) represented in the inset of Fig. 2. The change of sign of γ indicates the transition from space-charge limited injection conditions (when the channel is closed at low T) to the typical ohmic/saturated current when the effective width of the channel increases for higher T. These two regimes are determined by the amount of charge trapped at

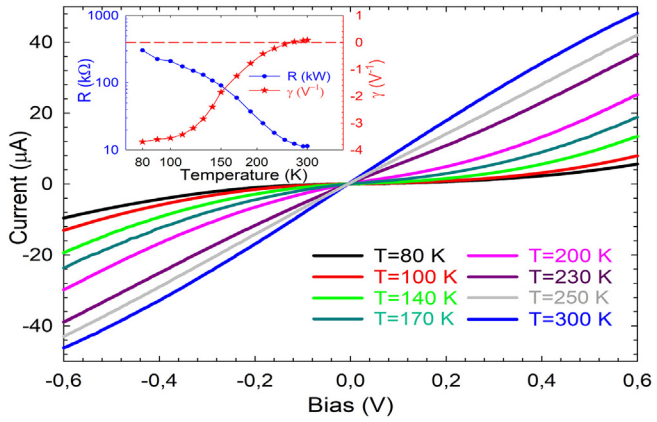

Fig. 2. *I-V* curves of the SSD under test at different temperatures. The inset shows the resistance (*R*) and the bowing coefficient (γ).

the surface states, so that a thermal trap activation process seems to be at the origin of the transition from one to the other.

Since traps produce dispersion effects on the electrical properties and are slow in nature [17], we have investigated the associated effects by measuring the low-frequency dispersion of the SSD output impedance, one of the most widely used techniques for analyzing traps [2–4,17]. Using the setup described in the previous section, we have obtained the real, Re[*Z*], and imaginary, Im[*Z*], parts of the impedance, *Z*, of the SSD between 75 kHz to 30 MHz. The results are reported in Fig. 3. For all temperatures, Re[*Z*] presents a constant value at low frequency followed by a roll-off, taking place at lower frequency as *T* decreases. The value of Re[*Z*] at low frequency is in good agreement with the one obtained from the *I-V* curves, represented by stars in Fig. 3. Apart from that, it is worth noting that the increase of the resistance for lower *T* observed in the DC characterization is confirmed with these AC measurements, which, jointly with the observed low-frequency dispersion, supports the interpretation given to the behavior of the *I-V* curves in terms of the presence of thermally activated traps. In addition, it seems that for the lower temperatures two separate characteristic times and frequency roll-offs are revealed, indicating the potential existence of two types of traps.

The presence of traps becomes even more visible in Im[*Z*], since a minimum (at f_{peak}), which shifts to higher frequency at increasing *T*, appears for $T < 200$ K at the same frequency as the roll-off in Re[*Z*]. This frequency behavior vanishes when increasing *T* above 200 K, again supporting the idea of a thermal activation of traps being at the origin of this dependence. To get more insight into the origin and

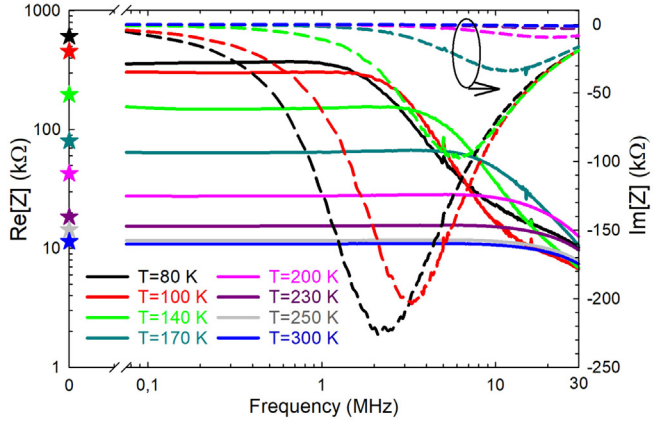

Fig. 3. Real, Re[*Z*], and imaginary, Im[*Z*], parts of the impedance vs. frequency (75 kHz-30 MHz) at different temperatures. The stars correspond to the resistance calculated from the DC curves ($f = 0$ Hz).

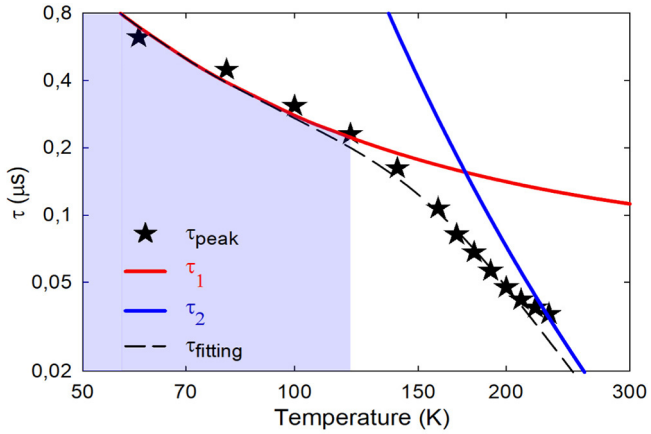

Fig. 4. Experimental values of τ_{peak} (stars), analytical fittings (solid lines) corresponding to surface (τ_1) and bulk (τ_2) traps, and global characteristic time (dashed line) calculated as $\tau_{fitting} = (\tau_1 \cdot \tau_2)/(\tau_1 + \tau_2)$. The shaded area indicates the temperature range where the behavior is dominated by surface traps.

characteristics of such energy states, we attribute the inverse of the peak frequency of Im[*Z*] to the characteristic time of the traps $\tau_{peak} = (f_{peak})^{-1}$. The extracted values of the characteristic time are plotted in Fig. 4 (stars) as a function of *T*. Surprisingly, two distinct slopes become clear in the figure, so that the coexistence of two kinds of traps with different origins and physical behavior appears to be the most reasonable explanation. At high temperatures the characteristic time exhibits a strong dependence on *T*, which softens for temperatures below 150 K. While at high *T* the temperature dependence of the characteristic time can be well explained by considering a trap with a discrete energy level, it is not the case for its slow variation with *T* for the low-temperature range. In the latter case, only the presence of a spread of relaxation times related with the existence of multiple traps with a wide energy distribution would allow to explain the soft temperature dependence of the characteristic times. This is a plausible explanation for the results in our SSDs, since the etching of the trenches would produce quite a lot of surface states at the sidewalls, with many different ionization energies distributed within the semiconductor GAP. The behavior of the characteristic times associated to such distribution of energies and relaxation times has already been observed in amorphous materials, related to the grain boundaries and the release of space charges [18,19]. In such materials, as in our devices, a negative temperature coefficient is observed (resistance grows as *T* is increased). When such an energy distribution of trap states appears, the capture and release of electrons occur from diverse levels instead of a discrete one and, as a result, a spread of relaxation times is expected, so that the temperature dependence of the effective characteristic time is much softer than for a single energy state. In addition to that, the release of charge trapped at the surface states due to their thermal activation enhances the opening of the channel, leading to the reduction of the low-frequency resistance of the devices.

We will therefore explain the global impedance relaxation mechanism, within the low-temperature range $T < 150$ K, which we attribute to intermediate surface states, through the Arrhenius relation typical from a spread or relaxation times characterized by a global activation energy E_{a1} [18].

$$\tau_1 = \tau_{01} \cdot e^{\left(\frac{E_{a1}}{k_B T}\right)}, \quad (1)$$

where τ_{01} is a pre-exponential factor independent of temperature and k_B is the Boltzmann constant.

Thus, the effective global energy of this energy-distributed kind of surface traps can be extracted from the values of τ_1 for the smallest temperatures. Fig. 5(a) shows the linear dependence of $\ln(\tau_1)$ with $1/k_B T$, providing a fitting slope of $E_{a1} = 12 \pm 2$ meV. The same

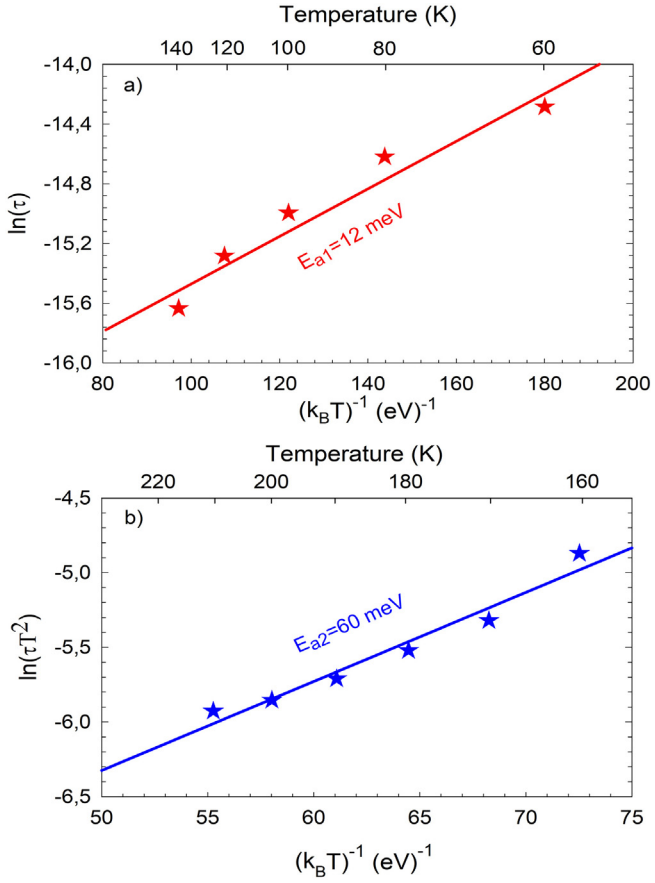

Fig. 5. (a) Arrhenius plot for τ_1, the characteristic time of the peak of Im[Z] at low temperatures. (b) Modified Arrhenius plot for τ_2, computed from $1/\tau_{peak} = 1/\tau_1 + 1/\tau_2$ at the higher temperatures. The solid lines are the obtained fittings.

extraction procedure has been accomplished in SSDs fabricated in the same technological process batch with different channel widths and the energies obtained are similar (always around 15 ± 3 meV).

Once the surface trap signature is determined, it is straightforward to estimate the values of τ_1 over the full temperature range, represented by the red line in Fig. 4. As expected, the surface traps stop being dominant for temperatures above 150 K, but they are still influential. Remarkably, 140 K is the temperature obtained if we associate E_{a1} with k_BT.

The interpretation of the slope change observed in Fig. 4 for $T > 150$ K makes necessary the consideration of a different kind of trap, whose influence becomes visible in the results at the higher temperatures. Going further, the characteristic time of the second trap at each temperature, τ_2, can be estimated just using the times calculated from the previous fitting of τ_1 and the values obtained for τ_{peak} from the experimental data, since they should fulfil the relation

$$\frac{1}{\tau_{peak}} = \frac{1}{\tau_1} + \frac{1}{\tau_2}. \quad (2)$$

In this case, the behavior of τ_2 is consistent with that shown by bulk traps associated with a discrete energy level, one of the most common types of traps found in devices based on the AlGaN/GaN heterostructure [2–4,20]. Traps located in the bulk of GaN are often generated by physical defects in the lattice such as vacancies, dislocations, impurities, etc. Bulk traps have been identified in AlGaN/GaN devices using various techniques, such as low frequency S-parameter measurements in HEMTs [2–4], quantitative mobility spectrum analysis on AlGaN/GaN heterostructures [20], current relaxation analysis in HEMTs [20], etc. Unlike the previously observed surface traps, a bulk trap is characterized by a discrete energy level (E_{a2}) and a cross section (σ_{a2}), which can be determined using the modified Arrhenius equation

$$\tau_2 T^2 = k_{02} \cdot e^{\left(\frac{E_{a2}}{k_B T}\right)}, \quad (3)$$

with k_{02} a pre-exponential factor independent of temperature, from which the cross section can be estimated. An activation energy $E_{a2} = 60 \pm 6$ meV is extracted from the linear fitting of the values of ln ($\tau_2 T^2$) vs. $1/k_BT$ following Eq. (3), plotted in Fig. 5(b). Similar values for E_{a2} have been extracted in SSDs with different channel widths (with quite a small dispersion, always in the range 60 ± 6 meV), also in coincidence with the values found by several authors in GaN HEMTs [2,20–22], thus supporting our assumptions. Just as τ_1, the characteristic time of bulk traps τ_2 has been calculated for the whole temperature range using the coefficients obtained from the previous fitting and it is plotted with a blue line in Fig. 4. Subsequently, in order to verify the accuracy of our analysis, τ_{peak} was calculated at each temperature by means of Eq. (2) and the τ_1 and τ_2 values extracted from the fittings, illustrated by a dashed black line in Fig. 4. A fairly good agreement is found for the whole temperature range.

As explained before, the spread of relaxation times related to surface traps and the discrete bulk trap energies have been observed in SSDs with different channel lengths and widths, all of them showing similar temperature dependencies and characteristic energies, thus supporting our findings. However we have found some results which can be related to geometric effects. Even if all devices, regardless of their geometry, exhibit a bulk trap with an energy of around 60 meV, its influence is more remarkable in the wider SSDs, as expected due to their smaller surface-to-volume ratio, which conceals the role of surface traps.

Finally, the influence of the traps on the microwave detection capability of our SSD is investigated using the last setup described in Section 2. The responsivity was calculated as

$$\beta_{50\Omega} = \frac{\Delta V}{P_{in}}. \quad (4)$$

The impact of the traps on detection becomes clearly visible in Fig. 6. At low frequency, an enhancement of $\beta_{50\Omega}$ together with a change of sign is found as temperature is lowered from 300 K, reaching values of 100 V/W. This effect is consistent with the change of sign and increasing absolute value of the bowing coefficient γ observed in the inset of Fig. 3 (in a low frequency approximation for a strongly mismatched detector, as it is our case, $\beta_{50\Omega}$ goes as $-2Z_0\gamma$, with $Z_0 = 50\ \Omega$).

The frequency roll-off of the responsivity observed in Fig. 6 appears at much higher frequencies than those used in the impedance characterization. Indeed, for narrower devices the cut-off frequency is even higher (around 2 GHz for an 80-nm-wide SSD). Therefore, it is difficult to link both results. However, we know that both of them are originated

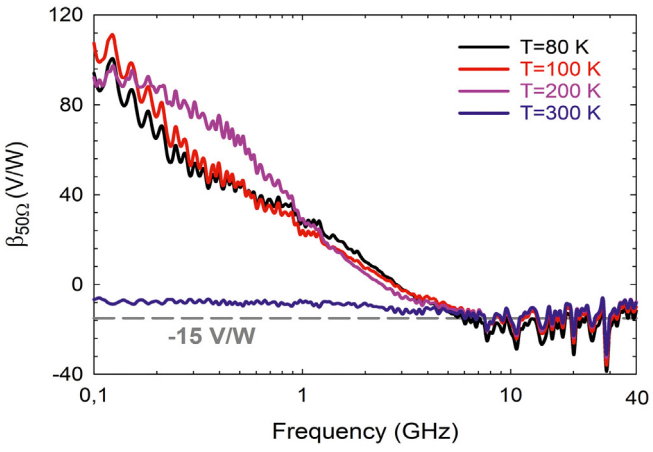

Fig. 6. Responsivity, $\beta_{50\Omega}$, at zero-bias as a function of frequency.

by the charge trapping/release at the sidewalls surface states, since they are subjected to the same thermal dependence (the frequency roll-off only appears when surface traps are active). On the other hand, transit-time or RC related cut-off mechanisms can be straightforwardly excluded, since they appear at much higher frequencies, as demonstrated by the measurements made in similar devices shown in [14]. We therefore attribute the roll-off of the responsivity at low temperature to the out-of-equilibrium trapping time of electrons at the surface states, which, being induced by the RF excitation, is much faster than the thermally activated charge release at low temperatures. As a consequence, an excess of surface charge is generated, which is at the origin of the increase of the low-frequency responsivity (and the sign inversion of the bowing coefficient). Indeed, for 300 K, contrarily to the positive values obtained at low frequency for lower T, $\beta_{50\Omega}$ is negative ($-9\ V/W$) as a result of the concave shape of the I-V curve (see inset of Fig. 2).

On the other hand, the release times decrease exponentially with temperature, thus compensating the trapping stimulated by the RF signal as temperature increases, so that the excitation-induced excess of surface charge is much lower and the responsivity is almost flat for $T > 200$ K. We have to remark that this explanation is consistent with the fact that for high frequencies, from 5 GHz onwards, when traps are not anymore responding to the excitation, the responsivity at all the temperatures shows an identical plateau of -15 V/W.

4. Conclusions

In this work, two kind of traps, whose existence was predicted by the DC characterization, have been identified in GaN based nanodiodes by means of AC impedance measurements. The first effect is associated with surface states at the sidewalls of the channel. These traps are responsible for the high resistance at low frequency, which is especially relevant at low temperatures. The dependence of the characteristic time of these traps with T reveals the classic behavior of a relaxation process resulting from a spread of times (associated with a wide distribution of energy states within the gap), with an effective activation energy of 12 meV. The second trap, whose characteristic energy is 60 meV, corresponds to a discrete energy state associated to a GaN bulk trap and matches perfectly with values provided by other authors. The dependence of the RF responsivity on temperature evidences the influence of such traps. The charges captured at the surfaces lead to an enhanced detection below 200 K, but only for frequencies lower than 5 GHz.

CRediT authorship contribution statement

E. Pérez-Martín: Conceptualization, Resources, Writing - original draft, Writing - review & editing. **D. Vaquero**: Resources. **V.J. Raposo**: Resources. **T. González**: Conceptualization, Writing - original draft, Writing - review & editing. **J. Mateos**: Conceptualization, Writing - original draft, Writing - review & editing. **I. Iñiguez-de-la-Torre**: Conceptualization, Resources, Writing - original draft, Writing - review & editing.

All the authors, E. Pérez-Martín, D. Vaquero, H. Sánchez-Martín, C. Gaquière, V. J. Raposo, T. González, J. Mateos and I. Íñiguez-de-la-Torre, have contributed equally to this work.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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