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Monte Carlo analysis of the influence of surface charges on GaN asymmetric nanochannels: Bias and temperature dependence

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ABSTRACT

In this paper, the occupancy of sidewall surface states having a clear signature in the performance of AlGaN/GaN-based self-switching diodes (SSDs) is analyzed using a semi-classical Monte Carlo (MC) simulator in a wide temperature (T) range, from 100 to 300 K. Experimental I–V curves show an unusual current decrease at low temperature attributed to surface trapping. The dependence on T of the negative surface charge density σ at the etched sidewalls of the SSDs is essential to explain the measurements. Two devices with different widths (80 and 150 nm) have been characterized and simulated in detail paying especial attention to the modeling of the surface states. At room temperature, MC simulations with a position-independent value of σ are able to qualitatively reproduce the I–V curves. However, a more complex approach is required to correctly replicate the values and shape of the DC experimental curves at low temperature, below 220 K. An algorithm where σ depends not only on T but also on the applied bias V is proposed to successfully fit the current values at every bias point. The model is able to explain the physics of the unexpected dependence of the resistance with the channel width and the sign change in the bowing coefficient, the parameters that govern the detection capabilities of the diodes.

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I. INTRODUCTION

The development of semiconductor devices operating in the terahertz (THz) region of the electromagnetic spectrum has attracted increasing attention in recent years in order to exploit its potential applications in fields like medicine, biology, astronomy, communications, security, etc.[1] Some of the efforts of the electronic industry to produce THz compact sources and detectors operating at room temperature are focused on using III-V high mobility materials along with downscaling devices to nanometer dimensions, thus leading to an increase in the operational speed of devices based on conventional architectures [such as THz high-electron mobility transistor (HEMTs)[2]] but also giving birth to new operational paradigms such as ballistic devices.[3,4] However, among other issues, such small dimensions typically involve a high surface-to-volume ratio, causing changes in the macroscopic electrical properties of the devices directly linked to phenomena taking place at the surfaces.[5,6] The fabrication technique, for example, the etching process, may create energy states inside the gap at the sidewalls of etched regions, which, by trapping electrons, partially deplete the conductive channel of the devices, resulting in a reduction of current.

Among III-V materials, the use of devices based on AlGaN/GaN has grown significantly, mainly due to the high carrier concentration achieved in two-dimensional electron gas (2DEG), larger than in other material systems.[7] Additionally, material properties of GaN, such as wide bandgap, relatively high electron mobility, large peak electron velocity, and high thermal conductivity and breakdown electric field[8] make it quite appropriate for the development of high-power and high-frequency devices, and, in particular, RF detectors. Indeed, several GaN-based devices have exhibited a high responsivity at moderate frequencies, like the well-known high-electron mobility transistors (HEMTs),[9] gated nanowire field-effect rectifiers (NW-FERs)[10] or self-switching diodes (SSDs),[11] and gated-SSDs (G-SSDs).[12]

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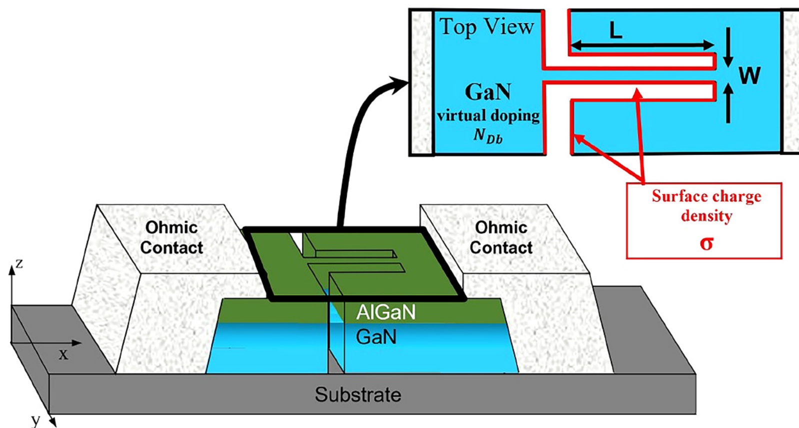

FIG. 1. Sketch of the SSD geometry and 2D "top-view" simulation domain.

In this work, we deal with SSDs fabricated on an AlGaN/GaN heterojunction grown on a Si substrate. SSDs are asymmetric planar nanodiodes with a conductive channel defined by the etching of two L-shaped trenches[13] (see Fig. 1). This asymmetric geometry can produce a rectifying behavior since the lateral field effect created by the negative (positive) applied voltage is able to open (close) the channel. The etching process used to define the channel creates numerous intermediate states at the semiconductor–air interfaces, so these devices are strongly affected by charges at the channel sidewalls. Nevertheless, their planar geometry and design flexibility make them potential candidates able to operate at THz frequencies. In fact, their capability for THz detection has been proved for different materials, like GaAs, InAs, and InGaAs.[14–16] Regarding GaN-based SSDs, in spite of the moderately high mobility of the material, sub-THz detection up to 320 GHz under probes[17] and 0.69 THz in a free-space configuration have been demonstrated.[18]

Apart from the experimental observations, electrical models, either based on analytical expressions (FET-like models)[19,20] or on numerical approaches [like Monte Carlo (MC) techniques],[21] are essential to understand how the geometry, material properties, or temperature affect the key figures of merit of the SSD as a detector. For example, in Ref. 22, a systematic study of the role of the flanges shape and size of InGaAs-2DEG based SSDs is reported. Concerning GaN SSDs, while some articles have theoretically explored their suitability to be used as Gunn emitters,[23,24] much less attention has been paid to the modeling of their operation as detectors, strongly affected by surface effects at low temperature. The presence of surface states in GaN SSDs is evidenced not only by an increase of the device resistance at low temperature but also by the presence of the typical features associated with traps found in the frequency dependence of their impedance,[25] whose measurement has allowed to determine the characteristic times and energies of such surface states. To get a deeper insight into the role played by such surface states, the aim of this work is to exploit the capabilities of Monte Carlo (MC) tools in order to interpret the temperature evolution of the I–V curves (and the associated detector parameters: resistance and bowing coefficient) of GaN SSDs of different channel widths in the 100-300 K range in terms of the charge trapped at the channel sidewalls. The suitability of the MC tool at explaining the physics of the DC and AC operations of SSDs including surface charges has been already proved in other works by our group.[21,24]

The paper is organized as follows. In Sec. II, the heterostructure of the devices under test, the experimental setup, and the main features of the numerical model used in the simulations are described. Section III presents the experimental DC curves that motivate the work, followed by MC simulations with a simple standard constant charge model (CCM). The comparison with experimental results shows the need for an improved model where surface charge depends on both the temperature and the applied bias. Microscopic quantities provided by MC simulations allow us to interpret and explain the observed dependencies of the resistance and bowing coefficient with the temperature. Finally, in Sec. IV, the main conclusions of this work are drawn.

II. DEVICE AND SURFACE CHARGE MODELS

The SSDs under test were fabricated using an heterojunction grown by EpiGaN on a high resistivity Si substrate. The epitaxial layer consists of a 575 μm thick Si substrate, 1.5 μm of GaN buffer followed by a 25 nm $Al_{0.35}Ga_{0.65}N$ barrier, and 3 nm of SiN as the passivation layer. Dry etching technology was used to define the two L-shaped insulating trenches as shown in Fig. 1. More technical details about the fabrication process can be found in Ref. 17. In this work, two SSDs with the same length (1 μm) but different widths W (80 and 150 nm) have been characterized. On-wafer measurements in a temperature range from 100 to 300 K were performed using a cryogenic probe station (LakeShore CRX-VF). The I–V curves were measured by means of a Keysight B2900A semiconductor analyzer connected to the device through continuously variable temperature probes allowing temperature sweeps without the need to lift and re-land the needles, thus minimizing the damage of the pads and allowing us to fully automatize the temperature control and measurements via an in-house LabView code.

Even if 3D simulations would be required to model the real geometry of the devices, here we make use of a 2D MC code. Previous studies of the impact of the extra inclusion of the 3D

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electric field[26] and the comparison between 2D and 3D MC simulations of ballistic junctions[27] indicate that the 2D approach is suitable to satisfactorily describe the operation of the SSDs, as we have already demonstrated in several types of nano-devices.[28–30] In our simulation, 3D spatial effects associated with the AlGaN/GaN heterojunction are ignored when solving Poisson's equation, and a zero electric field is applied in the non-simulated dimension. Nevertheless, to take into account the epilayer characteristics, a net background doping ($N_{Db} = 10^{17}\ \mathrm{cm}^{-3}$), representing the influence of the fixed charges of the real structure (negative charge at the top interface and positive piezoelectric charge at the heterojunction), is assigned to the GaN channel to solve Poisson's equation while impurity scattering is switched off (see Ref. 21 and references therein). The value of N_{Db} is kept constant for all the temperatures, since Hall effect measurements have confirmed a practically constant sheet electron concentration in the epilayer.

Furthermore, the transport model considers degeneracy, electron heating and contact injection with the appropriate statistics.[31] A semi-classical MC model is used; no effect of the 2DEG confinement on the scattering rates is included in our simulator. This may lead to some deviation in the value of the electron mobility at low temperatures, which can likely be disregarded if compared to other sources of mismatch between theory and experiments, such as geometrical and technological variability, epilayer dislocations, parasitic resistances,

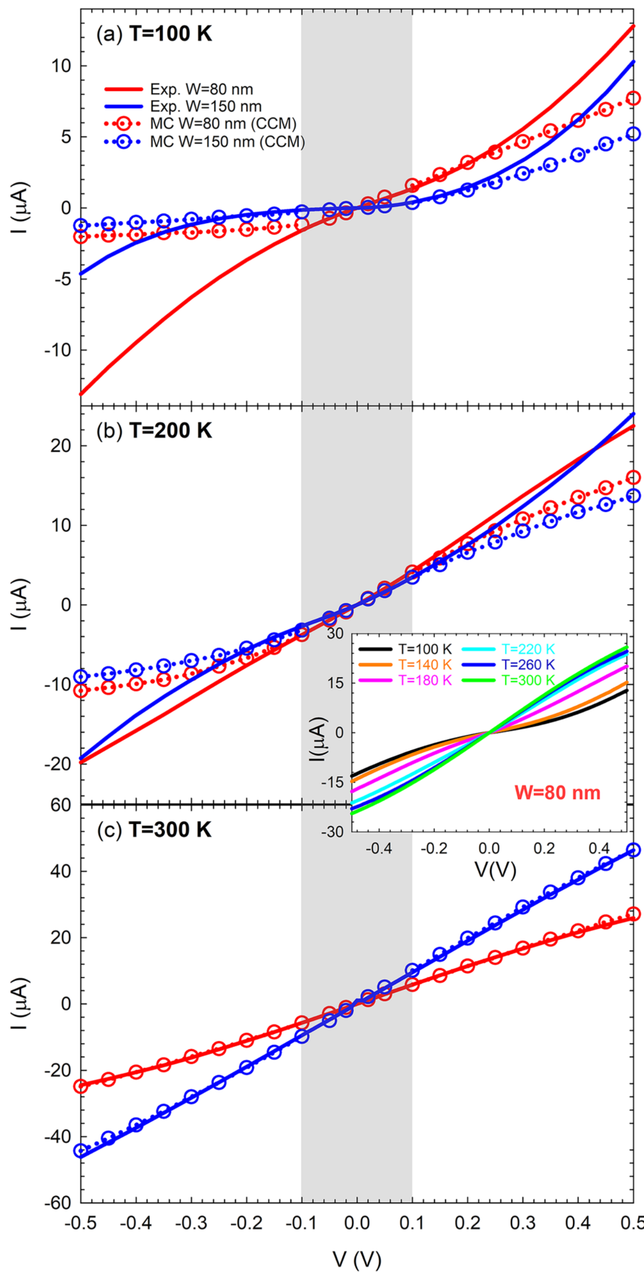

FIG. 2. Comparison of the experimental (solid lines) and MC simulated I–V curves (empty circles) for SSDs with two widths, $W = 80$ nm (red color) and $W = 150$ nm (blue color), at three temperatures: (a) 100, (b) 200, and (c) 300 K. The inset shows the temperature evolution of the I–V curves for the SSD with 80 nm width.

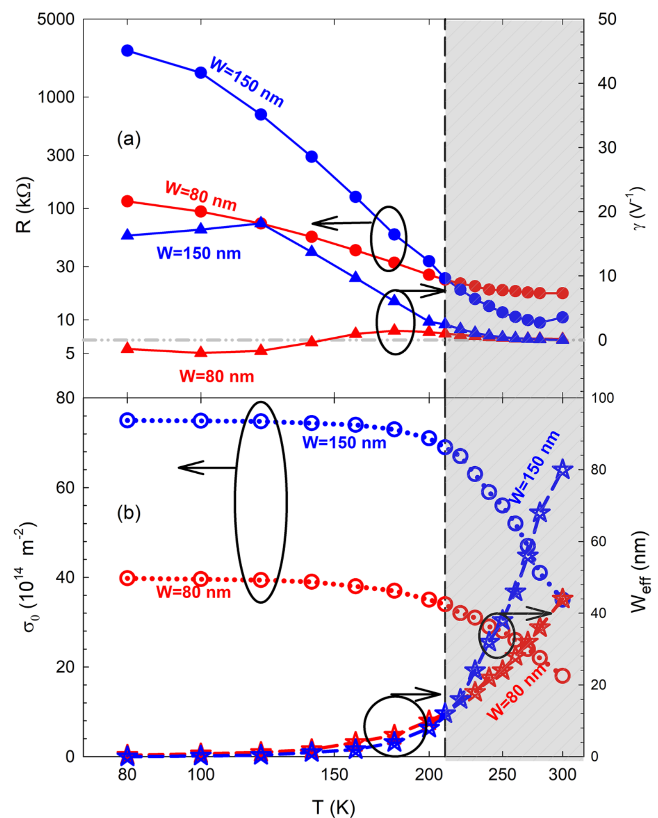

FIG. 3. (a) Resistance R and bowing coefficient γ extracted from the DC curves in the ± 0.1 V range. (b) Surface charge density σ_0 obtained with MC simulations as a function of T and associated effective width (W_{eff}). The red symbols represent the values for the 80 nm wide channel, while the blue ones correspond to the 150 nm wide channel.

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etc. A more detailed consideration of the 2DEG transport physics would probably lead to an offset in the values of the surface charges obtained at low T with no relevant change in the main conclusions of our work, while leading to a significant increase in the complexity of the models and a need for much more computing resources.

To account for surface charges, we use the model known as the constant charge model (CCM), which assigns a negative surface charge density σ independent of the position at the etched interfaces. Initially, a bias-independent σ will be considered at each temperature T. In a second step, the value of σ for each bias V and temperature T, $\sigma(V, T)$, will be determined from the fitting of the measured I–V curves. The ideal depletion region at each side of the channel induced by σ can be computed at equilibrium as $W_d = \sigma/N_{Db}$. Thus, the value of the effective (conducting) channel width is $W_{eff} = W - 2W_d$, with being W the actual width of the SSD. The electron dynamics has been simulated during a time series of 100 000 steps of 1 fs for each bias point.

III. EXPERIMENTAL MEASUREMENTS AND SIMULATIONS

Previous works[21,22] documented that the asymmetric shape of the channel of SSDs is the responsible for its non-linear I–V curve, being its shape and the ideal square-law detection severely affected by the presence of charges at the sidewalls' surface states originated during the etching process.[11] To evidence such an effect in the DC regime, the measurements of the I–V curves (in the low bias range ± 0.5 V) for the two channel widths, $W = 80$ and 150 nm, are shown in Fig. 2 for (a) 100, (b) 200, and (c) 300 K. We restrict the measurement range to low voltages since the objective is to test the performance of these devices as zero-bias detectors. Contrary to expectations, both devices exhibit a current decrease when lowering T (more clear to see in the inset of Fig. 2), despite the higher mobility. We attribute it to a significant increase of the surface charge density at low temperature. The capture of 2DEG electrons by surface traps partially depletes the channel, thus reducing the effective width and the current level. Another remarkable feature is found by comparing both device widths, since an opposite behavior to what expected is obtained for 100 K: the wider the channel, the lower the current. Indeed, the differential resistance, $R = \frac{\partial V}{\partial I}$, estimated from the I–V curves in the ± 0.1 V range, shown in Fig. 3(a), evidences a crossover from the expected behavior at room temperature, lower R for the wider channel, to the opposite result below 220 K. This behavior has also been observed in devices with other geometries (lengths of 1 and 2 μm, widths from 80 to 150 nm, with rectangular and tapered channels) and different number of parallel channels (1, 4, 8, and 16), with quite a small dispersion in the I–V curves.

To provide a physical explanation to these experimental outcomes, we have tried to reproduce these measurements, in the same voltage and temperature ranges, with MC simulations employing the CCM, shown by circles in Fig. 2. The diodes have been simulated using a single value of σ for each temperature, selected in order to fit the curves around equilibrium (± 0.1 V see the gray region in Fig. 2), so we call it σ_0. As observed, the CCM model with σ_0 is not able to reproduce the SSD behavior over the whole ± 0.5 V, mainly for low temperatures. Figure 3(b) shows the value of σ_0 as a function of T, exhibiting for both devices a monotonous increase when lowering T and becoming almost constant

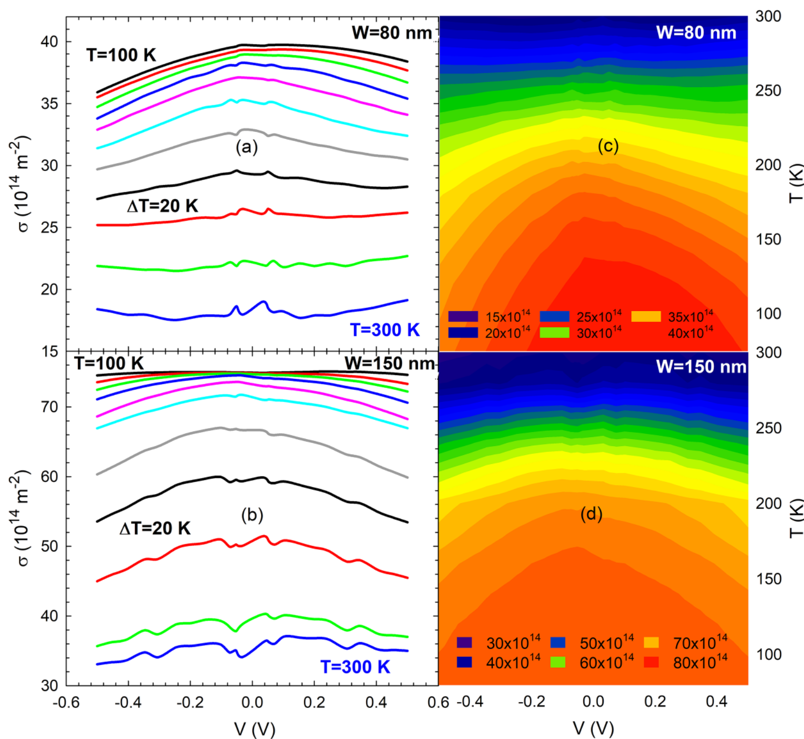

FIG. 4. Surface charge as a function of the applied bias for temperatures from 100 to 300 K in steps of 20 K, for both devices (a) $W = 80$ and (b) $W = 150$ nm. (c) and (d) show the same results in color maps.

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below 220 K. However, the increase is much sharper for the widest channel, since the narrower one does not allow to fill up the surface states when it is closed as much as the wide channels do.

For T above 220 K, a fairly good agreement between experimental and MC curves is achieved in the whole bias range [Fig. 2(c)]. In particular, values of $\sigma_0/q = 18 \times 10^{14}$ and $35 \times 10^{14}\,\mathrm{m}^{-2}$ for widths of 80 and 150 nm, respectively, are used at room temperature, thus originating depletion widths W_d of 18 and 35 nm (similar to those determined from electrical measurements of SSDs with different channel widths).[25,32] The disagreement between MC simulations and experiments at low temperature suggests that the surface charge density is not constant with the bias, so that it is necessary to use a bias-dependent value of σ in the MC simulations in order to replicate the shape of the I–V curve in the whole bias range, as we will show later.

The dependence of W_{eff} with T (extracted from the values of σ_0), shown in Fig. 3(b), can be used to explain the performance of the diodes: the higher W_{eff}, the lower R. Nevertheless, for T below 220 K, both diodes are almost completely pinched off ($W_{eff} \approx 0$), thus exhibiting very high resistances. Apart from the impedance, another remarkable figure of merit, playing a key role in microwave detectors, is the so-called bowing coefficient ($\gamma = R\frac{\partial^2 I}{\partial V^2}$).[33] The value of γ presents a much more complex pattern and shows completely different behavior for the two devices, as observed in Fig. 3(a), where the values of γ extracted from the experiments (also in the ± 0.1 V range) are plotted. At high temperatures, γ exhibit small positive values for both SSDs and increase with decreasing T. Unlike in the wider SSD, where γ is always positive, in the narrower one, γ undergoes a sign change as a consequence of the changeover of its I–V curve from a convex shape for high T (for which $\gamma > 0$), to a concave one for low T ($\gamma < 0$), see the inset in Fig. 2.

As explained before, for T below 220 K, the CCM model with just σ_0 is not able to reproduce the shape of I–V curves nor to explain the physics of the different behaviors exhibited by γ. Therefore, a more sophisticated algorithm, using a bias-dependent surface charge density $\sigma(V, T)$ globally accounting for the effects of the surface charge trapping and release mechanisms, is required. The value of $\sigma(V, T)$ is obtained for each T through the direct comparison between the experimental I–V curves with a series of MC simulations performed with different values of σ_0. The so obtained MC I–V curves match exactly the measurement in the whole bias range, so they are omitted in Fig. 2 for clarity. The interesting quantity is the so estimated $\sigma(V, T)$, whose values are plotted in Figs. 4(a) and 4(b), where the dependence of σ on the applied bias is clearly visible (mainly at low T). For both SSDs, $\sigma(V, T)$ presents a maximum around zero-bias, less pronounced

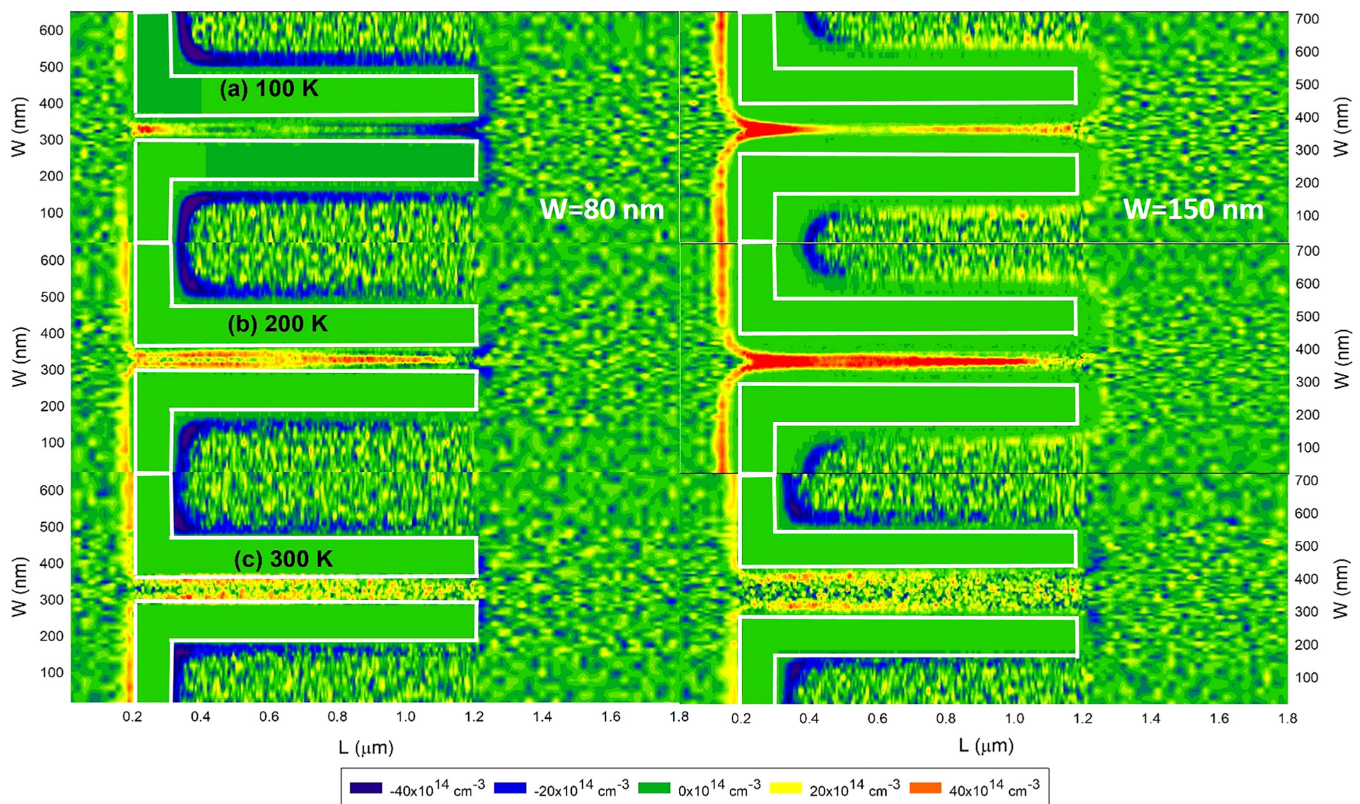

FIG. 5. Color maps of carrier concentration difference (Δn) between ± 0.1 V bias voltages for each SSD at three different temperatures: (a) 100, (b) 200, and (c) 300 K.

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when increasing T, and practically disappearing for T above 220 K. To better illustrate the evolution of $\sigma(V, T)$, color maps are displayed in Figs. 4(c) and 4(d).

The differences observed in the bias dependence of σ between both diodes allow explaining the presence or absence of the sign change in the bowing coefficient γ. In the 80 nm wide SSD, $\sigma(V, T)$ shows a higher asymmetry. At T above 220 K, $\sigma(V, T)$ takes nearly bias-independent values in both devices, very similar to those of σ_0 reported in Fig. 3(b), so that the non-linearity of their I–V curves is the one originated by the lateral field effect expected to take place in SSDs, thus providing higher currents for positive bias and leading to positive (and small) values of γ.

On the other hand, at low T (<150 K), we observe a strong bias dependence of σ on V, but with important differences when both SSDs are compared. For the 80 nm wide SSD, σ takes lower values for negative applied voltages, thus leading to a higher current in reverse bias, resulting in a negative bowing coefficient. By contrast, in the 150 nm wide SSD, $\sigma(V, T)$, besides taking significantly higher values, is more balanced, being moderately smaller for forward bias, resulting in a positive bowing coefficient (the same as in room temperature conditions). The physical mechanism at the origin of the dependence of σ on V is the modulation of the surface charge trapping/release rates by means of the electric field at the sidewalls of the channel. It increases under reverse bias

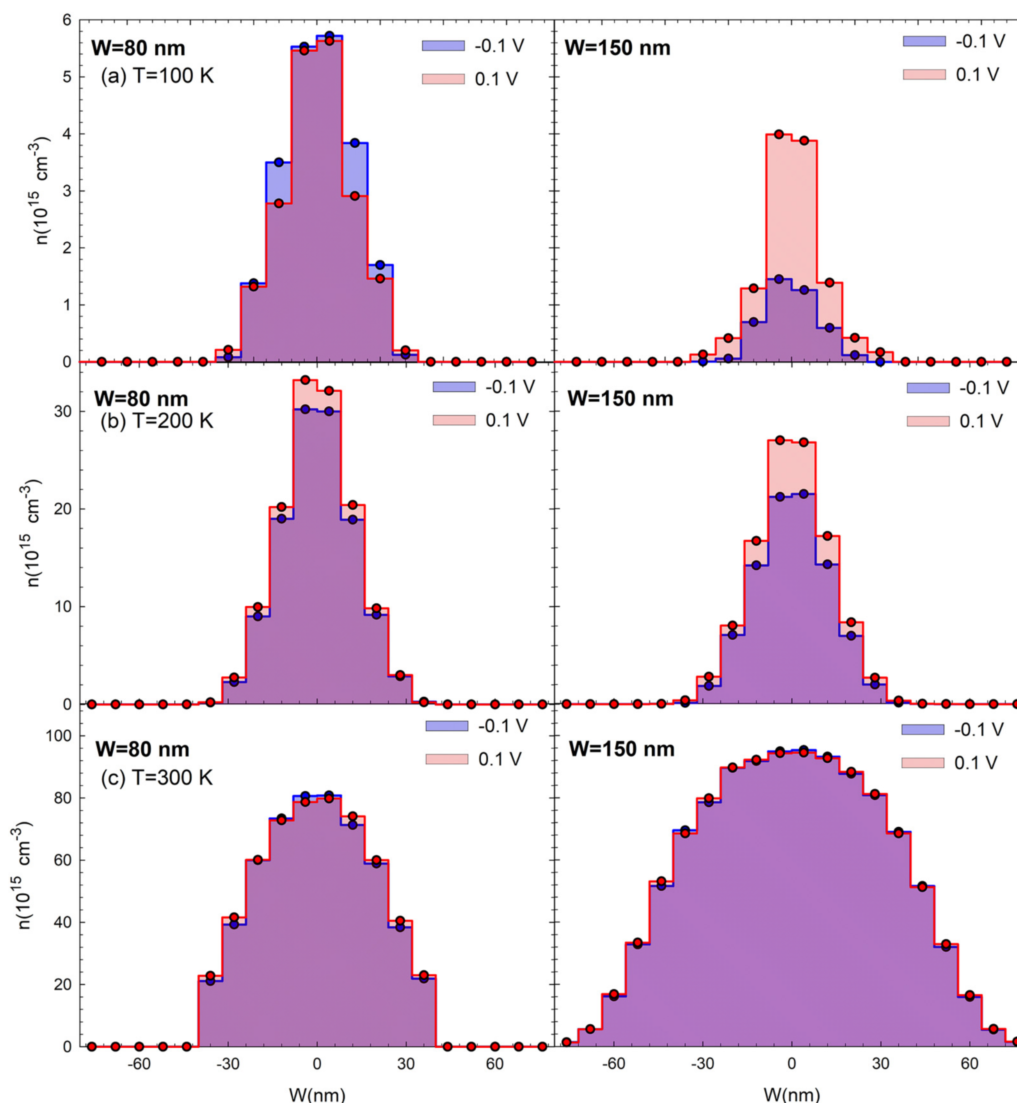

FIG. 6. Vertical profile of carrier concentration along the middle of the channel for two different bias voltages ($V = 0.1$ and $V = -0.1$ V) and for three different temperatures: (a) 100, (b) 200, and (c) 300 K.

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conditions, being able to increase the tunneling probability and the surface charge release rate for the case of the narrow channels.

The previous analysis of the dependencies of $\sigma(V, T)$ can provide an interpretation of the bowing coefficient sign in each device, but it is not enough to explain why γ is much higher for the wider SSD. To physically explain the origin of the differences, we have focused our attention on microscopic quantities provided by the MC simulations directly linked with the resistance and bowing coefficient. In particular, Fig. 5 shows, for three values of T, a color map of the carrier concentration difference (Δn) between two applied voltages, $+0.1$ and -0.1 V, using the respective values of $\sigma(V, T)$. Red color (positive values of Δn) represents the regions where the electron charge is higher in forward bias, while blue (negative values) indicates a higher concentration in reverse bias. At room temperature, positive values of Δn near the sidewalls of the channel appear for both devices, corresponding to the typical lateral field-effect SSD behavior, where a positive applied voltage opens the channel and a negative one depletes it. This response is kept for 200 K where the positive values are located in the middle of the channel, due to the fact that it is practically pinched off by the surface states at equilibrium. However, for T below 200 K, the patterns change, especially for the narrow SSD, where negative values appear at the anode (right) side of the channel. This behavior, opposite to what is expected in SSDs, indicates an enhanced concentration in reverse bias due to the previously discussed decrease of the surface charge density, which leads to a higher current.

To better understand these results and clarify their influence on both the values of R and γ, Fig. 6 shows the vertical profile of carrier concentration (n) along the center of the channel for both applied voltages ($V = 0.1$ and $V = -0.1$ V). At 300 K, the larger W_{eff} and the higher carrier concentration in the wider diode explain the lower values of R for the 150 nm wide SSD. On the other hand, the tiny differences between forward and reverse bias concentrations justify the small positive values of γ observed in both devices.

As T decreases, a considerable reduction of n takes place due to the higher values of $\sigma(V, T)$, Figs. 6(b) and 6(c). In contrast with the room temperature case, W_{eff} is similar in both devices and a surprisingly higher n is found for the narrow SSD due to the lower value of the surface charge of this device. This remarkable result is the reason why the resistance of the SSD with $W = 80$ nm is lower than for $W = 150$ nm even if W_{eff} is similar (R is inversely proportional to n) and is at the origin of the anomalous crossover of the R vs T curves of both devices. Additionally, the difference between n observed at $+0.1$ and -0.1 V is higher for the diode with $W = 150$ nm, especially at 100 K, which, together with the lower values of n, lead to a higher bowing coefficient (γ is proportional to $\Delta n/n$). The different sign of γ in the two SSDs is explained by the fact that the higher values of n are obtained for $V = +0.1$ V in the wide SSD (positive γ) while they are higher for $V = -0.1$ V in the narrow one (negative γ).

IV. CONCLUSIONS

In this work, two GaN-based SSDs with different widths (80 and 150 nm) have been analyzed in a temperature range from 100 to 300 K by means of a semi-classical MC simulator. We have demonstrated that the charges trapped at surface states in the sidewalls of the channel play a key role in the unexpected decrease of the current at low temperatures. Consequently, the analysis of the surface charge density is fundamental to explain the experimental I–V curves. Within a CCM to account for surface charges, a bias-independent value of σ has proven to be enough to replicate the experiments for $T \geq 220$ K. The evolution of σ_0 with T is consistent with the temperature behavior of R extracted from experiments. In this range of T, the smaller W_{eff} found in the 80 nm wide SSD makes its resistance higher (lower current). However, for $T \leq 220$ K, including the bias dependence of the surface charge, $\sigma(V, T)$ is necessary to fit the I–V curves, which is determined by means of an algorithm comparing the experimental DC curve at each T with simulations for different values of σ. The carrier concentration provided by MC simulations has helped us to interpret the observations, being especially relevant at low T, where the higher R found in the wider SSD is related to its lower carrier concentration (in spite of a similar W_{eff}) originated by an enhanced surface charge. On the other hand, the sign change of γ found when $T \leq 150$ K in the narrower diode is also explained in terms of n, which becomes higher in reverse bias than in forward bias (opposite to what is expected from the typical lateral field effect at the base of the SSD non-linear behavior).

The values obtained for $\sigma(V, T)$ help us to understand the physical mechanisms underlying the experimental findings. First, the narrower channels allow for a lower amount of carriers to approach the surfaces once the effective width decreases to become nearly null (at low temperature), so that less charge is trapped at the surfaces and the electron concentration in the channel is higher (and also the conductance). On the other hand, the change of sign of γ for the narrower devices is a consequence of a decrease of the value of σ in reverse bias, which can be associated with an enhanced release of the electrons trapped at the surface states. This happens only at low temperature, at which the release rate decreases due to a lower thermal energy, and for narrow channels. Under these conditions, the electric field appearing at the interface, which plays a key role in the surface charge trapping/release mechanisms, is able to modulate the tunneling probability and the charge release rate. All these effects are globally accounted for in our empirical model by means of the values of $\sigma(V, T)$ fitting the I–V curve.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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