Comparison Between the Dynamic Performance of Double- and Single-Gate AlInAs/InGaAs HEMTs

Beatriz G. Vasallo, Nicolas Wichmann, Sylvain Bollaert, Yannick Roelens, Alain Cappy, *Senior Member, IEEE*, Tomás González, *Senior Member, IEEE*, Daniel Pardo, and Javier Mateos

***Abstract*—The static and dynamic behavior of InAlAs/InGaAs double-gate high-electron mobility transistors (DG-HEMTs) is studied by means of an ensemble 2-D Monte Carlo simulator. The model allows us to satisfactorily reproduce the experimental performance of this novel device and to go deeply into its physical behavior. A complete comparison between DG and similar standard HEMTs has been performed, and devices with different gate lengths have been analyzed in order to check the attenuation of short-channel effects expected in the DG-structures. We have confirmed that, for very small gate lengths, short-channel effects are less significant in the DG-HEMTs, leading to a better intrinsic dynamic performance. Moreover, the higher values of the transconductance over drain conductance ratio g_m/g_d and, especially, the lower gate resistance R_g also provide a significant improvement of the extrinsic $f_{\max}$.**

***Index Terms*—Double-gate high-electron mobility transistor (DG-HEMT), dynamic behavior, Monte Carlo (MC) simulations.**

I. INTRODUCTION

InP-BASED high-electron mobility transistors (HEMTs) have proved to exhibit an excellent performance for applications in the microwave and millimeter-wave frequency ranges [1]. To further improve the frequency operation of these devices, their gate length L_g has been reduced down to the technological limit. In this way, a cutoff frequency f_t of 562 GHz and a maximum oscillation frequency $f_{\max}$ of 330 GHz have been obtained in a T-gate InAlAs/InGaAs pseudomorphic HEMT by reducing L_g down to 25 nm [2]. The reduction of the source and drain parasitic resistances by using a multilayer cap technology in a 30-nm-gate-length structure allowed us to reach an $f_{\max}$ of 400 GHz, together with a simultaneously high f_t of 547 GHz [3]. However, very small values of L_g involve the so-called short-channel effects (the gate capacitance does not scale with L_g anymore, and the transconductance g_m and the output conductance g_d are deteriorated), which limit the microwave performance of the HEMTs. To avoid these effects, a vertical scaling of the layer structure must go along with the reduction of the gate length in order to keep a high aspect ratio L_g/a, where a is the distance between the gate electrode and the 2-D channel electron gas. This scaling rule is limited by the emergence of a leakage current through the Schottky barrier at the gate; thus, this distance cannot be reduced to less than 8–10 nm. Then, f_t cannot scale up anymore with L_g. The device aspect ratio is consequently considered as the fundamental limit of HEMTs.

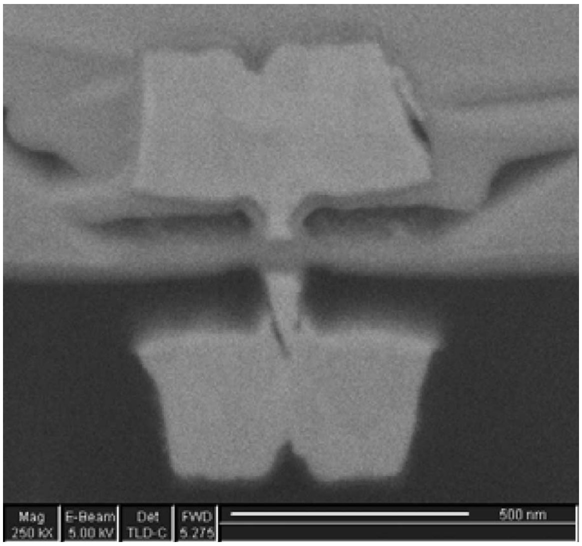

Fig. 1. SEM image of a 100-nm-gate DG-HEMT fabricated in the IEMN (Lille, France).

To keep on improving the frequency performance of these transistors (especially regarding $f_{\max}$), alternative solutions based on an evolution of the standard HEMT design have been considered. Thus, the double-gate HEMT (DG-HEMT), which is a HEMT with two gates placed on each side of the conducting InGaAs channel (see Fig. 1), has been recently developed [4]–[6]. Even if this idea was conceived some time ago for Si-devices [7]–[9], the authors in [4]–[6] show, for the first time to our knowledge, the fabrication of DG-transistors on III–V materials. In those previous works [4]–[6], we have reported the fabrication of a 100-nm T-gate DG-HEMT, which exhibits a very high extrinsic g_m and a good pinchoff behavior (lower g_d) as compared with the conventional single-gate (SG)-HEMT. This happens since the DG geometry can provide a better charge control and counteracts the effect of carrier injection into the buffer (since no buffer is used in the structure).

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B. G. Vasallo, T. González, D. Pardo, and J. Mateos are with the Departamento de Física Aplicada, Universidad de Salamanca, 37008 Salamanca, Spain (e-mail: bgvasallo@usal.es; javierm@usal.es).

N. Wichmann, S. Bollaert, Y. Roelens, and A. Cappy are with the Institut d'Electronique, de Microélectronique et de Nanotechnologies–Département Hyperfréquences et Semiconducteurs, 59652 Villeneuve d'Ascq, France.

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In order to better understand the intrinsic performance and to provide a theoretical model for this brand-new device, we present a complete study of $\mathrm{In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As}$ DG-HEMT structures carried out by means of a semiclassical 2-D ensemble Monte Carlo (MC) simulator [10]–[12]. Our model allows us to satisfactorily reproduce the static and dynamic performances of the experimental DG-HEMT presented in [5] and [6], thus confirming its validity for the simulation of DG-devices. It also provides a fully microscopic interpretation of the differences in the static and dynamic performances of the DG-HEMT, in comparison with a similar standard SG-HEMT. In addition, devices with different L_g are simulated to verify the expected attenuation of short-channel effects in DG-devices.

This paper is organized as follows. In Section II, the physical model employed in the analysis is described. Later, the comparison between the experimental and simulated 100-nm DG- and SG-HEMTs, both of static characteristics and small signal equivalent circuit (SSEC) parameters, is presented in Section III in order to validate our model. In Section IV, the MC results for the 100- and 50-nm-gate-length devices are shown. Finally, in Section V, the most important conclusion of this paper is drawn.

II. PHYSICAL MODEL

For the calculations, we make use of a semiclassical ensemble MC simulator, self-consistently coupled with a 2-D Poisson solver whose validity has been previously checked for conventional HEMTs [10]–[12]. The model takes into account important physical effects, as the influence of degeneracy in the electron accumulation appearing in the channel by using the rejection technique [10]. The schemes of the DG- and SG-device topologies used in the simulations are shown in Fig. 2. They are a recessed $\mathrm{In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As}$ DG-HEMT and the corresponding standard SG-HEMT. The layer structure is similar to that of the 100-nm-gate fabricated transistors [5], [6] to establish a correspondence with the experimental measurements.

Our MC algorithm allows us to analyze transistors with different gate lengths (the experimental one, where $L_g = 100$ nm, and the shorter ones, where $L_g = 25$ and 50 nm) to check the attenuation of short-channel effects expected for DG-devices with respect to standard SG-HEMTs. In order to provoke important short-channel effects and thus facilitate the study, the scaling down of the vertical dimensions is not performed when reducing L_g from 100 to 50 and 25 nm (the vertical thicknesses of the different layers are kept the same).

With regard to the dynamic behavior, the same intrinsic SSEC is considered for both types of devices [10]–[13]. This is correct as long as the DG-HEMT works in a common mode, i.e., the potential applied at both gate electrodes ($V_{\mathrm{GS1}} = V_{\mathrm{GS2}} = V_{\mathrm{GS}}$) is identical. The SSEC is calculated, taking as a basis the Y-parameters, obtained by using the typical MC technique [13]. After that, the intrinsic cutoff frequency f_C is calculated as $g_m/2\pi C_{\mathrm{gs}}$. Finally, having established a correspondence between measurements and MC results, the experimental parasitic elements can be taken into account in the SSEC for the correct calculation of the extrinsic f_t and $f_{\max}$.

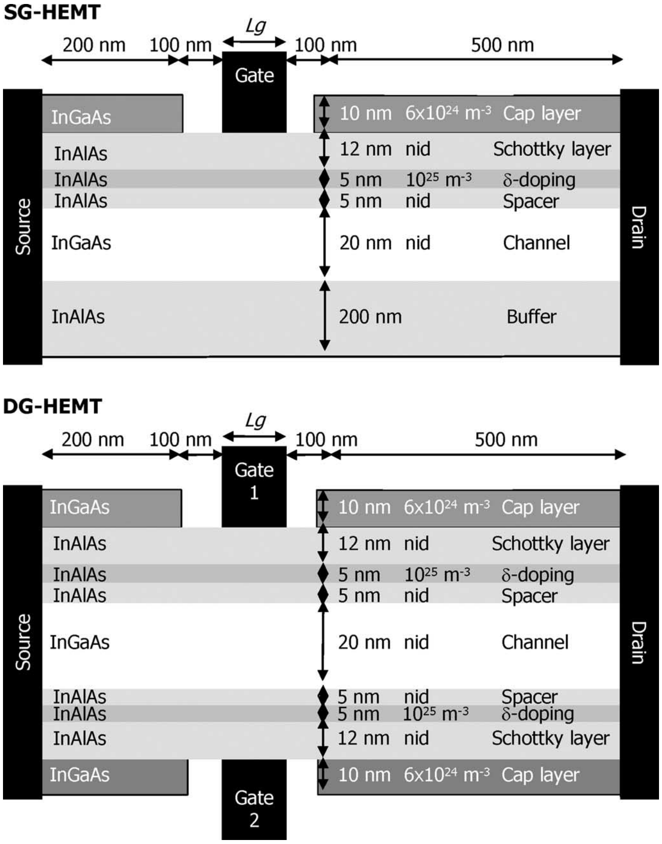

Fig. 2. Schematic drawing of the simulated SG- and DG-HEMTs.

III. COMPARISON BETWEEN EXPERIMENTAL AND MC RESULTS

In order to carry out the comparison of the measured results (extrinsic) with those obtained from the simulation (intrinsic), it is necessary to include, in a postprocessing stage, the parasitic elements that are not considered in the intrinsic MC model. Thus, drain (R_D^{met}) and source (R_S^{met}) parasitic resistances associated with metallizations have been incorporated into the original MC results, with the best fit being obtained for $R_D^{\mathrm{met}} = 0.15\ \Omega \cdot \mathrm{mm}$ and $R_S^{\mathrm{met}} = 0.10\ \Omega \cdot \mathrm{mm}$, which are found to coincide in both devices. By separately adjusting the surface charge at the cap layer and at the bottom of the recess (6.2×10^{16} and $4.3 \times 10^{16}\ \mathrm{m}^{-2}$, respectively), the static characteristics of the experimental 100-nm-gate DG- and SG-HEMTs [5] can be very nicely reproduced by our MC simulator, as shown in Fig. 3.

Regarding the dynamic behavior of the HEMTs, Fig. 4 shows the comparison between the experimental and the MC values of the main intrinsic SSEC parameters (g_m, g_d, C_{gs}, and C_{gd}) for the 100-nm-gate DG- and SG-HEMTs, where $V_{\mathrm{DS}} = 0.5$ V. For the calculation of the MC results, in order to extract the actual intrinsic SSEC, the access resistances corresponding to the ohmic regions near the source and drain electrodes R_S^{acc} and R_D^{acc}, respectively, are removed from the raw simulated values. The values for these parameters are extracted from the experimental measurements (in the 100-nm-gate devices) of the total parasitic resistances R_S^{exp} and R_D^{exp} by subtracting the resistances of metallizations, providing the

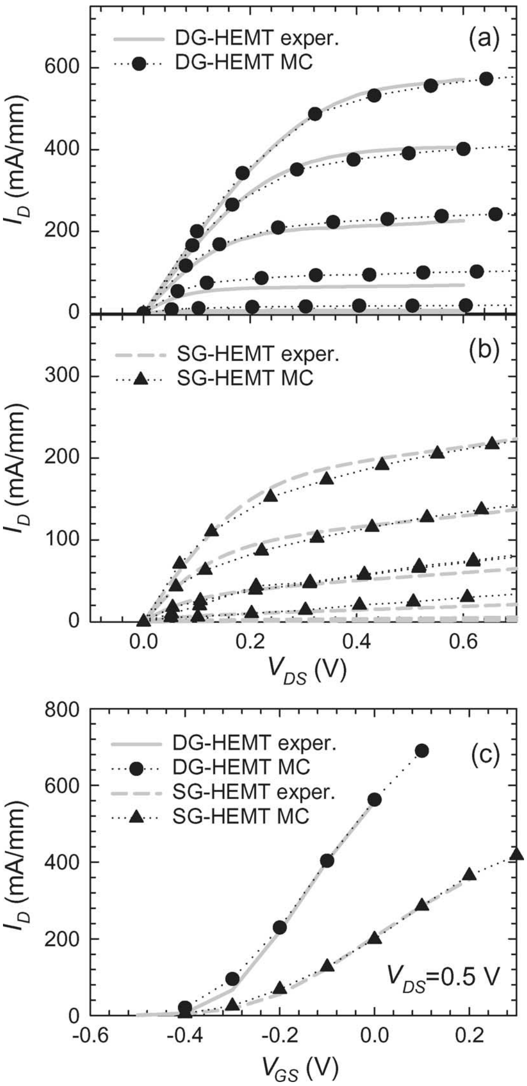

Fig. 3. Comparison of the extrinsic $I_D - V_{\mathrm{DS}}$ curves measured in fabricated 100-nm-gate (a) DG- and (b) SG-HEMTs with those obtained from the MC simulation of similar devices. The gate voltage of the top curves is $V_{\mathrm{GS}} =$ 0.0 V, and the step of the gate bias is $\Delta V_{\mathrm{GS}} = 0.1$ V for both sets of curves. (c) Corresponding $I_D - V_{\mathrm{GS}}$ curves for $V_{\mathrm{DS}} = 0.5$ V.

following: $R_S^{\mathrm{acc}} = R_S^{\mathrm{exp}} - R_S^{\mathrm{met}} = 0.08\ \Omega \cdot \mathrm{mm}$ and $R_D^{\mathrm{acc}} = R_D^{\mathrm{exp}} - R_D^{\mathrm{met}} = 0.11\ \Omega \cdot \mathrm{mm}$ in the DG-HEMT and $R_S^{\mathrm{acc}} = 0.23\ \Omega \cdot \mathrm{mm}$ and $R_D^{\mathrm{acc}} = 0.22\ \Omega \cdot \mathrm{mm}$ in the SG-HEMT. The same values are used for the 50-nm-gate devices. Note that the access resistances are lower for the DG-HEMT than for the SG-device due to the higher carrier concentration.

In addition, it is necessary to include the so-called "external" geometric capacitances between the contact accesses $C_{\mathrm{gs}}^{\mathrm{ext}}$ and $C_{\mathrm{gd}}^{\mathrm{ext}}$ (extracted from the comparison of the results of the simulations at $I_D = 0$ with the experimental measurements, as explained in [10] and [11]). The values obtained for the 100-nm-gate devices (which will also be used for the 50-nm ones since the same layout is considered) are the following: $C_{\mathrm{gs}}^{\mathrm{ext}} = 280$ fF/mm and $C_{\mathrm{gd}}^{\mathrm{ext}} = 255$ fF/mm for the DG-HEMT and $C_{\mathrm{gs}}^{\mathrm{ext}} = 210$ fF/mm and $C_{\mathrm{gd}}^{\mathrm{ext}} = 152$ fF/mm for the SG-HEMT.

In general, we find a good agreement between the experimental and the MC results for g_m and C_{gd} for both DG- and SG-transistors. The discrepancy in the values of g_d for high V_{GS} can be attributed to the experimental frequency dispersion due to traps and other layer defects which are not included in the MC model. It seems that, in a dynamic operation, the devices are more resistive, so that the stationary bias point, which is in the saturated region of the I–V curves, may be shifted to the linear part of the characteristics (providing the increase of g_d for high V_{GS}). Indeed, the static value of g_d is well reproduced by the simulations, as confirmed by the satisfactory agreement of the I–V curves [Fig. 3(a) and (b)]. On the other hand, MC simulations somewhat underestimate the values of C_{gs}, mainly in the DG-HEMT (even if the agreement can be considered reasonable up to $V_{\mathrm{GS}} = -0.2$ V). The cause for this discrepancy can again be the not-considered layer defects. We remark that experimental Hall measurements show a degradation of the mobility in the channel of the DG-HEMTs. This fact, together with the common overestimation of the electron velocity given by the ideal MC model [10]–[12], means that the electron concentration in the simulations fitting the experimental values of I_d and g_m is probably lower than the real one (mainly in the DG-HEMT), which can also lead to lower values of C_{gs}.

IV. MC COMPARISON BETWEEN DG- AND SG-HEMTs

The simulated extrinsic output characteristics for 100- and 50-nm-gate DG (where $V_{\mathrm{GS1}} = V_{\mathrm{GS2}} = V_{\mathrm{GS}}$) and SG-HEMTs with a device width of $W = 100\ \mu$m are shown in Fig. 5. The drain current provided by the DG-HEMTs is about twice that given by the SG-transistors (as shown in Fig. 3). This occurs because the electron concentration in the DG-HEMT channel is significantly higher than in the conventional HEMT (for both values of L_g) due to the presence of two charge-accumulation regions. This can be appreciated in Fig. 6, where the electron density profile along the vertical direction under the gate of the 100-nm DG- and SG-HEMTs is presented ($V_{\mathrm{DS}} = 0.5$ V and $V_{\mathrm{GS}} = -0.1$ V).

The immunity to short-channel effects in the static characteristics achieved with the DG-architecture is confirmed by the results shown in Fig. 7, which reports the behavior of the threshold voltage (V_T, calculated by extrapolating to zero current the $\sqrt{I_D}$ versus V_{GS} plot) when shortening L_g. In Fig. 7(a), it is observed that the V_T roll-off is less pronounced in the DG-structure than in the SG-one. Drain-induced barrier lowering (DIBL, calculated as the difference between the values of V_T for $V_{\mathrm{DS}} = 1.0$ and 0.5 V) is also reduced in the DG-device, as shown in Fig. 7(b). Regarding subthreshold swing, the value experimentally found in the DG-structure (75 mV/dec) is much lower than in the SG-HEMT (125 mV/dec) for the 100-nm-gate devices. This parameter cannot reliably be calculated with MC simulations because of the extremely low current level.

With regard to the dynamic behavior of the transistors, Fig. 8 shows that the MC values of g_m are notably higher in the DG than in the conventional HEMT due to the approximately double charge in the channel. When decreasing L_g, an increase of g_m would be expected, but this does not happen. This is due to the nonoptimized layer structure of the 50-nm-gate devices.

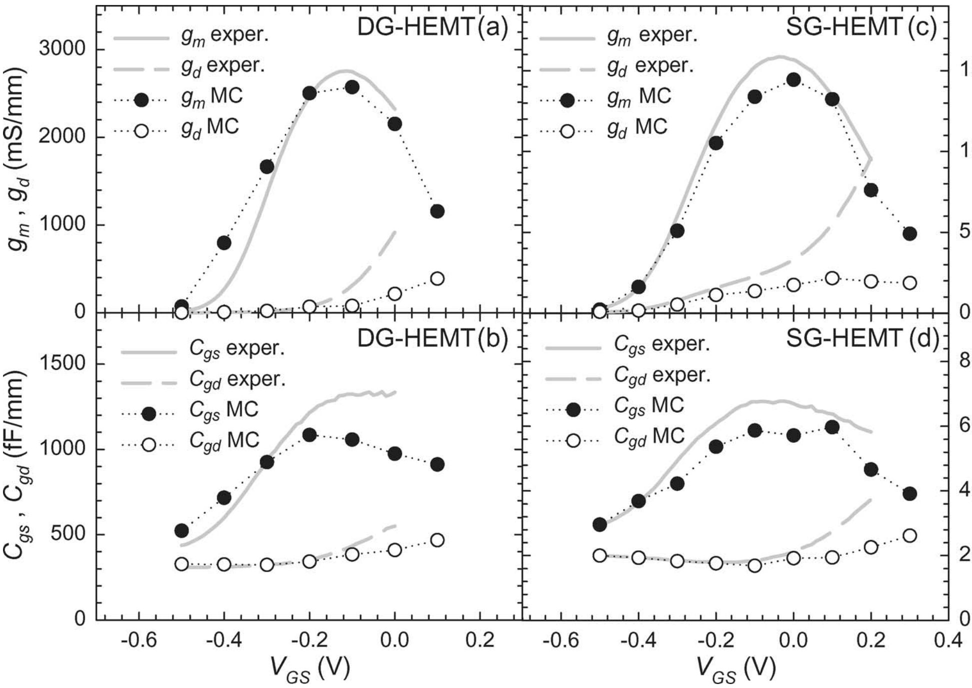

Fig. 4. Experimental and MC values of (a) and (c) g_m and g_d, and (b) and (d) C_{gs} and C_{gd} versus V_{GS} for the 100-nm-gate (a) and (b) DG- and (c) and (d) SG-HEMTs. $V_{\mathrm{DS}} = 0.5$ V.

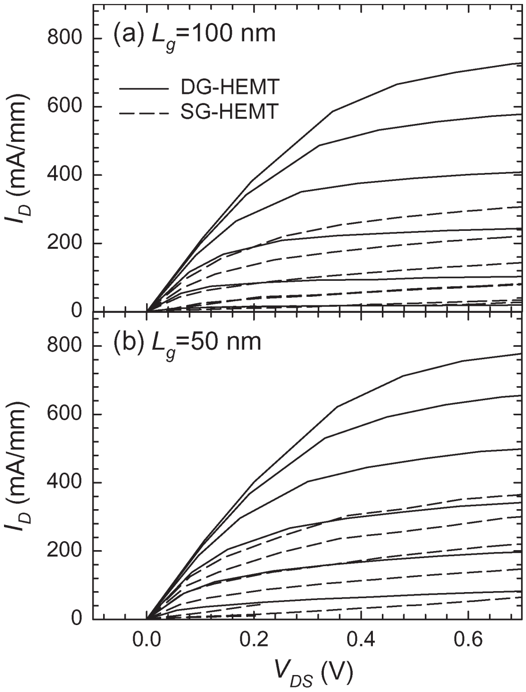

Fig. 5. MC extrinsic output characteristics for the (a) 100-nm- and (b) 50-nm-gate DG- and SG-HEMTs that are shown in Fig. 2. The gate voltage for the top curves is $V_{\mathrm{GS}} = 0.1$ V, and the step of the gate bias is $\Delta V_{\mathrm{GS}} = 0.1$ V.

This short-channel effect is more evident in the SG-HEMT, for which g_m decreases when reducing L_g, while in the case of the DG-HEMT, it remains approximately the same, which is a clear evidence of the expected attenuation of short-channel effects in DG-HEMTs. This result constitutes a remarkable proof of the improved charge control achieved by the presence of two gates. Another improvement introduced by the new device geometry is the reduction of g_d, which is shown in Fig. 8(b) (at least up to $V_{\mathrm{GS}} = -0.1$ V, where the DG-HEMTs approach the linear region and g_d sharply increases), due to the absence of buffer in those structures. An increase in g_d is appreciated in both types of devices when reducing L_g due to the enhanced short-channel effects. It is noticeable that the combined effects of a higher g_m and a lower g_d induce an extremely high intrinsic unloaded voltage gain g_m/g_d in the DG-HEMTs, which is more than three times than that obtained for the SG-HEMTs. This fact, as will be shown later, leads to an improved value of $f_{\max}$.

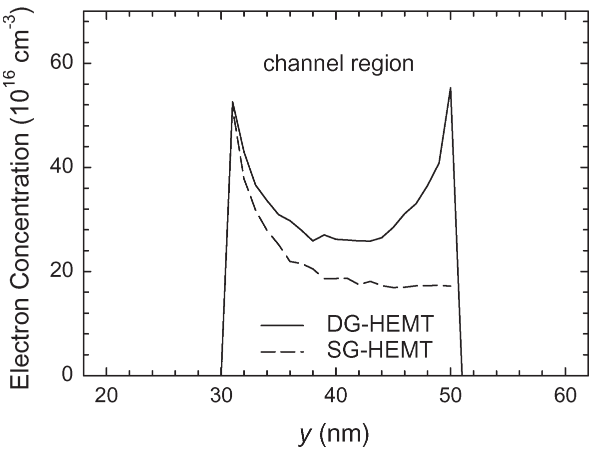

Fig. 6. Transversal profile of electron concentration under the gate for the simulated 100-nm DG- and SG-HEMTs. The top gate is at the left, and the bottom gate (or the substrate) is at the right side of the graph. $V_{\mathrm{DS}} = 0.5$ V and $V_{\mathrm{GS}} = -0.1$ V.

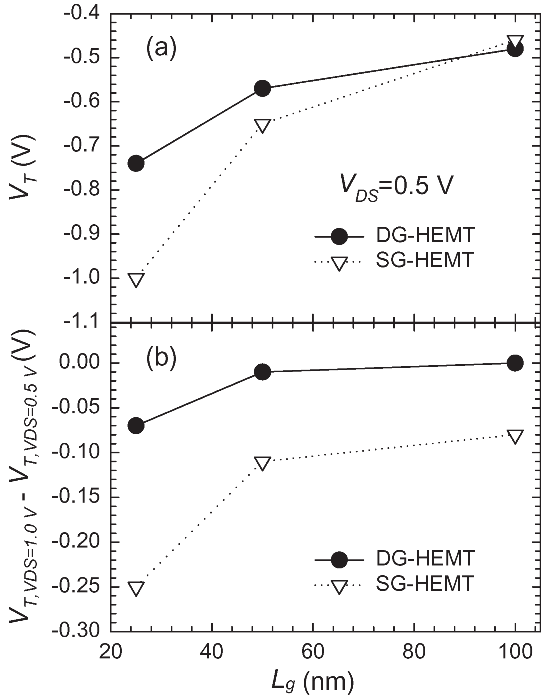

Fig. 7. (a) V_T for $V_{\mathrm{DS}} = 0.5$ V and (b) DIBL, calculated as the difference between V_T for $V_{\mathrm{DS}} = 1.0$ V and 0.5 V, for the simulated SG- and DG-HEMTs as a function of L_g.

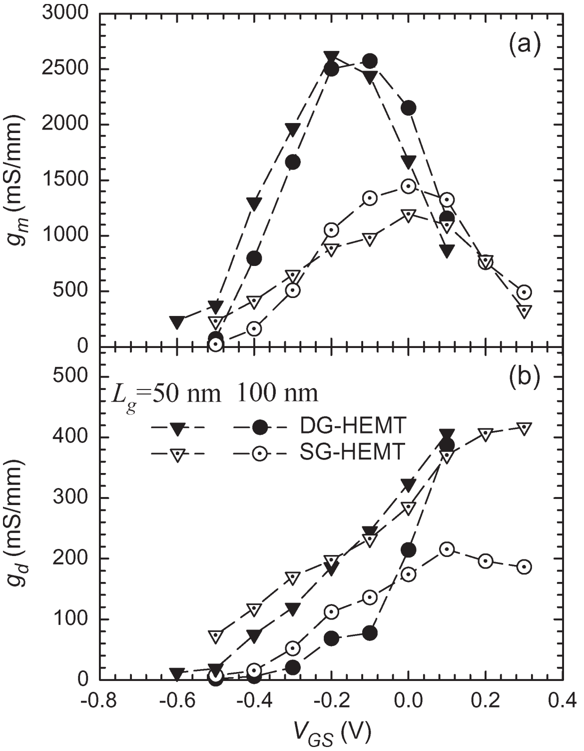

Fig. 8. MC values of (a) g_m and (b) g_d versus V_{GS} for the 50- and 100-nm-gate DG- and SG-HEMTs. $V_{\mathrm{DS}} = 0.5$ V.

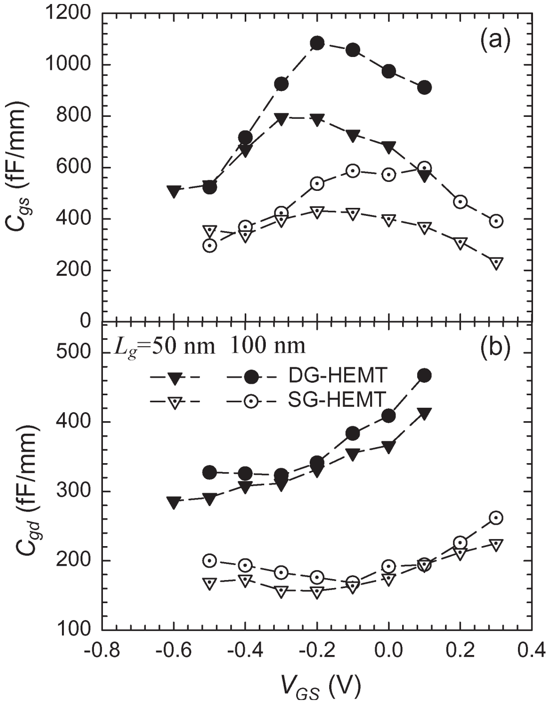

Fig. 9. MC values of (a) C_{gs} and (b) C_{gd} versus V_{GS} for the 50- and 100-nm-gate DG- and SG-HEMTs. $V_{\mathrm{DS}} = 0.5$ V.

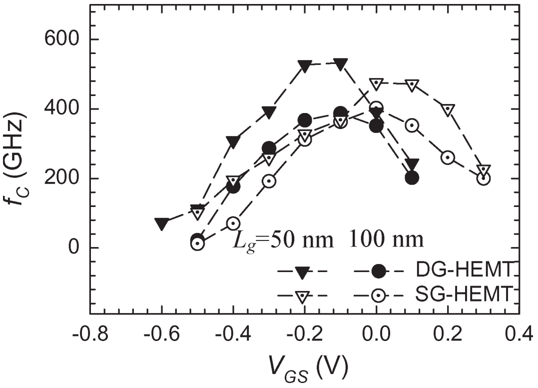

Fig. 10. MC values of f_C versus V_{GS} for the 50- and 100-nm-gate DG- and SG-HEMTs. $V_{\mathrm{DS}} = 0.5$ V.

The MC values of the gate-to-source C_{gs} and gate-to-drain C_{gd} capacitances for the different transistors are shown in Fig. 9. It can be observed that the values of both C_{gs} and C_{gd} are almost twice in the DG-HEMT as compared to the conventional HEMT due to the presence of two gates and two regions of electron accumulation in the channel (Fig. 6). The reduction of the gate length affects the capacitances of both types of devices in a similar way: C_{gs} decreases (even if its reduction is not proportional to L_g due to short-channel effects) and C_{gd} remains almost the same (the intrinsic contribution is almost negligible with respect to the "external" geometric capacitance).

The MC intrinsic cutoff frequency f_C of the simulated devices is shown in Fig. 10 as a function of V_{GS} for $V_{\mathrm{DS}} = 0.5$ V. The significant increase of g_m in the DG with respect to the SG-HEMTs is compensated by the higher values of C_{gs}, thus surprisingly providing lower values of f_C for the 100-nm-gate DG with respect to the SG-devices. Evidently, the value of $C_{\mathrm{gs}}^{\mathrm{ext}}$ has a strong influence on these results for f_C, and it must be minimized, as much as possible, in the design of the experimental devices. This qualitative behavior is in good agreement with the experimental measurements, even if the simulated values of f_C are somewhat higher (MC simulations predict a maximum of 401 and 387 GHz for the SG- and DG-HEMTs, respectively, whereas the measurements reach only 369 and 320 GHz, respectively), which can be attributed to the overestimation of the electron mobility in the channel and the lower values of C_{gs} [Fig. 4(b)]. In addition, the difference between the simulated values of f_C for SG- and DG-devices is reduced, as compared to the measurements due to the degradation of the mobility in the DG-HEMT. It is also important to remark that, when reducing L_g, the maximum f_C significantly increases in the DG-device, becoming higher than the SG-one, where a small improvement of f_C is found due to the more pronounced increase of short-channel effects and the consequent deterioration of g_m. In spite of the slight discrepancy between experimental and MC results, the simulations provide very useful information about the comparison of the purely intrinsic performance of DG- and SG-HEMTs. In fact, our simulations show that, as long as the devices have a sufficient aspect ratio (thus avoiding important short-channel effects, as in the case of 100-nm devices), the DG architecture does not provide any significant improvement with respect to the SG-HEMTs in terms of f_C, but when short-channel effects are more pronounced, the improvement obtained with DG-structures can be significant (as in the case of 50-nm-gate devices).

In order to complete the comparison of the DG- and SG-HEMT dynamic behavior, we have obtained the values of their extrinsic cutoff frequencies $f_{\max}$ and f_t, defined as the values for which the unilateral gain U and the short-circuit current gain H_{21} is equal to one, respectively. In contrast to f_C, only regarding the intrinsic performance of the devices (and not being influenced by the values of g_d or C_{gd}), $f_{\max}$ and f_t account for the device parasitics [5], [6] and provide more practical information about the dynamic performances of the devices for analog and digital applications, respectively. For example, the fact that the DG-HEMT benefits from two gates in parallel is of great importance, thus reducing its gate resistance to nearly half that of the SG-HEMT ($R_G = 17$ and 38 Ω/mm, respectively). In addition, as shown before, source and drain access resistances (R_S^{acc} and R_D^{acc}) are much lower in the DG-HEMTs. The MC values of $f_{\max}$ and f_t as a function of the gate bias are shown in Fig. 11 (the inset shows the typical frequency behavior of U and $|H_{21}|^2$), and their maximum values are presented in Table I. f_t is calculated by extrapolating the low-frequency behavior of H_{21}, while $f_{\max}$ is the exact value for which $U = 1$ (thus correctly considering the frequency dependence of U, as explained in [12]).

In Fig. 11(a), it is observed that, in the 100-nm-gate DG-HEMT, the values taken by $f_{\max}$ are higher than in the SG-structure. More exactly, the simulations show a significant improvement (around 30%) in the maximum values of $f_{\max}$: 287 GHz for the DG-HEMT and 226 GHz for the SG-HEMT (in good agreement with the results of the measurements, which are 288 and 220 GHz, respectively). Regarding f_t [Fig. 10(b)], the simulations and the experiments show similar values for the 100-nm-gate DG- and SG-devices (around 200 GHz). When reducing L_g to 50 nm, $f_{\max}$ is about the same in both types of devices due to the important short-channel effects provoked by the reduced aspect ratio. On the contrary, the value of f_t in the DG-HEMT increases with respect to the 100-nm-gate device (reaching 258 GHz, which is an important 20% increase), while it is not improved in the SG-HEMT (the increase of f_C is higher in the DG-HEMT; Fig. 10). As shown in Fig. 11, the improvement of $f_{\max}$ in the DG-architecture is greater than that of f_t due to a reduced value of R_g and g_d, which have a significant influence on $f_{\max}$, without much affecting the value of f_t. For this same reason, the strong degradation of g_d when decreasing the gate length prevents the increase of $f_{\max}$, while f_t is improved.

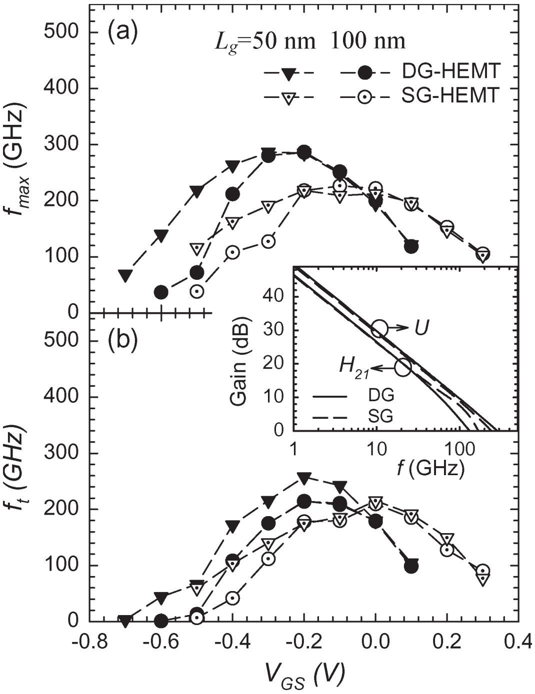

Fig. 11. MC values of (a) $f_{\max}$ and (b) f_t versus V_{GS} for the 50- and 100-nm-gate DG- and SG-HEMTs. $V_{\mathrm{DS}} = 0.5$ V. The inset shows U and $|H_{21}|^2$ versus frequency for the 100-nm devices for a gate bias corresponding to the maximum $f_{\max}$.

TABLE I
MAXIMUM VALUES OF $f_{\max}$ AND f_t FOR THE DIFFERENT DEVICES OBTAINED WITH MC SIMULATIONS. $V_{\mathrm{DS}} = 0.5$ V

f_{max} (GHz)	L_g=100 nm	L_g=50 nm
SG-HEMT	226	218
DG-HEMT	287	286

f_t (GHz)	L_g=100 nm	L_g=50 nm
SG-HEMT	209	215
DG-HEMT	214	258

These results show that, even if the purely intrinsic behavior of DG-devices is not much improved with respect to the standard SG-architecture when devices have a sufficiently high aspect ratio, DG-HEMTs demonstrate a noticeably superior extrinsic frequency performance and a higher immunity to short-channel effects due to the reduced parasitic resistances and lower drain conductance.

V. CONCLUSION

We have presented an MC-based study of DG-HEMTs, comparing their static and dynamic performances with standard SG-devices. The good agreement between the experimental and simulated results is the starting point for the comparison of the intrinsic and extrinsic behaviors of both types of devices, without being affected by the technological problems that can hinder an experimental comparison (as it happens with the degradation of the electron mobility in the DG-HEMT). The simulations of the 50- and 25-nm-gate devices with low aspect ratio clearly demonstrate the expected improved immunity to short-channel effects in the static characteristics of DG-HEMTs with respect to SG-structures (in terms of the behavior of V_T roll-off, DIBL, and subthreshold swing). However, the improvement of the purely intrinsic dynamic behavior of the DG-HEMTs over the standard devices does not come out in well-designed devices since the increase of g_m is partially compensated by higher values of $C_{\rm gs}$. However, the differences are more evident when comparing the extrinsic $f_{\max}$. The higher g_m/g_d, together with lower R_g and source and drain access resistances, leads to significantly higher values of $f_{\max}$ in the DG-HEMTs.

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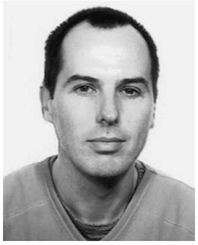
Beatriz G. Vasallo was born in Salamanca, Spain, in 1978. She received the degree in physics and the Ph.D. degree from Universidad de Salamanca, Salamanca, in 2000 and 2005, respectively.

She was with the Institut d'Electronique, de Microélectronique et de Nanotechnologies, University of Lille, France, for a year. She is currently an Assistant Professor with the Departamento de Física Aplicada, Universidad de Salamanca. Her current research interest includes modeling and optimization of the high-frequency and low-noise performance of advanced HEMTs.

Nicolas Wichmann was born in Valenciennes, France, on January 5, 1979. He received the Ph.D. degree from the Institut d'Electronique, de Microélectronique et de Nanotechnologies (IEMN), University of Lille, Villeneuve d'Ascq, France, in 2005, for his work on the design, fabrication, and characterization of double-gate HEMTs using InAlAs/InGaAs materials.

He is currently an Associate Professor with the IEMN–Département Hyperfréquences et Semiconducteurs. His main research is focused on the design and process development of novel nanoscaled devices for ultrahigh-speed frequency application. He is currently involved in the realization and characterization of III–V compounds velocity modulation transistor.

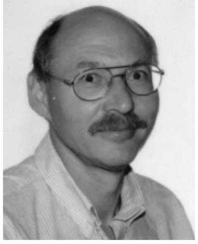


Sylvain Bollaert was born in Calais, France, on February 17, 1965. He received the Ph.D. degree from the University of Lille, Villeneuve d'Ascq, France, in 1994.

He is an Associate Professor with the Institut d'Electronique, de Microélectronique et de Nanotechnologies–Département Hyperfréquences et Semiconducteurs. His main research interest includes fabrication of nanoscaled devices and monolithic microwave integrated circuits (MMICs). For the last three years, he developed the fabrication process for the 50-nm-gate-length HEMTs using InAlAs/InGaAs lattice-matched and pseudomorphic HEMT on InP and metamorphic HEMT on GaAs. He is currently involved in the realization of ultrahigh-speed MMICs using such devices and in the development of sub-50-nm-gate-length HEMTs. His other research work includes study and realization of ballistic devices and transferred-substrate HEMTs for terahertz-frequency applications.

Yannick Roelens was born in Villeneuve d'Ascq, France, on May 3, 1972. He received the Ph.D. degree from the University of Lille, Villeneuve d'Ascq, in 2000. His dissertation was on the application of high-Tc superconductors in microwave.

Since September 2001, he has been an Associate Professor with the Institut d'Electronique, de Microélectronique et de Nanotechnologies–Département Hyperfréquences et Semiconducteurs. His main research interest includes fabrication of nanoscaled devices and microwave circuit. He is involved in the realization and characterization of ballistic devices.



Alain Cappy (M'92–SM'96) was born in Chalons sur Marne, France, on January 25, 1954. He received the Docteur en Sciences degree from the Institut d'Electronique, de Microélectronique et de Nanotechnologies (IEMN), University of Lille, Villeneuve d'Ascq, France, in 1986, for his work on the modeling and the characterization of MESFETs and HEMTs.

Since 1977, he has been with the IEMN–Département Hyperfréquences et Semiconducteurs, where he is currently the Director of the IEMN and a Professor of electronics and electrical engineering. His main research interests include modeling, realization, and characterization of ultrahigh-speed device and circuits for applications in the centimeter- and millimeter-wave ranges.

Tomás González (M'05–SM'07) was born in Salamanca, Spain, in 1967. He received the degree in physics and the Ph.D. degree in physics from Universidad de Salamanca, Salamanca, in 1990 and 1994, respectively.

Since 1991, he has been with the Departamento de Física Aplicada, Universidad de Salamanca, where he is currently a Full Professor of electronics. His main research activity is in the field of electronic transport in semiconductor materials and high-frequency electronic devices, with special application to the modeling of electronic noise by microscopic approaches. Recently, he is also involved in the development of novel device concepts based on ballistic transport. He is the author or coauthor of more than 100 refereed scientific journal papers and 150 conference presentations. He is a member of the Editorial Board of *Fluctuation and Noise Letters* (World Scientific).

Dr. González serves on the committees of several international conferences including the International Conference on Noise and Fluctuations (ICNF), Non-Equilibrium Carrier Dynamics in Semiconductors, and Trends in Nanotechnology. He was the Chairman of the 18th ICNF, held in Salamanca, in September 2005.

Daniel Pardo was born in Valladolid, Spain, in 1946. He received the degree in physics and the Ph.D. degree from the University of Valladolid, Valladolid, in 1971 and 1975, respectively.

From 1971 to 1981, he was with the Electronics Department, University of Valladolid, working on the characterization of semiconductor materials and modeling of semiconductor devices, where he became an Associate Professor in 1978. In 1981, he joined the Departamento de Física Aplicada, Universidad de Salamanca, Salamanca, Spain, where he has been a Full Professor since 1983 and the Head of the Semiconductor Devices Research Group. His current research interest includes Monte Carlo simulation of semiconductor devices, with a special application to noise characterization.

Javier Mateos was born in Salamanca, Spain, in 1970. He received the B.S. and Ph.D. degrees in physics from Universidad de Salamanca, Salamanca, in 1993 and 1997, respectively.

Since 1993, he has been with the Departamento de Física Aplicada, Universidad de Salamanca, where he became an Associate Professor in 2000. He has worked for one year with the Institut d'Electronique, de Microélectronique et de Nanotechnologies. His current research interest includes development of novel device concepts using ballistic transport, together with the modeling and optimization of high-frequency and low-noise performance of ultrashort-gate-length HEMTs.