Geometry and bias dependence of trapping effects in planar GaN nanodiodes

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***Abstract*— Pulsed and transient measurements performed in planar nanodiodes fabricated on an AlGaN/GaN heterolayer reveal the influence of surface and bulk traps on the I-V characteristic and AC impedance. Rectangular and V-shape diodes of different lengths and widths have been measured. Surface trapping effects become relevant in narrow channels, as the surface to volume ratio of the device is increased, while in wider rectangular and V-shape diodes bulk trapping effects prevail.**

Keywords—traps; GaN nanodiodes; pulse and transient measurements

I. INTRODUCTION

The presence of surface and bulk traps is a main issue in GaN devices, limiting their reliability [1]. Bulk traps are at the origin of effects like current collapse and current lags in FETs [2]. As the size of the devices is shrunk and the surface to volume ratio increases, surface trapping effects become relevant, especially when transport takes place near etched boundaries where surface states are present. This is the case of the so called Self-Switching Diodes (SSDs) analyzed in this paper [3], a particular type of nanodiode fabricated by etching L-shaped trenches on a semiconductor heterolayer, which define an asymmetric conducting channel, as shown in Fig. 1.

In this work we will focus on SSDs fabricated on AlGaN/GaN heterolayers [4]. These type of diodes have already shown a good capability to operate as detectors of sub-THz signals [5] and are being explored to operate as THz generators based on Gunn effect [6], but they suffer from problems related to traps. Indeed, carriers trapped at the sidewalls of the trenches defining the channel play a significant role in the behavior of GaN SSDs. In particular, they lead to an early saturation of their I-V curve [4] and may deteriorate their performance when operating as detectors, and even block the onset of Gunn oscillations. V-shaped geometries, Fig. 1(b), have been proposed as an alternative to standard rectangular diodes in order to alleviate such problems [6]. In this work we will analyze trap effects in rectangular and V-shaped GaN SSDs of different sizes by means of pulsed and transient measurements of I-V curves and AC impedances, trying to identify their location and determine their characteristic times.

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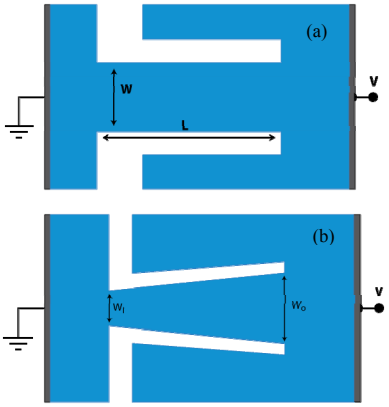

Fig. 1. (a) Rectangular and (b) V-shape geometries of the SSDs under analysis. Regions in white are insulating trenches.

II. DEVICES UNDER ANALYSIS

The SSDs under analysis were fabricated at IEMN on an epitaxial layer consisting of 1.8 µm of GaN on a high-resistivity Si substrate, with a barrier of 23 nm of $Al_{0.3}Ga_{0.7}N$. Measured values of sheet carrier density n_s in this epilayer are in the range 6-8×10^{12} cm^{-2}, with a Hall mobility around 1200 cm^2/Vs. The fabrication process starts by depositing ohmic contacts (Ti/Al/Ni/Au, with a resistance of 0.4 Ω mm) and isolation by ionic implantation (He^+). Then, the etching of the trenches takes place with a PMMA resist and inductively coupled plasma (ICP) chlorine based technology, and finally the top metal layer (Ti/Pt/Au) is deposited for coplanar waveguide access.

Several sizes and arrays of SSDs have been measured by means of a probe station connected to a semiconductor analyzer Keithley 4200 SCS with a pulse measurement unit (Keithley 4225-PMU) and a remote amplifier/switch (Keithley 4225-RPM), which allows us to perform ultrafast pulsed I-V measurements. A duty cycle of a 1% has been used with a minimum pulse width of 1 µs for the measured range.

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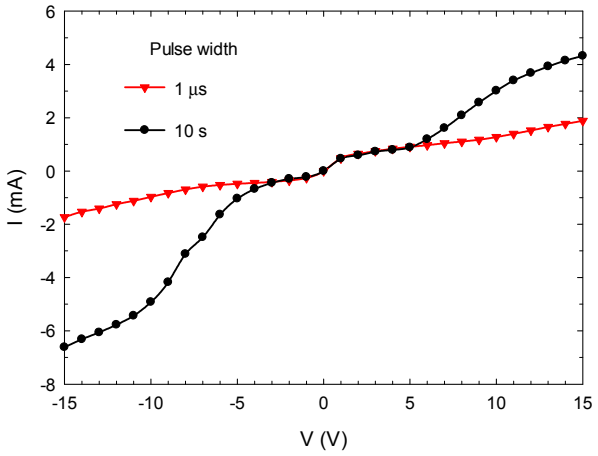

Fig. 2. Pulsed current-voltage characteristic of an array of 16 rectangular SSDs in parallel with L=1000 nm and W=75 nm. A duty cycle of 1% is used in the measurements.

III. RESULTS

Fig. 2 shows the measured pulsed current-voltage characteristic of an array of 16 rectangular SSDs in parallel with L=1000 nm and W=75 nm (narrow channel). As observed, for long pulse width (10 s) a significant increase in the measured current takes place for high-enough applied voltages. For short pulses (1 µs) the current saturates due to the fast trapping of electrons in states at the sidewalls of the channel [4]. Such electrons are partially released at longer times in the case of long pulses of high-enough amplitude, thus increasing the width of the effective conducting channel and allowing a higher current to flow. The threshold voltage for the described effect to take place is smaller in reverse (V < -3 V) than in forward bias (V >5 V), reflecting the asymmetry of the diodes.

Fig. 3(a) shows the measured current for different pulse widths and bias conditions in the same diode of Fig. 2. For pulse amplitudes higher than 5 V, the value of the current experiences a transition from a low value for short pulse width, I_0, to a high value for longer width, I_∞. The increase in the current is more pronounced the higher is the amplitude of the voltage pulse. By fitting the measurements to an expression of the type

$$I(t) = I_0 + (I_\infty - I_0)\exp(-t/\tau), \qquad (1)$$

it is possible to estimate a characteristic time of detrapping, τ [7]. Such a detrapping time is plotted in Fig. 3(b) as a function of the pulse amplitude, both in forward and reverse bias. The obtained values are in the range of s to ms, and they decrease as the voltage amplitude increases. Interestingly, for low voltages, the detrapping time is shorter in forward bias, however, the decrease with the voltage is more pronounced in reverse than in forward bias, so that for the highest applied voltages, τ is shorter in reverse bias.

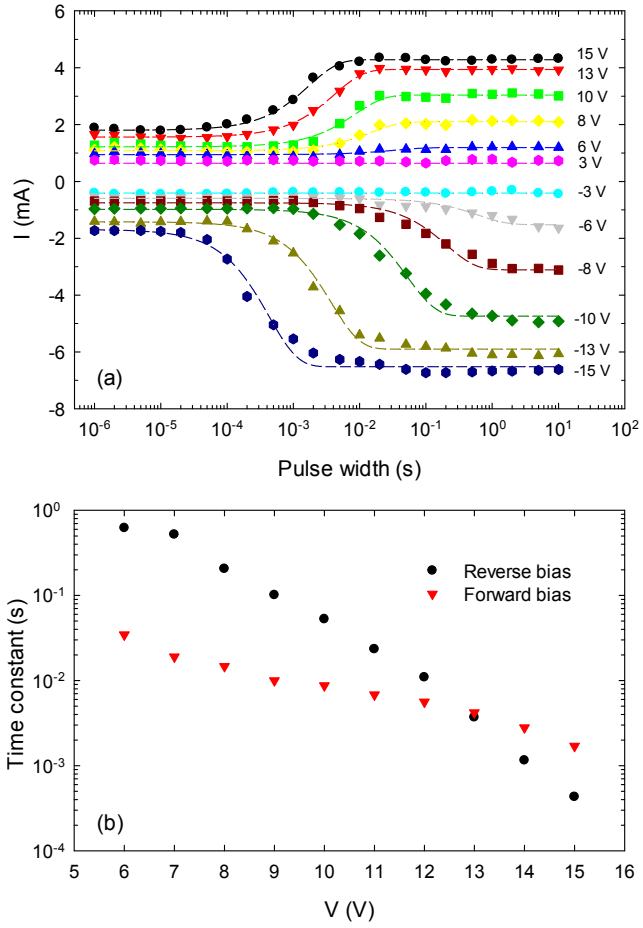

Fig. 3. (a) Symbols: measured current vs. pulse width for different bias conditions. Dotted lines: fitting of the measurements to (1). (b) Detrapping time constant extracted from the measurements in (a) vs. applied voltage. Results correspond to the SSDs of Fig. 2.

The observed effects are attributed to trapping/detrapping of electrons at the states present in the sidewalls of the trenches that define the channel, originated by the etching process. At equilibrium, the surface charges produce a depletion region near the interfaces of about 30 nm at each side of the channel. As a consequence, the 75 nm-wide channel is near to be completely depleted, its current level is low and the influence of the occupancy of surface states is very strong, since they modify quite noticeably the width of the conducting channel. As the width of the channel is increased, it is expected that such an influence is reduced. To confirm this behavior, we have measured pulsed I-V curves in the case of wider rectangular (L=2000 nm and W=500 nm) and V-shape (L=1000 nm, W_i=250 and W_o=550 nm) diodes, shown in Figs. 4(a) and 4(b), respectively. As expected, the effects observed in narrow channels are absent in these diodes, which, in contrast, exhibit lower current levels for measurements performed with long pulses. In these wider channels, surface effects are much less important and we attribute the observed behavior to the influence of both bulk traps and heating effects.

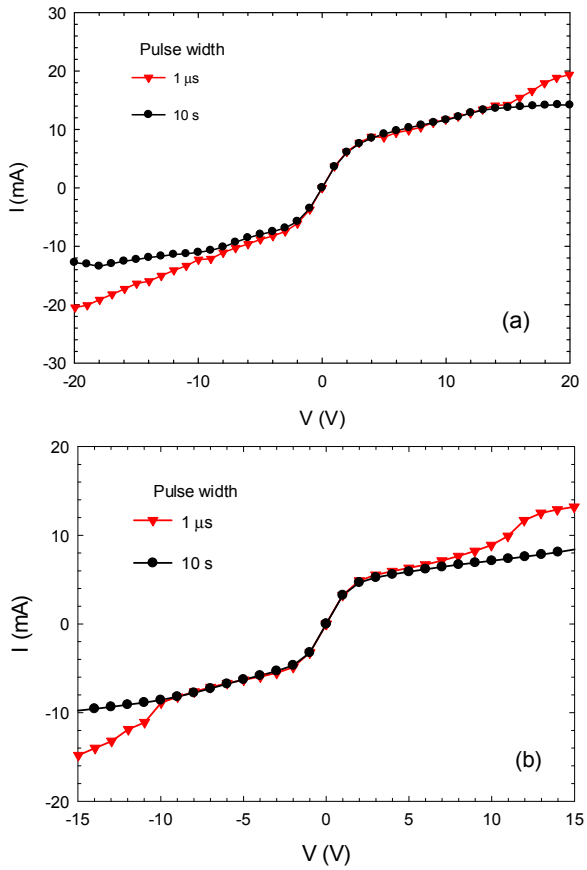

Fig. 4. Pulsed current-voltage characteristics of an array of (a) 16 rectangular SSDs in parallel with L=2000 nm and W=500 nm; and (b) 16 V-shape SSDs in parallel with L=1000 nm, W_i=250 and W_o=550 nm.

The transient behavior of the zero-bias AC impedance of the diodes measured after applying a voltage pulse can provide useful information about the trapping/detrapping processes taking place in the devices and their characteristic times. Fig. 5 shows the time evolution of the zero-bias AC impedance (@100 kHz) measured just after applying a voltage pulse to the narrow-channel SSDs of Fig. 2. Fig. 5(a) shows the results for pulses with a time width 10 ms and different amplitudes, V_0, in forward and reverse bias, while in Fig. 5(b) the amplitude is always 10 V and the width of the pulse, T_0, is modified. The steady-state value is also shown for comparison. Surface states are known to be charged when the current flows through the diodes, thus decreasing the current and producing a hysteretic behavior in the I-V curve, which shows long-lasting memory effects (even of some minutes duration) due to the large release time of such traps [8, 9]. The measurements of the AC impedance shown in Fig. 5 are coherent with this behavior.

The initial high values of the impedance (as compared with that at steady state) obtained in all cases for the shortest times are attributed electrons trapped in surface and bulk states due to the application of the pulse. For a given applied voltage, such increase is more pronounced in forward than in reverse bias. Once the pulse finishes, in case that the amplitude was not high enough to release electrons from the surface states during the application of the pulse, a slow decrease of the impedance due to the detrapping of electrons is observed.

In contrast, for pulse amplitudes high-enough to release electrons from surface states when the pulse width is 10 ms (see Fig. 3), an increase of the impedance at short times (some tenths of second) takes place, during which electrons are trapped again in those states, for then decreasing at a much longer time scale as in the previous case (detrapping of electrons). This interpretation is corroborated by the fact that when the measurement is done under illumination, the behavior at short times, attributed to trapping of electrons, does not change, while the detrapping taking place at longer times becomes accelerated by the presence of the light. It is interesting to highlight that the initial increase of the AC impedance becomes noticeable for smaller pulse amplitudes in reverse that in forward bias.

When the amplitude of the pulse is fixed to 10 V while its width is modified, Fig. 5(b), for the shorter pulses ($T_0 < 10$ ms) the behavior of the AC impedance is essentially the same since no previous release of surface electrons takes place. However, for longer pulses, the initial trapping of electrons at the surface states becomes visible. As the width of the pulse is enlarged, since more electrons were previously released, the increase in the AC impedance is more pronounced and persists for longer times.

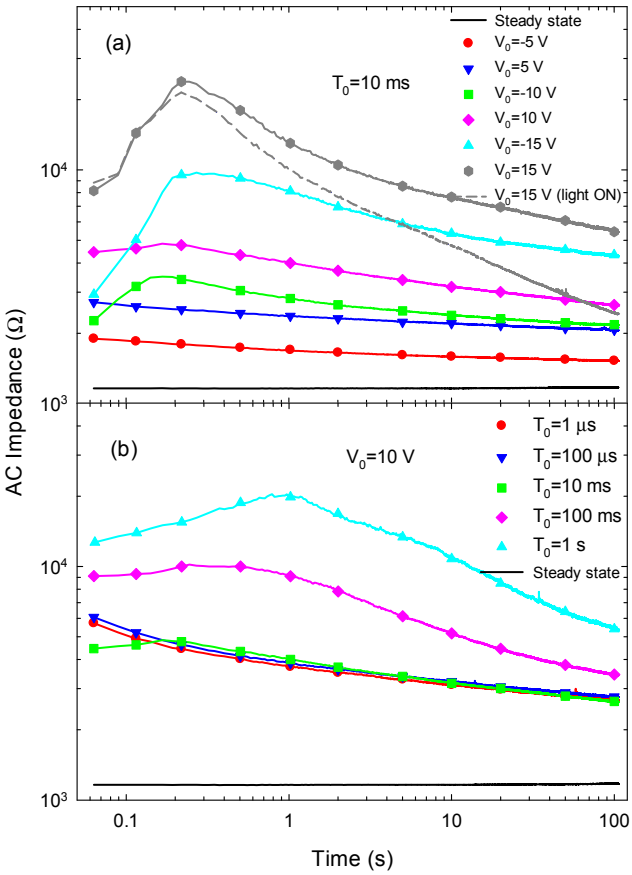

Fig. 5. Zero-bias AC impedance vs. time measured just after applying a voltage pulse to the SSDs of Fig. 2 of (a) time width T_0 of 10 ms and different amplitudes V_0 in forward and reverse bias, and (b) amplitude of 10 V and different time widths.

When similar measurements are performed in the wide rectangular and V-shape diodes of Fig. 4, the effects observed in the transient behavior of the AC impedance are much weaker (not shown), thus confirming the minor role played by the trapping/detrapping mechanisms at the surface states in wide-channel diodes. The initial increase of the impedance with respect to the steady-state value is much smaller than in the narrow SSDs and the effect related to the trapping of the electrons previously released is only observed for high forward bias in the V-shape SSDs.

IV. CONCLUSIONS

Trapping effects have been analyzed in GaN asymmetric nanodiodes by means of measurements of pulsed I-V curves and transient AC impedance. In the case of diodes with narrow channels, surface traps are found to play a major role. In particular, we observe an increase of the current for high applied voltages when measuring the I-V curve with increasing pulse duration. Such effect is attributed to the release of electrons from surface states at the sidewalls of the trenches defining the channel, which takes place in a relatively long time scale once a bias voltage is applied. We have identified detrapping times in the range of s to ms, decreasing for higher applied voltages. In the case of wide channels, the described effects are absent, and mainly the influence of bulk traps leading to a decrease in the current level is observed. The transient of the AC impedance measured just after the application of a voltage pulse provides information on how the detrapping processes take place. In the case of narrow channels, an increase of the impedance at the shortest times after the application of pulses of large amplitude has been found, which reflects an initial retrapping of electrons before they are released at longer times.

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