Influence of surface states in AlGaN/GaN nanodiodes analyzed by preconditioned transient current measurements

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***Abstract*—AlGaN/GaN nanodiodes consisting in an array of several nanochannels in parallel are potential candidates for detection in the THz range. The nanochannels are fabricated by etching two isolating trenches and show a current-voltage characteristic strongly influenced by the presence of surface charges at the channel sidewalls. Transient current effects have been characterized at room temperature and found to be associated to electron capture and emission mechanisms by surface traps. The conductance of these devices increases or decreases depending on the history of applied voltage, since it changes the occupation of the surface states and thus the depletion region present near the sidewalls. Moreover, the lateral field effect plays an important role, since, in addition to promoting trap charging or discharging, modifies the depletion region around the trenches, both of these processes determine the conductance of the channel. Additionally, the increase of the bias induces an effect analog to the drain induced barrier lowering of FETs. In this paper, the static behavior and transients of current of these nanochannels were characterized from the experimental point of view thanks to very short duration voltage pulses, while through Monte Carlo simulations were able to mimic the observed trends providing as well a physical interpretation that the charges trapped at the sidewalls of the trenches of the channels act as the gate in a FET.**

***Index Terms*—AlGaN/GaN devices, Diodes, Detectors, Terahertz, Trapping effects**

I. Introduction

NOWADAYS, the more established and traditional high-frequency technologies are reaching their limits. The efforts are focused on exploring new materials and topologies to increase the operation frequency. This is the case of RF and terahertz zero-bias detectors, specially at room temperature. Among the traditional devices used for RF/THz applications, GaAs Schottky barrier diodes (SBDs) and InGaAs, InAs high electron mobility transistors (HEMTs) are the most common technologies. A state of the art review in this field can be found in [1], [2]. Despite the lower electron mobility of GaN, it exhibits high saturation velocity and low permittivity, and its wide bandgap provides robustness and high thermal stability. These properties, jointly with the use AlGaN/GaN heterojunctions, which avoid the need of any doping, make GaN technology quite interesting for high frequency and high power applications.

In this work, we analyze a planar structure candidate to operate at terahertz frequencies, the self-switching diode (SSD), fabricated with just one lithography step [3], in our particular case on a AlGaN/GaN heterojunction . The etching of two L-shaped trenches defines an asymmetric channel and causes a non-linear I-V curve influenced by both a lateral field effect (the voltage applied to the anode propagates to the regions at the sides of the channel) and the depletion imposed by charges accumulated in the trenches' surfaces [4]. The topology of the SSD improves the coupling with free-space radiation and the high-frequency operation by reducing the parasitic capacitances. SSDs show significant detection capabilities in sub-terahertz and terahertz ranges at room temperature in materials such as GaAs [5], InGaAs [6], InAs [7], GaN [8], graphene [9], [10], ZnO [11], SOI [12], or poly(3-hexylthiophene) [13]. At cryogenic temperatures, the performance is even improved, since it has shown power detection up to 2.5 THz below 60 K in InGaAs [14]. On the other hand, the possible applications of the SSDs are not limited to the detection, but they may be also used as a room temperature THz source by means of the Gunn effect, as indicated by Monte Carlo (MC) simulations [15].

These devices show memory and low-frequency dispersion effects which influence their operation [16]. To turn into reality the applications of the SSDs, it is necessary to understand the behavior of the devices under different conditions. The fabrication process creates surface states at the sidewalls of

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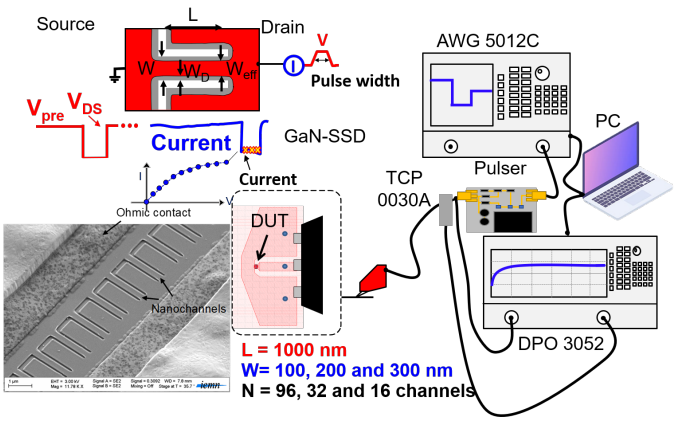

Fig. 1. Experimental setup used to measure the current transients. At the top left, the topology of the device and the implemented bias scheme are sketched. The bottom-left panel shows a SEM image of an array of SSDs.

the etched regions, which, by trapping electrons, bend the conduction band and shrink the effective width (W_{eff}) of the channels, thus reducing the current (see the sketch of the device in Fig. 1). Because of the nanometric dimensions of the channels, the high surface-to-volume ratio of SSDs leads to a behavior essentially governed by such surface states. Indeed, MC simulations predict a clear influence of the applied bias on the charge trapped at the sidewalls of the trenches of AlGaN/GaN SSDs, modifying the conductance of the channel by increasing the depletion region W_D around the trenches (and reducing its W_{eff}). The occupation of the traps and therefore their induced depletion region is both temperature and position dependent [17], [18].

Here, we give a more detailed and accurate interpretation to the work already presented in [19], where only preliminary characterization and conclusions about the impact of trapping effects on the current transients were provided. In this paper, the authors significantly extend the content of [19], not only at the measurement level (for example at higher voltages), but also providing an interpretation of these results on the device operation using numerical modeling by means of MC simulations that replicate the tendencies of the current-voltage curves. Thanks to the comparison between the model and measurements, we conclude that the charges trapped at the sidewalls of the trenches act like the gate of a FET.

II. Devices under test and setup

The SSDs under test were fabricated on an AlGaN/GaN heterojunction grown on a high resistivity SiC substrate. The epitaxial stack consists of 25 nm of $Al_{0.35}Ga_{0.65}N$ and 1.5 μm of GaN on a SiC substrate (thickness 575 μm), and passivated with 3 nm of SiN. The isolating trenches were defined using dry etching [20]. The devices under analysis, shown in Fig. 1, consist in multiple channels in parallel, all of them with the same length, L = 1 μm. Three devices, with different channel width W and number of channels, will be compared in this work to extract the information about the physical mechanisms governing the behavior of the SSDs: the first one with W = 100 nm and 96 channels, the second one with W = 200 nm and 32 channels and the last one of W = 300 nm and 16 channels. The width of the trenches is 50 nm and the distance between channels is 1 μm. The equilibrium depletion width around the trenches W_D^{eq}, estimated by extrapolating to zero value the plot of the conductance versus the channel width W, is found to be 35 nm [21], [22]. These devices show a breakdown voltage around 40-50 V depending on the geometry. Measurements were done on-wafer at room temperature and light conditions. The devices have coplanar waveguide pads contacted by Allstron RF Probes of 100 μm pitch. The setup, shown in Fig. 1, consists in a Tektronix AWG5012C arbitrary waveform generator to excite a home-made pulser, which builds up the pulsed bias at the device terminals, and a Tektronix DPO 3052 digital phosphor oscilloscope to measure the voltage and current provided by a Tektronix TCP0030A current probe. More details about the setup and the pulser can be found in [23], [24].

Regarding the simulation tool, although 3D simulations are the appropriate approach to model the real SSDs, here we make use of a properly calibrated 2D MC code. The accuracy of this approximation in different type of nano-devices, including SSDs, was demonstrated in previous works [25]–[27]. To account for the details of all the microscopic mechanisms present in the devices, the temporal step of the simulations is 1 fs, making impossible the simulation of the trapping dynamics, which would require huge simulation times. However, the static trapping effects have been modeled with an *ad hoc* self-consistent charge model (SCCM) able to reproduce the surface charge effects. The essence of this model is the adaptation of the value of the surface charge to the carrier density in the nearby region of the sidewalls [27]. In Fig. 2 we show a comparison between a typical $I-V$ curve of a SSD measured with a Keysight 2902A source measurement unit and the $I-V$ curve obtained with MC simulations. Although this model does not include the details of capture and release of electrons by traps, it is able to reproduce their global effect on the channel conductance, providing the satisfactory agreement observed in the figure.

III. Transients of current

The devices under test show hysteresis in the $I-V$ curves like in Fig. 2 and reported in previous works [16], [28]. Pulsed current-voltage measurements have also exhibited a time-dependent behavior [29]. Thus, the first task to understand the behavior of the SSD is to evidence the dynamics of the capture and emission processes, where capture or trapping is typically a fast process and emission or de-trapping a slow one [30]. Initially, we have analyzed the characteristic transient times when the device bias is stepped-up from V_{pre} = 0 V up to different V_{DS}, voltage at which we measure the current (see the inset of Fig. 3 for a better understanding of the test). The maximum measured voltage is 25 V. Fig. 3 (a) shows this transient process at different V_{DS} starting from 0 V for the device with W = 100 nm: the current reached its steady state after a time in the order of 1-2 s. According to the transients of current, the observed behavior is the capture of free carriers into the trap states of the boundaries. It can be

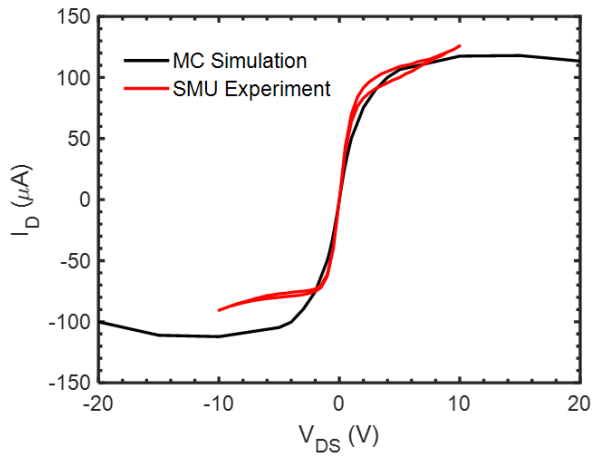

Fig. 2. Current-voltage characteristic measured in the device with W = 100 nm (red line) and predicted by means of MC simulations using the SCCM (black line).

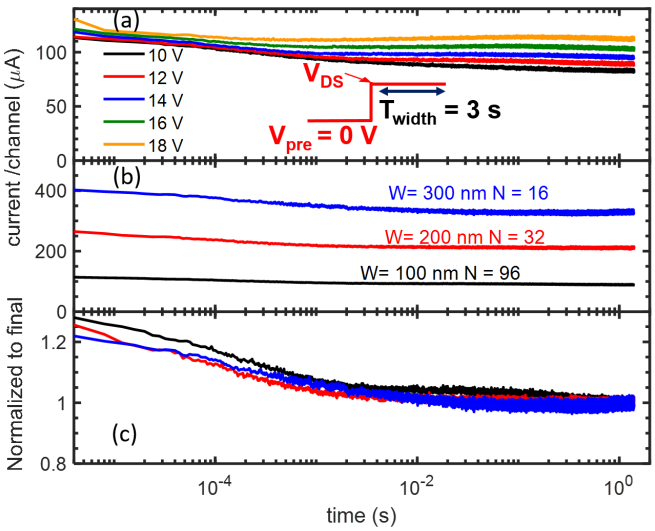

Fig. 3. Capture transients starting after 3 s of V_{pre} = 0 V (a) at V_{DS} = 10, 12, 14, 16 and 18 V of the device with W = 100 nm, (b) at V_{DS} = 12 V for devices with W = 100 nm, 200 nm and 300 nm and (c) normalized to the final value of the transient of current. The inset shows an sketch of the biasing in the experiment.

also observed some dependence on V_{DS}, which, in an analogy to the FET's channel length modulation, could be explained by a non-zero drain conductance in the saturation region of the output characteristics. To compare the behavior of the current in different SSD geometries, we have measured the transient for different channel widths [see Fig. 3 (b)]. It can be observed that the relative decrease of the current is similar in the three cases and the transients show similar dynamics [see Fig. 3 (c)].

In order to interpret these results, we analyze the profile of some quantities obtained from MC simulations. From the point of view of the simulations, the occupation of the energy states at the sidewalls of the trenches tends to increase when increasing the applied voltage, since in the *ad hoc* model (SCCM) the probability of trapping a carrier increases when there are more carriers in the vicinity of the boundary. In the simulations, to obtain significant differences, we will compare three biases more distant than the experimental ones, V_{DS} = 4, 10 and 20 V, one in the linear region, while the other two are in the (carrier velocity and thus current) saturation region. Since the applied voltage both accelerates electrons in the channel (becoming more energetic) and reaches the external sidewalls of the trenches, as V_{DS} increases, more electrons approach the internal sidewalls and may be captured by the surface states, thus providing higher values of surface charge [see Fig. 4 (a)]. In the case of the higher voltages, the spatial distribution of the surface charge is strongly non-homogeneous, being much higher in the boundary closer to the drain contact because highly energetic electrons are able to reach the sidewalls in that region. Accordingly, the perpendicular electric field exhibits the dependence with the position shown in Fig. 4 (b), tending to increase in the boundary closer to the drain contact at higher V_{DS}. In Fig. 4 (a) we also include in the right axis the values of the equivalent depletion induced around the trench by the surface charge,which is calculated as σ/N_{Db}, where σ is the surface charge obtained with the SCCM and N_{Db} the so called "virtual background doping", which reproduces the space charge effect originated by the positive charge at the AlGaN/GaN heterojunction, with a value of $N_{Db} = 10^{17}$ cm^{-3} in the simulations [18]. This parameter helps to understand the shape of the depletion region. These results can be linked directly with the previous experimental current transients, since the profiles obtained from the simulation correspond with the final situation of the SSD after the transients, where the trapped surface charges constrain the channel, specially close to the drain contact, thus reducing the current. During the transient, the increasing number of electrons approaching the channel sidewalls, particularly close to the drain contact, are captured by the initially empty traps. Thus, two different effects drive the evolution of the transients: (i) when a positive V_{DS} is applied, it originates a longitudinal electric field which drifts electrons along the channel, but V_{DS} also reaches the external sidewalls of the trenches, acting very similarly to a gate in a FET device, so that the current should also increase due to this lateral field-effect, and (ii) as the electrons in the channel approach the internal sidewalls, their trapping by the surface states is promoted. Therefore, the rise of the current produced by a higher bias is compensated by an enhanced trapping of carriers at the sidewalls. The comparison of the transient for V_{DS}=12 V measured for SSDs with different channel widths W [see Fig. 3 (b)] reveals that the absolute decrease of the current is smaller in the case of the narrower diode due to the lower amount of electrons available to fill the surface states, while the decrease relative to the initial value is similar for the three analyzed values of W. In previous works [20] two kinds of traps, associated to bulk and surface states (the latter distributed in a broad energy range), were identified in these diodes. At low temperatures, the preliminary values found for the activation's energies were in the order of tens of meV both for the discrete bulk trap state and the surface states. With MC simulations we have estimated the surface density of occupied trap states to be in the 10^{11}-10^{12} cm^{-2} range.

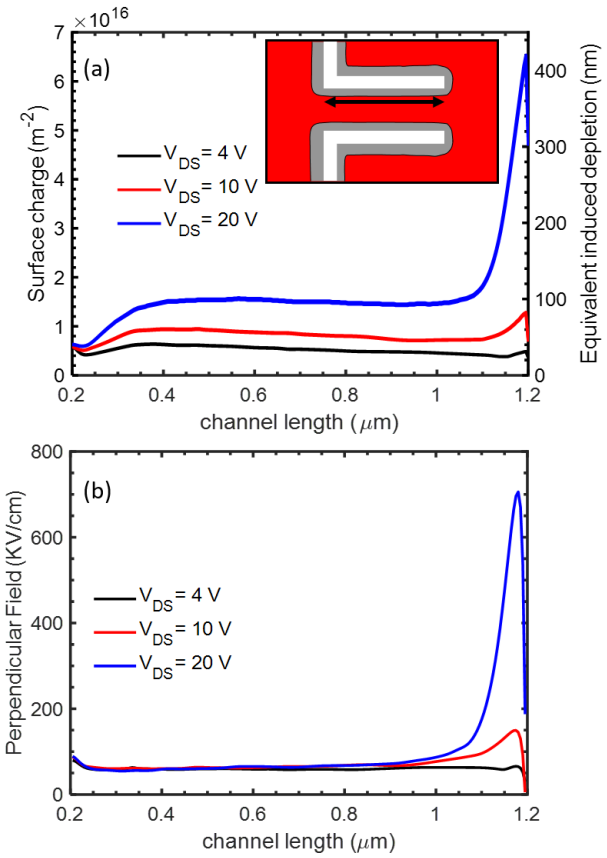

Fig. 4. Profiles of (a) surface charge (left axis; equivalent depletion width normal to the boundary in the right axis) along the longitudinal sidewall of the channel, as signaled in the inset, and (b) electric field perpendicular to the channel along the same line, for three values of V_{DS}, 4, 10 and 20 V.

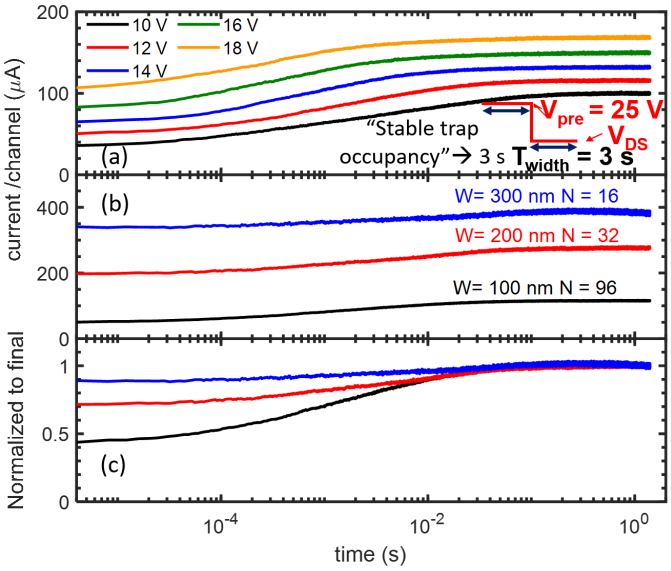

Fig. 5. Emission transients after 3 s of V_{pre} = 25 V (a) at V_{DS} = 10, 12, 14, 16 and 18 V of the device with W = 100 nm, (b) at V_{DS} = 12 V for devices with W = 100 nm, 200 nm and 300 nm and (c) normalized to the final value of the transient of current. The inset shows an sketch of the biasing in the experiment.

As a second test, the transient of current is studied immediately after a pulse V_{pre} different from 0 V, applying another V_{DS} lower than V_{pre} (see the inset of Fig. 5 as a graphic explanation of the test). Fig. 5(a) shows the transients of current measured under different V_{DS} after a long preconditioning pulse of V_{pre} = 25 V is applied (2 s width, i.e., the time when the capture was found to be stable in the previous test). It can be observed that the current increases and the steady state is reached in the order of some ms to s, taking longer time for smaller V_{DS}. This behavior originates from the de-trapping of electrons from the surface states, which leads to an increase of carrier concentration and effective channel width W_{eff}. In this situation, the de-trapping is activated not only by thermal emission, but also assisted by the test biasing conditions V_{DS}, for which the perpendicular electric field attracting electrons to the sidewalls is smaller than under the preconditioning voltage. As expected, the steady state of these emission transients is similar to that of the capture transients at the same voltage, because it is obtained as a balance between the de-trapping produced by the emission from the surface states, which has the consequence of increasing W_{eff}, and the trapping caused by the mechanisms studied in the simulations, which tends to reduce the W_{eff}. This situation can be defined as a stable trap occupancy state. The mechanism is very similar to that described by the (Shockley–Read–Hall) SRH statistics, since the trapping dynamics are described by the difference between the capture and emission rates of free electrons [23]. In our case, the electrons are not forced into the buffer but into the sidewalls of the trenches, but the trapping dynamics can be described by the difference between the capture and emission rates of free electrons under different biasing conditions, reflected as a change in the measured current. Again, to give more experimental support to this interpretation, we should compare the narrower device, in which the walls are closer and the effects more evident, with two wider devices in which the effect of the surfaces is softened [see Fig. 5 (b)]. It can be observed that, in contrast with the trapping transient, now the absolute increase of the current is similar in the three cases, while the relative one is less pronounced in the wider devices because the depletion around the trenches is smaller as compared to W_{eff} and the transients show similar dynamics [see Fig. 5 (c)].

IV. Current-Voltage Characteristics

Once the timescales of capture and emission processes were studied and a physical interpretation qualitatively inferred from the results of simulations, we can extract more conclusions about the physics of the device from the $I-V$ curves obtained under different preconditioning situations and measure times. The preconditioning voltage V_{pre} will always correspond to a trapping (positive) bias applied during 3 s. The first set of measurements, shown in Fig. 6 (a) and (b), correspond to a very fast current measurement, performed within the first 20 μs after the application of V_{DS}, when the de-trapping has not yet started, while the second set of I-V curves, Fig. 8, is obtained waiting 3 s after the application of V_{DS}, allowing for the completion of the de-trapping process.

Regarding the first set of curves, where V_{pre} varies from 25 to 1 V, it shows that in the SSD with W = 100 nm it is possible to completely close the channel by applying a positive enough V_{pre} [see Fig. 6 (a)]. Indeed, the device behaves as a FET in which the potential associated to the charge trapped at the surface states acts as the gate potential, which in the case of V_{pre} = 25 V is able to close the channel. In this situation, the surface charge profile is similar to the high voltage one shown in Fig. 4 (a), where the attraction of carriers to the boundary of the trenches induces the trapping, constraining the channel. Therefore, the electrons without enough energy are not able to cross the potential barrier created by the surface charge. When V_{pre} decreases, the attraction of free carriers is not so intense and the trapping effect is smaller. In this situation, the surface charge profile is more similar to the low potential profile of Fig. 4 (a), where the barrier in the channel is lower, it is not so constrained and the carriers have enough energy to reach the drain contact. The result of this experiment is a set of curves similar to the output characteristics of a FET, where the surface charge at the trenches act as the gate voltage controlling the current. Note that the time elapsed since the application of V_{DS} until the current is measured is so short that V_{DS} is not able to significantly change the surface charge at the sidewalls of the trenches, but just to move electrons along the channel. Thus, the current increases with V_{DS}, reaching a different level depending on V_{pre}, which determines electron concentration in the channel. An interesting result obtained in these measurements is found when V_{pre} is high enough (>16 V) to pinch-off the device. As observed, as V_{DS} increases, even if the SSD is initially pinched-off, at a high enough value (lower for smaller V_{pre}), the device starts conducting. This effect is analog to the drain induced barrier lowering (DIBL) of a FET [31], where V_{DS} is reducing the barrier imposed by the depletion region around the trenches allowing the conduction of energetic enough carriers. In addition, this depletion region is wider in the drain side of the trench, also in analogy with a transistor. Again, the comparison of different geometries allows to extract more conclusions about the characteristics of the device. In the narrowest device, it is possible to close the channel by increasing the surface charge in the sidewalls applying V_{pre} = 25 V. However, the wider structures do not show this pinch-off [see Fig. 6 (b)]. The device is not pinched-off because the depletion induced by the surfaces is less preeminent with respect to the total width of the channel. For the same reason, the difference in the level of current between two curves obtained with different V_{pre} in the SSDs with W = 200 and 300 nm (results not shown) is less pronounced than in the case of the SSD with W = 100 nm. Actually, this effect on the resistance of the channel is gradually less evident as W increases.

To confirm the previous interpretation that the trapped charges at the sidewalls of the trenches resembles the role of the gate in a FET we have run MC simulations in order to replicate the experimental trends. Due to the nature of the characteristic times of the traps and the time step of simulations (fs) the evolution in time is unapproachable inside our simulator. However, we can assume that the final state of the occupation of the surface states obtained after the capture

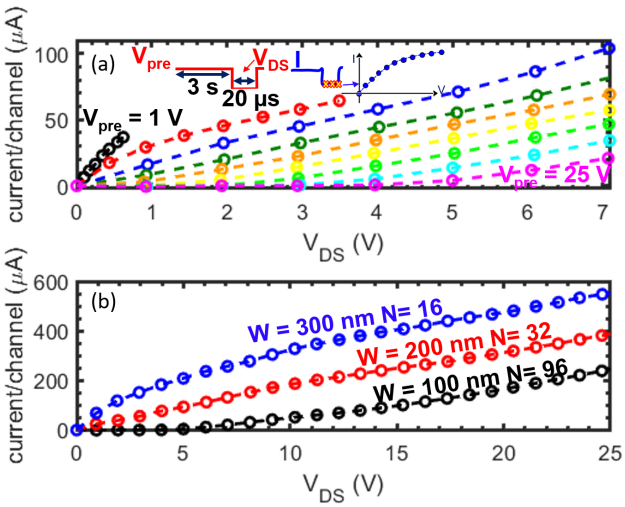

Fig. 6. (a) Measured $I-V$ curves in the SSD with W = 100 nm and N = 96 subjected to a 2-s pre-pulse of different amplitude V_{pre} from 25 V to 1 V (step 3 V) and (b) comparison of the I-V curves measured with a pre-pulse of V_{pre} = 25 V in the SSDs of W = 100 nm and N = 96 (black), W = 200 nm and N = 32 (red) and W = 300 nm and N = 16 (blue). The values of V_{DS} are stepped from 1 V to the corresponding V_{pre} of the experiment. The points correspond to the mean value of the current measured during the first 20 μs after the application of V_{DS}. The inset shows an schematic of the biasing in the experiment.

(after the 3 s of the preconditioning voltage V_{pre}) is well reproduced by the SCCM approach. Afterwards, we freeze this profile of the surface charges obtained with V_{pre}^{MC} and run the MC core for the rest of the other points of the I-V curve. In this framework the static simulation using the frozen profile corresponds with the measurements of the current measured during the first 20 μs after the application of V_{DS} of Fig. 6 (a). It is to say, we consider that the charges trapped at the sidewalls obtained within the SSCM had not enough time to be released from the walls after being filled and they are still constraining the conductive channel by electrostatic repulsion. We have carried out simulations using three values of the bias V_{pre}^{MC} = 20, 10 and 4 V (see Fig. 7) whose final surface charge profiles were already shown in Fig. 4 (a). The depletion that partially closes the channel is smaller the lower the value of V_{pre}^{MC} is. We note that for the two highest V_{pre}^{MC} the channel is pinched-off suggesting again that the effect of the charges in the sidewalls is essentially the field effect of a gate in a transistor.

The set of I-V curves obtained measuring the current after a longer time, allowing for the de-trapping transient to conclude, do not show any pinch-off, according to the results shown in Fig. 8, for V_{pre}=25 V. As expected, under such conditions, the measured current is that corresponding to the surface charge profile obtained for the applied V_{DS} irrespectively of the initial V_{pre}. This final state of the experiment corresponds with the final result of the simulation once the transient finishes. When the depletion region does not constrain the channel completely, the side regions out of the channel connected to the drain terminal act as a lateral gate electrode biased with a V_{DS} potential. However, the lateral field effect is quite weak due to the large width of the trenches. Additionally, it is screened

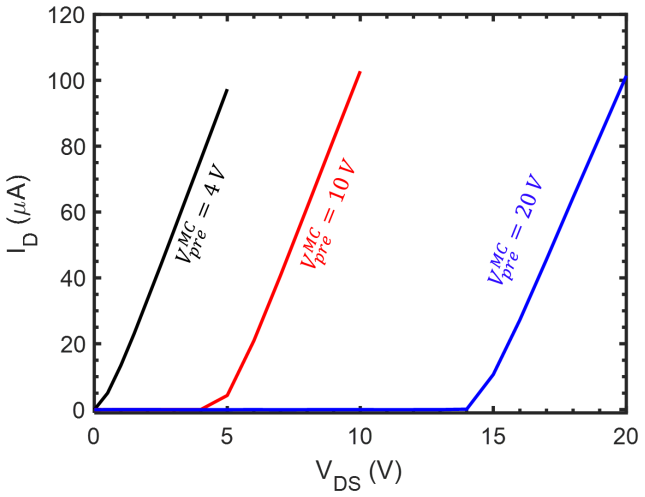

Fig. 7. I-V curves obtained by MC simulations in the SSD of W = 100 nm and N = 96 freezing the surface charge profiles of Fig. 4 (b) at V_{pre}^{MC} = 4 (black), 10 (red) and 20 V (blue).

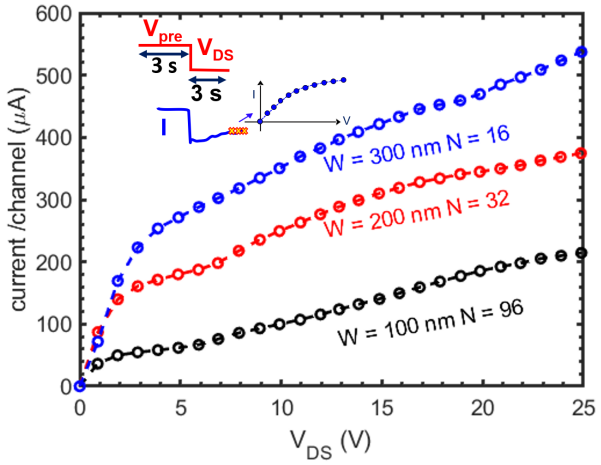

Fig. 8. Comparative of the $I - V$ curves measured 3 s after the application of V_{DS} in the SSDs with W = 100 nm and N = 96 (black), W = 200 nm and N = 32 (red) and W = 300 nm and N = 16 (blue), previously subjected to a 3 s pre-pulse V_{pre} = 25 V. The inset shows an schematic of the biasing in the experiment.

by the surface charges at both sidewalls of the trenches, like an un-gated transistor, i.e., a channel of approximately constant width evidencing ohmic conduction followed by the limitation of the carrier velocity saturation. Moreover, the saturation mechanism can be also understood with these results. The narrowest device tends to saturation for lower V_{DS} than the other two devices. The surface charge profile in the narrowest device shown in Fig. 4 (a) helps understanding this behavior. The saturation is induced by the surface charges that constrain the channel as V_{DS} increases. A higher V_{DS} is necessary to reach the knee in the I-V curve as the channel is wider, since the surface charges do not constrain the channel so much, as discussed before.

V. Conclusion

This work confirms that the transients of current observed in SSDs can be related to the increment of electrons in the channel that approach the sidewalls of the trenches when a bias is applied to the device, becoming trapped at the surface states, and being more evident at higher voltages. In addition, MC simulations reinforce this physical interpretation providing similar trends in the current-voltage curves. The emission is activated when the carriers in the channel decrease by reducing the applied voltage, increasing the available free states in the channel. The final state is an equilibrium condition between both processes. The DC behavior of the device is influenced by the depletion induced by the charges trapped at the sidewalls of the trenches, which are able to completely close the channel, showing some effects like DIBL. This device can be understood like a FET, where the charge at the trenches acts like the gates in the transistor.

References

[1] E. Javadi, D. B. But, K. Ikamas, J. Zdanevicius, W. Knap, and A. Lisauskas, "Sensitivity of field-effect transistor-based terahertz detectors," *Sensors*, vol. 21, p. 2909, apr. 2021.

[2] F. Aniel, G. Auton, D. Cumming, M. Feiginov, S. Gebert, T. González, C. Li, A. Lisauskas, H. Marinchio, J. Mateos *et al.*, "Terahertz electronic devices," in *Springer Handbook of Semiconductor Devices*. Springer, 2022, pp. 807–849.

[3] A. M. Song, M. Missous, P. Omling, A. R. Peaker, L. Samuelson, and W. Seifert, "Unidirectional electron flow in a nanometerscale semiconductor channel: A self-switching device," *Appl. Phys. Lett.*, vol. 94, no. 9, p. 1881, sep. 2003.

[4] J. Mateos, B. G. Vasallo, D. Pardo, and T. González, "Operation and high-frequency performance of nanoscale unipolar rectifying diodes," *Appl. Phys. Lett.*, vol. 86, no. 21, p. 212103, may 2005.

[5] C. Balocco, S. R. Kasjoo, X. F. Lu, L. Q. Zhang, Y. Alimi, S. Winnerl, and A. M. Song, "Room-temperature operation of a unipolar nanodiode at terahertz frequencies," *Appl. Phys. Lett.*, vol. 98, no. 22, pp. 223 501,1–4, May 2011.

[6] C. Balocco, A. M. Song, M. Åberg, A. Forchel, T. González, J. Mateos, I. Maximov, M. Missous, A. A. Rezazadeh, J. Saijets, L. Samuelson, D. Wallin, K. Williams, L. Worschech, and H. Q. Xu, "Microwave detection at 110 GHz by nanowires with broken symmetry," *Nano Lett.*, vol. 5, no. 7, pp. 1423–1427, 2005.

[7] A. Westlund and P. Sangaré and G. Ducournau and P-Å. Nilsson and C. Gaquière and L. Desplanque and X. Wallart and J. Grahn, "Terahertz detection in zero-bias InAs self-switching diodes at room temperature," *Appl. Phys. Lett.*, vol. 103, no. 13, pp. 133 504,1–4, 2013.

[8] P. Sangaré, G. Ducournau, B. Grimbert, V. Brandi, M. Faucher, C. Gaquière, A. Íñiguez-de-la Torre, I. Íñiguez-de-la Torre, J. F. Millithaler, J. Mateos, and T. González, "Experimental demonstration of direct terahertz detection at room-temperature in AlGaN/GaN asymmetric nanochannels," *J. Appl. Phys.*, vol. 113, no. 3, pp. 034 305,1–6, 2013.

[9] A. Westlund and M. Winters and I. G. Ivanov and J. Hassan and P.-A. Nilsson and E. Janzen and N. Rorsman and J. Grahn, "Graphene self-switching diodes as zero-bias microwave detectors," *Appl. Phys. Lett.*, vol. 106, no. 9, pp. 093 116,1–4, 2015.

[10] M. Winters, M. Thorsell, W. Strupinski, and N. Rorsman, "High frequency electromagnetic detection by nonlinear conduction modulation in graphene nanowire diodes," *Appl. Phys. Lett.*, vol. 107, no. 14, pp. 143 508,1–5, 2015.

[11] M. Y. Irshaid, C. Balocco, Y. Luo, P. Bao, C. Brox-Nilsen, and A. M. Song, "Zinc-oxide-based planar nanodiodes operating at 50 MHz," *Appl. Phys. Lett.*, vol. 99, no. 9, pp. 092 101,1–3, 2011.

[12] G. Farhi, E. Saracco, J. Beerens, D. Morris, S. Charlebois, and J.-P. Raskin, "Electrical characteristics and simulations of self-switching-diodes in SOI technology," *Solid-State Electron.*, vol. 51, no. 9, pp. 1245–1249, Aug. 2007.

[13] J. Kettle, S. Whitelegg, A. M. Song, M. B. Madec, S. Yeates, M. L. Turner, L. Kotacka, and V. Kolarik, "Fabrication of poly(3-hexylthiophene) self-switching diodes using thermal nanoimprint lithography and argon milling," *J. Vac. Sci. Technol. B:Nanotechnol. Microelectron.*, vol. 27, no. 6, pp. 2801–2804, Dec. 2009.

[14] C. Balocco, M. Halsall, N. Q. Vinh, and A. M. Song, "THz operation of asymmetric-nanochannel devices," *J. Phys. Condens. Matter*, vol. 20, no. 38, p. 384203, Aug. 2008.

[15] S. García-Sánchez, M. Abou Daher, M. Lesecq, L. Huo, R. Lingaparthi, D. Nethaji, K. Radhakrishnan, I. Íñiguez-de-la Torre, B. G. Vasallo, S. Pérez, T. González, and J. Mateos, "On the practical limitations for the generation of Gunn oscillations in highly doped GaN diodes," *IEEE Trans. Electron Devices*, vol. 70, no. 7, pp. 3447 – 3453, May 2023.

[16] H. Sánchez-Martín, E. Pérez-Martín, G. Paz-Martínez, J. Mateos, T. González, and I. Íñiguez-de-la-Torre, "Low temperature memory effects in AlGaN/GaN nanochannels," *Appl. Phys. Lett.*, vol. 123, no. 10, p. 103505, Sep. 2023.

[17] E. Pérez-Martín, I. Iñiguez-de-la-Torre, C. Gaquière, T. González, and J. Mateos, "Monte Carlo analysis of the influence of surface charges on GaN asymmetric nanochannels: Bias and temperature dependence," *J. Appl. Phys.*, vol. 130, no. 10, p. 104501, Sep. 2021.

[18] A. Íñiguez-de-la-Torre, I. Íñiguez-de-la-Torre, J. Mateos, T. González, P. Sangarè, M. Faucher, B. Grimbert, V. Brandli, G. Ducournau, and C. Gaquière, "Searching for THz Gunn oscillations in GaN planar nanodiodes," *J. Appl. Phys.*, vol. 111, no. 11, p. 113705, Jun. 2012.

[19] H. Sánchez-Martín, I. Íñiguez-de-la-Torre, J. Mateos, S. Pérez, T. González, L. C. Nunes, and J. Pedro, "Characterization of trap-related transient-current effects in AlGaN/GaN nanochannels," in *Proc. IEEE 2023 International Workshop on Integrated Nonlinear Microwave and Millimetre-Wave Circuits (INMMIC)*, Nov. 2023, pp. 1–4.

[20] E. Pérez-Martín, T. González, D. Vaquero, H. Sánchez-Martín, C. Gaquière, V. J. Raposo, J. Mateos, and I. Iñiguez-de-la-Torre, "Trap-related frequency dispersion of zero-bias microwave responsivity at low temperature in GaN-based self-switching diodes," *Nanotechnology*, vol. 31, no. 40, p. 405204, Jul. 2020.

[21] J. S. Galloo, E. Pichonat, Y. Roelens, S. Bollaert, X. Wallart, A. Cappy, J. Mateos, and T. González, "Transition from ballistic to ohmic transport in T-Branch junctions at room temperature in GaInAs/AlInAs heterostructures," in *Proc. IEEE IRPM*, Jun. 2004, pp. 378–381.

[22] H. Sánchez-Martín, S. Sánchez-Martín, I. Íñiguez-de-la-Torre, S. Pérez, J. A. Novoa, G. Ducournau, B. Grimbert, C. Gaquière, T. González, and J. Mateos, "GaN nanodiode arrays with improved design for zero-bias sub-THz detection." *Semicond. Sci. Technol.*, vol. 3, no. 9, p. 095016, Aug. 2018.

[23] C. F. Gonçalves, L. C. Nunes, P. M. Cabral, and J. C. Pedro, "Pulsed I/V and S-parameters measurement system for isodynamic characterization of power GaN HEMT transistors," *Int. J. RF Microw. Comput. Aided Eng.*, vol. 28, no. 8, p. 21515, Oct. 2018.

[24] J. L. Gomes, L. C. Nunes, C. F. Gonçalves, and J. C. Pedro, "An accurate characterization of capture time constants in GaN HEMTs," *IEEE Trans. Microw. Theory Techn.*, vol. 67, no. 7, pp. 2465 – 2474, Jul. 2019.

[25] J. Millithaler, I. Íñiguez-de-la-Torre, J. Mateos, T. González, and M. Margala, "Optimization of ballistic deflection transistors by monte carlo simulations," in *J. Phys.: Conf. Ser.*, vol. 647, Jul. 2015, p. 012066.

[26] I. Íñiguez-de-la-Torre, J. Mateos, T. González, D. Pardo, J. S. Galloo, S. Bollaert, Y. Roelens, and A. Cappy, "Influence of the surface charge on the operation of ballistic t-branch junctions: a self-consistent model for monte carlo simulations," *Semicond. Sci. and Technol.*, vol. 22, no. 6, pp. 663–670, May 2007.

[27] I. Iñiguez-de-la-Torre, T. González, D. Pardo, and J. Mateos, "Hysteresis phenomena in nanoscale rectifying diodes: A Monte Carlo interpretation in terms of surface effects," *Appl. Phys. Lett.*, vol. 91, no. 6, p. 063504, 2007.

[28] E. Pérez-Martín, H. Sánchez-Martín, T. González, J. Mateos, and I.Iñiguez-de-la-Torre, "Trap-assisted enhancement of the responsivity in asymmetric planar GaN-based nanodiodes at low temperature," *Nanotechnology*, vol. 34, no. 32, p. 325201, May 2023.

[29] H. Sánchez-Martín, O. García-Pérez, I. Íñiguez-de-la-Torre, S. Pérez, J. Mateos, T. González, and C. Gaquière, "Geometry and bias dependence of trapping effects in planar gan nanodiodes," in *2017 Spanish Conference on Electron Devices (CDE)*, 2017, pp. 1–4.

[30] J. L. Gomes, L. C. Nunes, N. A. Sobolev, and J. C. Pedro, "Memristive properties of GaN HEMTs containing deep-level traps," *Phys. Status Sol B*, vol. 5, no. 256, p. 1800387, 2019.

[31] M. J. Uren, K. J. Nash, R. S. Balmer, T. Martin, E. Morvan, N. Caillas, S. L. Delage, D. Ducatteau, B. Grimbert, and J. C. D. Jaeger, "Punch-through in short-channel AlGaN/GaN HFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 2, pp. 395 – 398, 2006.