Avoiding Avalanche Breakdown in Planar GaN Gunn Diodes by Means of a Substrate Contact

S. García-Sánchez,[*,†] S. Pérez,[†] I. Íñiguez-de-la-Torre,[†] B. García-Vasallo,[†] L. Huo,[‡] R. Lingaparthi,[¶] D. Nethaji,[¶] K. Radhakrishnan,[‡,¶,§] M. Abou Daher,[‖] M. Lesecq,[‖] T. González,[†] and J. Mateos[†]

†*Department of Applied Physics and USAL-NANOLAB, Universidad de Salamanca, Salamanca 37008, Spain.*

‡*UMI3288 CINTRA, (CNRS/NTU/THALES), Nanyang Technological University, Singapore.*

¶*Temasek Laboratories, Nanyang Technological University, Singapore.*

§*Centre for Micro/Nano-electronics (CMNE), Nanyang Technological University, Singapore.*

‖*Institut d'Electronique de Microélectronique et de Nanotechnologie, Lille, France.*

E-mail: sergio_gs@usal.es

Abstract

Impact ionization originated by the buffer leakage current, together with high electric fields (>3 MV/cm) at the anode corner of the isolating trenches, has been identified as the failure mechanism of shaped planar GaN Gunn diodes when biased above 20 V, so that no evidence of Gunn oscillations in fabricated devices has been observed yet. In order to avoid the avalanche, we propose the addition of a Schottky substrate terminal, which, by means of Monte Carlo simulations, has been confirmed to be able to suppress such not-desired leakage current when applying a negative substrate bias. When the

substrate bias is positive, impact ionization is also reduced due to the lower electric field at the hotspot, but a vertical cathode-substrate current degrades the device operation. In order to avoid such current, we propose the use a MIS configuration for the substrate contact, which is the optimal solution.

Introduction

In the last years, the development of GaN technology has made significant advances for its broad use in high-power, high-frequency and high temperature applications[1,2] due to its wide bandgap (3.4 eV), high electron saturation velocity ($\sim 2.5\times10^{7}$ cm/s) and high breakdown electric field (<3.3 MV/cm). GaN-based technologies, by providing a high-power radio frequency (RF) input at the first stages of Schottky-barrier-diode-based frequency multipliers (at frequencies below 50 GHz), could also become good candidates for improving the performance of RF sources in the millimeter and terahertz (THz) wavelengths and allow the widespread use of THz applications, for example, in satellite communications, body scanners, automotive, radar, medical and military applications.[3–7] Indeed, high power oscillators based on GaN HEMTs in the K band are presently being used as fundamental source for THz sources.[8] Another approach to increase the output power of such ultra high frequency RF sources is to generate high-power high-frequency Gunn oscillations.[9] Such fundamental oscillators with frequency above 200 GHz[10] and output power above the mW level, would allow reducing the frequency multiplication factor of the multiplier chain also avoiding complex power combining designs, thus much increasing its efficiency and THz output power while decreasing its complexity and cost.

Simulations show that GaN Gunn diodes are able to generate RF output power above 300 GHz based on the negative differential resistance (NDR) of GaN.[10–14] However, up to now only indirect evidences of such oscillations have been observed experimentally in vertical GaN structures.[15,16] Another approach for generating Gunn oscillations, avoiding the appearance of large electric fields at the ohmic contact edges (leading to electromigration and device failure),[17,18] is the use of geometrically-shaped planar Gunn diodes (GS-PGDs) inspired on the self-switching diode concept.[19,20] Indeed, such geometry allows to concentrate the electric field at the channel region while also reducing the DC current level and thus self-heating problems. This approach was initially tested by our group fabricating devices based on AlGaN/GaN heterojunctions, but in spite of large technological efforts and many tests, no evidence of Gunn oscillations was observed. In this contribution we present results of GS-PGDs fabricated using a highly doped GaN active layer[21] where the electric field is more effectively localized and Gunn effect is easier to obtain in comparison with an AlGaN/GaN-based diodes. Indeed, Monte Carlo (MC) simulations show that by increasing the doping of the active layer, the Debye length is much reduced, so that the formation of the Gunn domain is promoted by the presence of a higher electric field, which appears very fast in the close vicinity of a space charge outbreak.

However, after manufacturing different runs of devices based on different epilayer configurations (with varying active layer thickness and doping levels in the 10^{18}-10^{19} cm^{-3} range), all of them show a premature breakdown for biases below any Gunn oscillation was observed.[22] MC simulations show that the failure mechanism can be attributed to an impact ionization (II) avalanche process initiated by the leakage current of electrons flowing through the buffer (which is intensified when Gunn domains start to form). This happens due to the huge electric fields appearing at the anode end of the channel, at the corner of the etched regions.[22] In this work we propose an improved design of the GaN GS-PGDs consisting in the addition of a bottom contact to the GaN buffer, which allows to suppress the II mechanisms by reducing the buffer leakage current and the electric field hotspot and thus avoid the avalanche process and the consequent device failure. This novel device concept has not been applied previously to the fabrication of planar Gunn diodes and here we provide its theoretical background, which will be applied in a forthcoming fabrication run.

Experimental Section

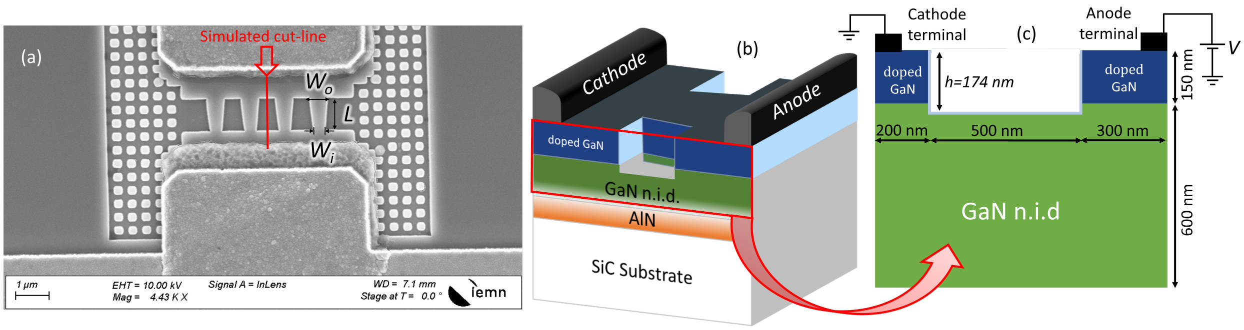

Figure 1: (a) SEM picture of the fabricated diode (with the meaning of the geometrical parameters L, W_i and W_o of the channels indicated and a cut-line indicating the simulated zone), whose 3D sketch is shown in (b). (c) Front-view of a longitudinal cut at the etched sides of a channel with an isolation depth of h=174 nm.

Figure 1(a) shows a scanning electron microscope (SEM) image of a diode fabricated on a 150 nm thick active layer doped at N_D=6.6×10^{18} cm^{-3} with a geometry with length L=1 μm, widths at the entrance and exit W_i=300 nm and W_o=450 nm, respectively and N=4 parallel channels, which was defined by etching ∼200 nm deep trenches. The three-dimensional (3D)

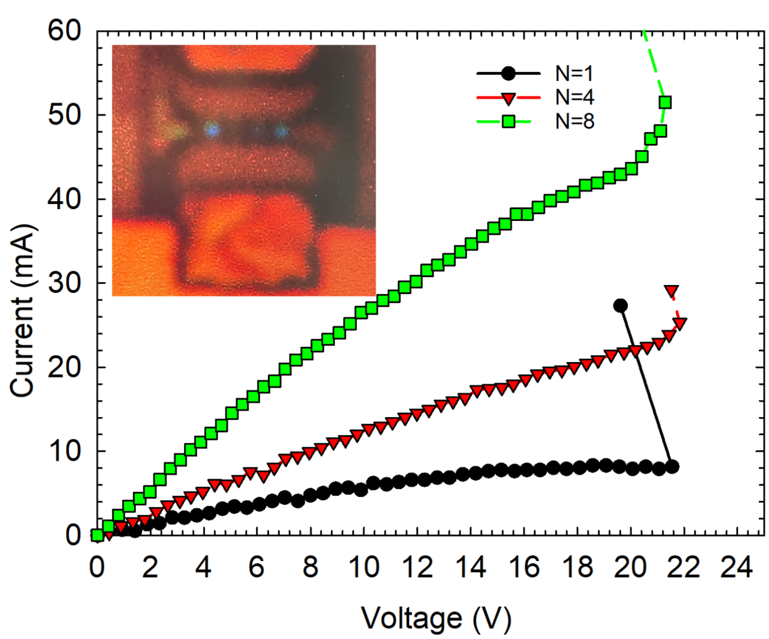

Figure 2: I-V curves obtained at T=8 K using 300 ns-wide pulses (1% duty cycle) for arrays of N=1, 4 and 8 diodes with L=1 μm, input width W_i=350 nm and output width W_o=450 nm. The inset shows the blue light emission observed before the device breakdown.

sketch of a GS-PGD is summarized in Figure 1(b). The pulsed I-V curves shown in Figure 2, for devices with the same geometry and N=1, 4 and 8, were obtained at T=8 K using using 300 ns wide-pulses (with 1% duty cycle) in order to avoid as much as possible the heating of the samples. Indeed, it is clearly observed that the breakdown voltage, V_B, takes place about 22-24 V regardless of the number of parallel channels, so that self-heating is not at the origin of the failure (even the device with larger dissipated power has a slightly higher value of V_B). The assumption that the failure mechanism is related to a high field process is supported by the fact that V_B decreases for channels with shorter length, even if the current level (and therefore the dissipated power and the associated self-heating) is similar, and further confirmed by the fact that room temperature measurements provide almost the same current values and breakdown voltages than those observed at 8 K.[22] Finally, blue light emission appears for voltages slightly below V_B, inset of Figure 2, probably coming from the recombination processes subsequent to the generation of electron-hole pairs by II. The interaction of hot electrons with defect states in the C-doped GaN buffer could also be at the origin of this luminescence,[23] anyway revealing a significant injection of high-energy electrons into the GaN buffer, which can be related to the appearance of a non-negligible leakage current. This phenomenon precedes the catastrophic breakdown of the devices before the onset of Gunn oscillations. Another evidence of the non-thermal related origin of the device failure is obtained from the measurements performed with a high-definition thermographic infrared camera, which show a maximum temperature increase of less than 50 K for the devices with N=1. All those evidences lead us to attribute the breakdown to an II-initiated avalanche mechanism.[22]

Monte Carlo Simulations and Device Details

A semiclassical ensemble MC self-consistently coupled with a two-dimensional (2D) solution of the Poisson's equation is employed for the simulation of the GS-PGDs.[10,22] The electron transport is described by a three-nonparabolic, spherical valley model (Γ_1, U and Γ_3 valleys). Scattering with ionized impurities and optical and acoustic phonons, together with piezoelectric, alloy and intervalley scattering mechanisms are included in the simulator. Fermi-Dirac statistics, using a self-consistent calculation of the Fermi level, are imposed for the occupancy of the energy states by means of a rejection technique after every scattering mechanism. Poisson equation is updated every 0.2 fs with a meshing in the range 2-5 nm in order to adequately reproduce the electric field variations, in time and space, with a total simulation time of 0.4 ns (2 million iterations). More details about the parameters used in the simulator can be found in Ref.[10] The influence of the surface charge at the semiconductor dielectric interfaces is incorporated by using the self-consistent surface-charge model described in Ref.[24] II mechanism has been incorporated through the Keldysh approach[25,26] as in Ref.,[22] using the following parameters: ε_{th}=3.5 eV, $S=10^{13}\,\mathrm{s}^{-1}$ and k=4; values which provide a good agreement with the results of Ref.[26] for the GaN II coefficient.

We will show the results of front-view 2D MC simulations, which are able to account for the mechanisms leading to the avalanche process, since they correctly describe the electric field hotspot at the anode side corner of the trenches and the leakage current through the buffer.[22] Our simulated device has a 150 nm thick doped GaN active layer ($N_D=5\times10^{18}\,\mathrm{cm}^{-3}$) on top of a 600 nm thick undoped GaN buffer (both considered to be trap-free) and a 174 nm deep etched region filled with air (dielectric permittivity ε_r=1 is considered), corresponding to the top region of the fabricated epilayer (see Figure 1(c)). The length of the simulated trench is L=500 nm, and the size of the access regions has been shrinked with respect to the fabricated devices in order to reduce the computation time.

In Ref.[22] we showed that the amount of II mechanisms observed in the 2D simulations is not sufficient for the onset of the avalanche process for the voltages at which the experimental failure is experienced. The comparison of the MC simulations with those of the experiments indicates that the value of the intervalley separation ε_{1-2} may be lower than the one typically used (0.9 eV instead of 2.2 eV, as indicated by recent experiments[27,28]). In both cases, the amount of II mechanisms at the anode corner of the trenches in steady state conditions is quite low, but the threshold voltage of the Gunn Oscillations obtained with simulations made using ε_{1-2}=0.9 eV is similar to the experimental breakdown voltage. As a consequence, we attribute the breakdown at lower voltages than expected from 2D simulations to (i) the 3D geometry that increases the electric field at the channel/trench corners and (ii) the enhanced injection of electrons into the buffer when Gunn domains start to be formed. Another evidence supporting the fact that the appearance of the Gunn instability triggers the avalanche process is that the velocity-field characteristics extracted from the I-V curves of the diodes[22] show that failure takes place just the electric field within the channel reaches about 200 kV/cm (for devices with both L=1.0 and 0.5 μm), just the value for which the peak velocity is found and the negative differential mobility region starts. Even if the 3D simulations should have been done in order to perfectly reproduce the corners of the channels, where the electric field would concentrate, the 2D simulations performed here are able to capture the main qualitative dependencies of the amount of II mechanisms appearing at the hotspot and the effect that the substrate contact has on it.

Results and Discussion

When high biases are applied to the GS-PGDs, Figure 3, some electrons are able to penetrate into the buffer, where they find a huge electric field at the anode-side corner of the etched region, Figures 3(a) and (b), just at the boundaries of the dielectric, the highly doped GaN active layer and the undoped GaN buffer. Such high electric field, in the presence of a non-zero electron concentration in the buffer, leads to the onset of II mechanisms in that region, as observed in Figures 3(g) and (h), being almost null for an applied bias of V=20 V, but already significant for V=30 V.

One of the possibilities to suppress such effect is improving the isolation by realizing deeper trenches.[22] Indeed, MC simulations indicate that a trench depth of about 250 nm

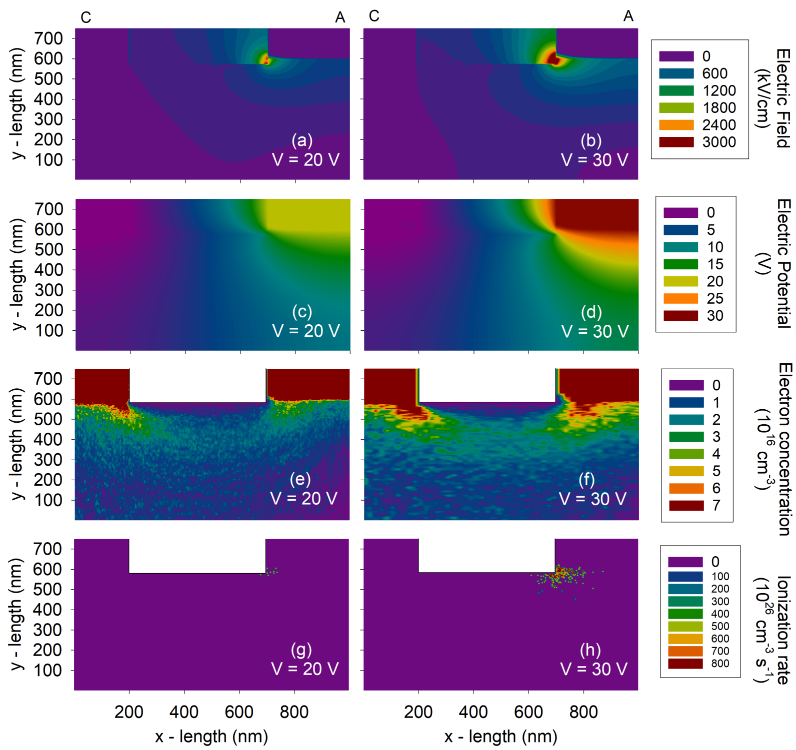

Figure 3: Maps of (a) and (b) electric field modulus, (c) and (d) electric potential, (e) and (f) electron concentration and (g) and (h) II rate for (a), (c), (e) and (g) V=20 V and (b), (d), (f) and (h) V=30 V.

(100 nm deeper than the active layer thickness) is able to almost completely avoid the leakage current and thus protect the diodes from failure. However, realizing such deep trenches is a difficult technological process. That is why we suggest the use of a bottom substrate (backside) contact, whose bias V_S can help to reduce the possibility of avalanche in the GS-PGDs. In such three-terminal GS-PGDs (3T-GS-PGDs) the substrate contact bias V_S can be controlled to either reduce the electric field hotspot (when applying positive values of V_S) or suppress the leakage current (for negative V_S). To fabricate a real 3T-GS-PGD, a further substrate thinning step should be added to the technological process, but it is just an etching step which could be performed even in a post-processing stage. This bottom recess process is not extremely demanding since its size can be large (it can cover the whole device), and the alignment with the top lithography is not crucial and can easily be made through the transparent GaN and SiC layers. The most critical point would be to well calibrate the

depth of such a deep etching, which determines the distance between the active region and the substrate contact. Also, the small thickness of the membrane fabricated could lead to a mechanical stress which may produce destructive cracks in the device.

Figure 4 shows the maps of electric field, electric potential, electron concentration and electron energy for V=30 V and several values of V_S in the 3T-GS-PGDs with two different substrate terminal configurations: (i) Schottky contact and (ii) metal-insulator-semiconductor (MIS) contact. Within MC simulations, in the case of the Schottky contact, electrons are not injected into the semiconductor, but they are absorbed when reaching the metal contact, thus leading to a non-zero current (mainly in the case of positive substrate bias), while in the MIS substrate contact the electron flux is completely blocked (tunneling is not considered in the model), so that current is always null. In Figure 4 one can observe that when applying a negative substrate bias of V_S=-10 V, even if the electric field at the hotspot is somewhat increased, the buffer leakage current is suppressed by the vertical electric field imposed by V_S, so that II processes are almost completely cancelled due to the absence of electrons in the buffer. Under these bias conditions the substrate contact does not practically affect the value of the anode current, so that the generation of Gunn oscillations within the channel is not degraded. Note that the results shown in Figure 4 for V_S=-10 V correspond to the case where a non-injecting Schottky contact has been simulated at the bottom boundary of the buffer, but the result is the same with the MIS contact configuration (not shown). This beneficial buffer leakage suppression effect would not be observed if an ohmic substrate contact is implemented since electrons would be injected from the substrate terminal. Note, that the effect of this backside contact is just to provide an electrostatic control without any vertical current, as in the case of vertical transistors,[29,30] also avoiding the detrimental effects that buffer traps may cause to device operation.

On the other hand, for positive values of V_S, a remarkable electron conduction through the cathode side of the buffer layer takes place (it is not a perfect insulator), but the electric field is effectively reduced at the anode side of the recess. This can be clearly observed

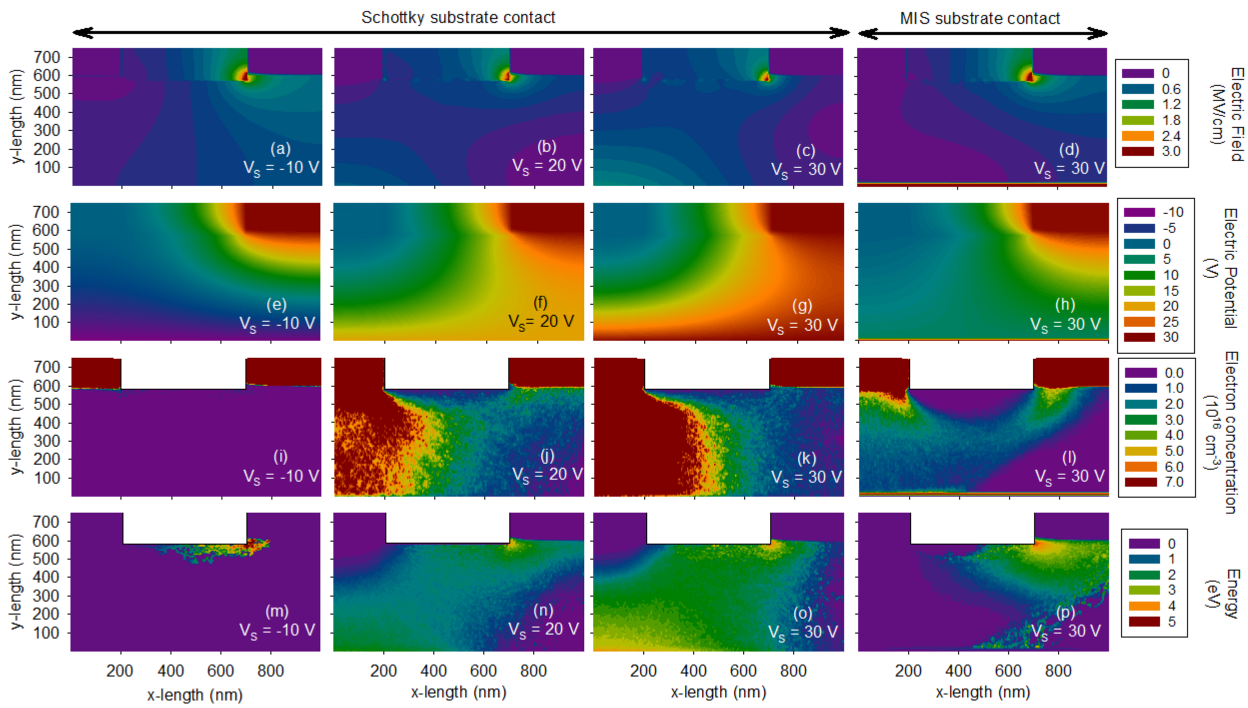

Figure 4: Maps of (a), (b), (c) and (d) electric field modulus, (e), (f), (g) and (h) electric potential, (i), (j), (k) and (l) electron concentration and (m), (n), (o) and (p) electron energy for V=30 V and different substrate bias V_s=-10 V, +20 V and +30 V. The results shown in (d), (h), (l) and (p) include a dielectric layer (10 nm) with ε_r=6 in between the semiconductor and the substrate contact.

in the profiles of electric field shown in Figure 5. As a consequence, even if the electron concentration in the buffer is quite large (higher as V_S increases), II is mostly suppressed at the hotspot region. The problem is that for V_S above 30 V, II mechanisms arise at the cathode side of the buffer due to the vertical conduction between cathode and substrate, which produces highly energetic electrons, Figure 4(o) for V_S=+30 V.

In order to find the optimum value for V_S, Figure 6(a) shows the number of II mechanisms as a function of V_S compared with the result in absence of the substrate contact. II is increased when the V_S is set to zero with respect to the absence of substrate contact due to the different voltage distribution at the anode side of the device: the electric potential at the bottom surface is higher than zero when the substrate contact is not present, thus decreasing the electric field and the corresponding impact ionization rate, see Figures 3(b) and 3(h). The negative range of V_S has the most effective avalanche mitigation effect, since

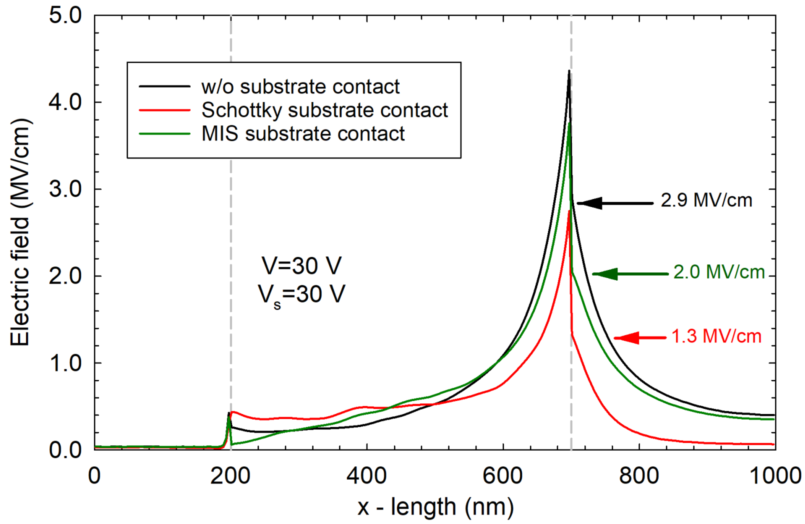

Figure 5: Profiles of the electric field modulus at the position corresponding to the n^+-buffer homojunction (where the maximum electric field and II rate are observed, see Figure 3), for V=30 V and V_S=30 V for the GS-PGD and both the Schottky and MIS configurations of the 3T-GS-PGD. The position of the trenches is indicated by the vertical dashed lines and the value of the maximum electric field within the semiconductor for each case is shown with the arrows (showing also its numerical value).

a complete suppression of the II processes is obtained at V_S below -15 V for V=30 V (and -5 V for V=20 V). But also, the reduction of the electric field at the hotspot attained when V_S is positive is also able to reduce the II rate. In this case, the optimum value is found to be around 10-15 V for V=20 V and around 20 V for V=30 V, but the effect is smaller than for negative V_S. This is due to the fact that when V_S is increased II mechanisms arise near the substrate contact due to the current flowing between cathode and substrate, as explained before. In order to separate the II events taking place near the hotspot region from those arising from the vertical current, such contributions are represented separately in Figures 6(b) and (c) (accounting for the II events taking place at the top 300 nm of the epilayer and those below that region, respectively). Figure 6(b) shows how the value of V_S to be applied in order to completely suppress II near the hotspot is quite high, around 40 V for V=30 V, so that II near the substrate contact is already quite strong, Figure 6(c). Indeed, the amount of II is very significant for V_S>25 V, regardless of the anode-to-cathode bias (as expected since it is from the grounded cathode from which electrons are injected). Moreover, the substrate terminal current is even higher than the anode current for V_S above 10 V (not shown here), so that, on the one hand, can hinder the onset of Gunn oscillations and, on the other, may strongly contribute to self-heating and the degradation of the device performances. Such bias conditions should therefore be avoided.

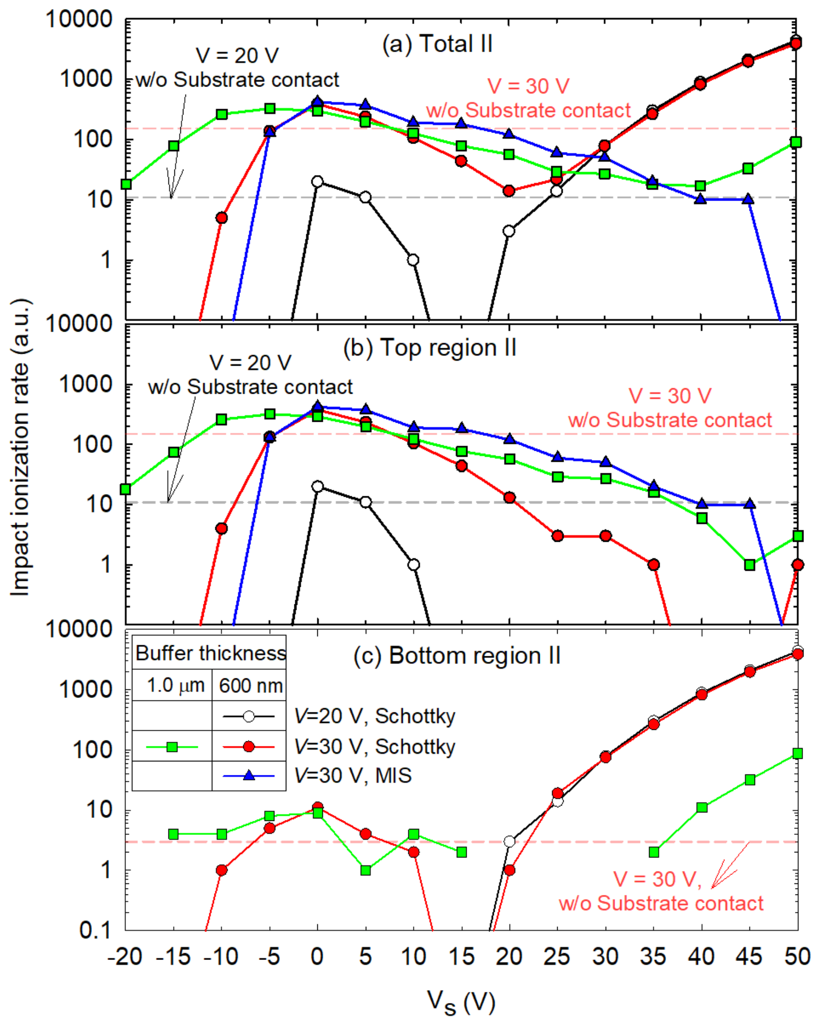

Figure 6: II rate *vs.* V_S in 3T-GS-PGDs with Schottky contact configuration and buffer thickness 600 nm, for anode-cathode biases of V=20 V and 30 V compared with those obtained for GS-PGDs (in absence of the substrate contact, dashed horizontal lines). For V=30 V also the results for the MIS configuration and the Schottky one with a thicker buffer of 1.0 μm are plotted. (a) Shows the total number of II events, (b) those taking place near the hotspot (above the bottom 300 nm of the layer structure) and (c) those near the substrate contact (within 300 nm distance).

One way to mitigate the detrimental effects originated from the vertical current is to increase the thickness of the GaN buffer. In Figure 6, the results of the simulations when the buffer thickness is increased from 600 nm to 1 μm are also plotted. It can be observed that II near the substrate terminal is almost completely suppressed up to V_S 40 V, so that its optimum value increases to about 35-40 V, as the substrate contact is located further from the hotspot region. This electric field screening effect is also observed in the negative range of V_S, since voltages below -20 V have to be applied in order to completely suppress the leakage below the etched region and the associated II processes.

A better way to solve the problems originated by the vertical cathode to substrate current when applying positive V_S values is to use the MIS configuration of the substrate contact. In this case, an additional dielectric layer is to be interposed between the substrate terminal and the substrate layer. The simulations have been performed using a 10 nm dielectric layer with ϵ_r=6 (corresponding approximately to that of SiN), and the result is shown in Figures 4(d), (h), (l) and (p), for V_S=+30 V. We have to remark that in a practical implementation of this MIS backside contact approach the thickness of the dielectric should be increased in order to completely suppress the tunneling current (MC simulations do not consider such effect). It is observed that the MIS contact, by suppressing the vertical conduction through the buffer, is able to almost completely avoid the II events, Figure 5, even if the electric field at the hotspot is not lowered as much as with the Schottky contact configuration. This can be observed in Figure 5, where the electric field at the semiconductor side of the hotspot is decreased from around 2.9 MV/cm for the GS-PGD to approximately 1.3 MV/cm and to 2.0 MV/cm for the Schottky and MIS configurations, respectively, of the 3T-GS-PGD. This configuration allows for the use of a single DC bias by short-circuiting anode and substrate (by means of via holes), thus simplifying the device connections without the need of accessing to the bottom side. Apart from this simple, two-contact implementation, the optimum choice is to apply separate bias values for the cathode and the substrate (which can also be made by accessing the bottom contact through via-holes) so that the optimum substrate voltage can be applied depending on the cathode bias, buffer thickness, operation temperature, etc. The flexibility of the choice of V_s allows to individually optimize the breakdown of each device, but it has to be done after the fabrication process since it will be strongly dependent on the diode topology, buffer quality, etc. Finally, we would like to remark that Gunn oscillations in 3T-GS-PGDs are only slightly influenced by the presence of the substrate terminal and their behaviour is similar to that observed in GS-PGDs, previously studied in Ref.[21]

Conclusions

In conclusion, we have found that buffer leakage current in highly doped GaN GS-PGDs is at the origin of the failure mechanism of fabricated devices due to the electric field hotpot appearing near the anode side of the etched trenches, which provokes an avalanche process. We have demonstrated that the addition of a substrate contact is effective in reducing the amount of II mechanisms by reducing the electric field hotspot (by applying positive V_S) or decreasing the leakage through the buffer (by applying negative V_S), so that it could be implemented in real devices to improve their reliability by increasing their breakdown voltage and effectively generate Gunn oscillations. Both Schottky contact and MIS configurations have been analysed, the latter being able to avoid the vertical cathode-to-anode conduction for V_S>0 and allowing for the use of a single DC bias for anode and substrate.

Acknowledgement

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