# Evidence of surface charge effects in T-branch nanojunctions using microsecond-pulse testing

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*Abstract*—The understanding of the influence of surface charge effects on the electrical properties of nanostructures is a key aspect for the forthcoming generations of electronic devices. In this work, by using an ultrafast electrical pulse characterization technique, we report on the room-temperature time response of a T-branch nanojunction which allows identifying the signature of surface states. Different pulse widths from 500 ns to 100 μs were applied to the device. For a given pulse width, the stem voltage is measured and compared with the DC result. The output value in the stem is found to depend on the pulse width and to be related to the characteristic charging time of the interface states. As expected, the results show that the well-know nonlinear response of T-branch junctions is more pronounced for long pulses, beyond such a characteristic time.

## 1. Introduction

Three terminal junctions (TTJs) with nanometer dimensions have been extensively studied in the literature [1-18]. A large number of potential applications, both analog and digital, have been proposed. In a TTJ, the open circuit voltage at the central stem $V_S$ is always negative when left and right contacts are biased in push-pull fashion ($V_L$=-$V_R$). This nonlinear characteristic of TTJs can be used for detecting AC signals [2], high-frequency harmonic generation [3], signal mixing [4] and performing logic operations [5, 6]. Wesström [7] predicted theoretically a negative differential conductance effect which was confirmed experimentally by Lukasz *et. al* [8]. Müller *et. al* [9] have demonstrated current and voltage gain with the center branch used as a leaky gate and, recently, Spanheimer *et. al* [10] reported on power gain at room temperature up to 1.5 GHz, demonstrating the capability of TTJs to act as active devices. These nanodevices exhibit robust rectifying phenomena also at room temperature [11] and in different material systems: III-V semiconductor heterostructures [12], silicon-on-insulator (SOI) [13], carbon nanotubes [14], InAs nanowires [15] and even recently in graphene [16]. Charges trapped on the sidewalls of the etched branches of TTJs play a crucial role in their behavior by depleting part of the conducting channels and modifying the potential profiles [17, 18], specially when the lithographic dimensions are of the order of the lateral depletion [19].

Due to their nanometric size, and by means of the use of high mobility materials, the operation frequency of TTJs is likely to reach the THz range. Indeed, the authors of this letter have reported theoretical expectations of intrinsic response of TTJs up to THz by means of Monte Carlo simulations [4]. However, only an experimental demonstration up

to 94 GHz has been achieved till now [19], even if a recently proposed time-domain electro-optical measurement setup estimates a cut-off frequency of around 500 GHz [20]. Most of the experimental works in the high-frequency regime were done using 50 Ω high frequency environments. Nevertheless, the mismatch due to the high impedance of TTJs makes very difficult such type of measurements [8, 10, 19].

The poor response of TTJs at very high frequency is generally explained by the cut-off due to the association of high impedance values of the devices and parasitic capacitances. However, in some cases, authors suspect that the dynamics of charge transfer between the bulk of the etched channels and the surface states, which may take place by thermionic emission and tunneling mechanisms [21-23], can also influence the AC performance of TTJs.

In previous papers based on Monte Carlo simulations, we have predicted a strong influence of surface charges on the DC electrical properties of TTJs [18] and speculated that beyond the characteristic frequency of the charging/discharging dynamics of traps the detecting capability of the TTJs could be reduced (even if they would be still satisfactorily operative) [4]. To clarify these questions and provide experimental evidence, we propose an ultrafast electrical pulse characterization of TTJs to confirm the influence of surface traps and investigate their dynamics.

It is to be noted that the surface charges have typical times around μs, while the RC time constant introduced by parasitic/impedance effects is around tens/hundreds of ps (R~kΩ and C~fF, leading to cut-off frequencies of the order of tens/hundreds of GHz [19]). Consequently, both effects are well separated in frequency by several decades. Here we will focus on the surface charge effects taking place at the lower frequencies, around

MHz, far away from the ultimate RC high-frequency cut-off of the device operation (which is also below the intrinsic limit of TTJs, which can reach the THz range).

The paper is organized as follows. In Section 2 the device under analysis is presented, followed by a brief description of the electrical characterization setup. Results of the output voltage for different pulse widths are reported and discussed in Section 3. Finally, Section 4 summarizes the work.

## 2. Device under test and experimental setup

A T-shaped TTJ fabricated by electron beam lithography and dry plasma etching from a δ-doped $Al_{0.48}In_{0.52}As/Ga_{0.25}In_{0.75}As$ heterostructure will be studied [Fig. 1(a)]. This heterostructure is the same as that of the TTJs presented in Ref. 20. We want to remark that the channel has a 75% indium content to get maximum electron mobility and the device has been passivated with a $Si_3N_4$ layer by means of a PECVD technique. A sheet carrier density $n_s=2.5\times10^{12}$ cm$^{-2}$ and a Hall mobility $\mu_H=14000$ cm$^2$/Vs were measured at room temperature. These high values of $n_s$ and $\mu_H$ contribute to reduce the square resistance $R_\square$ of the layer structure, thus lowering both the device resistance and the parasitic resistance of 2DEG access reservoirs. In Fig. 1(b) an atomic force micrograph (AFM) of the device is depicted [24]. Fig. 1(c) shows the AFM image of the structure in 2D, where the dark areas have been etched away. The distance between the left and right reservoirs is about 600 nm, while the width of the horizontal branches is around 200 nm. The stem has a length of 500 nm and a width of 100 nm approximately. The induced lateral depletion due to the surface charge has been experimentally estimated to be

around 40 nm at each side of the channel [19], so the surface effects are expected to be relevant in the 100 nm-wide stem.

For the electrical characterization of the TTJ the three branches are connected as follows: the left one is grounded, a voltage $V_R$ is applied to the right one and the voltage at the bottom contact (or stem) $V_S$ is measured in open circuit, as shown in Fig. 1(c). Several devices in different regions of the wafer were tested showing similar results. This configuration is known as push-fix biasing scheme. The DC measurements are performed by means of a Keithley 4200 SCS Semiconductor Parameter Analyzer. It is to be noted that the current in the vertical branch is null, as it is connected to a source-measure unit (SMU) working as a voltmeter with infinite impedance.

To evidence the influence of surface charges on the dynamic response of TTJs, in addition to the DC measurements we propose to exploit a pulse characterization technique. To this end we have used a pulse measurement unit (Keithley 4225-PMU) with a remote amplifier/switch (Keithley 4225-RPM) which allows us to perform ultrafast I-V measurements. Fig. 2(a) shows the shape of the applied pulses, with the different features that can be modified. Our aim is to determine, like in the DC case, the curve of open-circuit stem voltage $V_S$ vs. amplitude of the input right-voltage pulse $V_R$ for different pulse widths ($\delta_T$). However, we have already shown [4] that the frequency response of a high impedance device using high a impedance measurement system (like an oscilloscope) in presence of the capacitance due to the BNC cable is strongly affected by a cut-off frequency associated to the measurement setup which hinders the intrinsic response of the device. To circumvent this issue we used a low impedance measurement environment: we proceed as shown in Fig. 2(b). We sweep in pulse way the voltages

applied to the stem and to the right contact, from -0.8 V all the way to 0.3 V [corresponding to the range of $V_S$ in Fig. 3] and from -1 V to 1 V, respectively. Synchronized pulses of identical width covering the indicated ranges are applied in both contacts. In this way it is possible to identify, for each $V_R$ amplitude, which is the value of $V_S$ for which the current at the stem $I_S$ is null (i.e. intersects the 0 value). Therefore the open-circuit (zero-current) stem voltage is determined for each value of $V_R$ and for the different pulse widths. We have double-checked this approach by using the SMU (with DC voltages) instead of the PMU, replicating the $V_S$-$V_R$ curve obtained for long pulses (if thermal effects are avoided). In order to compensate unwanted voltage drops in the test circuit (50 Ω output impedance of pulse system and leads, cables, probes and pin resistances) we have used a Load Line Effect Compensation (LLEC) algorithm. In addition, we did a PMU connection compensation (short and open). For the pulse measurements we used 100 pulses to average in each sweep point, returning one reading per pulse burst. The pulse window where the measurement is performed is 75-90% of the total width. The timing parameters are: 1 ms of period and 0.1 μs of delay (to enable for pre-pulse waveform capture). The base of the pulses is always 0 V and rise and fall times are 40 ns.

## 3. Results

The DC values obtained for $V_S$ (and the horizontal current in the inset) for the TTJ when biased with the SMUs in push-fix are shown in Fig. 3. The typical nonlinearity observed in the measured $V_S$ vs. $V_R$ curve is attributed to addition of two effects: i) the ballistic nature of electron transport and ii) surface charge effects (see for example Ref. 20). The

physical origin of the linear dependence in the high-bias regime $|V_R|>0.45$ V [corresponding to the saturation in the current, inset of Fig. 3] is the onset of intervalley scattering mechanisms [4, 20]. On the other hand, the quadratic dependence within the low-bias regime is influenced by the geometrical dimensions of the horizontal and vertical branches [18]. Surface charges were suggested to play a key role in the dependence of such a quadratic response on the geometrical dimensions [19]. If that is the case, the AC performance of TTJs is expected to be influenced by the dynamics of surface states [4]. Pulse measurements, never used so far to characterize TTJs, can provide quite useful information on such dynamics.

The results for the $V_S$ vs. $V_R$ curve obtained with the PMU with pulses of width $\delta_T$= 500 ns, 1 μs, 10 μs, and 100 μs are shown in Fig. 4. It should be noted that here, even if measurements are performed in push-fix mode, we present the results converted into push-pull bias configuration ($V_R$= -$V_L$=$V_{bias}$) [25] in order to more clearly evidence the variations of $V_S$. As observed, the values of $V_S$ are of lower amplitude for shorter pulses. This can be understood as follows. As we suggested in [17], the stem voltage is the result of the combination of an horizontal effect originated by the ballistic transport (combined with very fast surface effects in the horizontal branches) and a vertical one coming from the interface charge effects at the stem walls, since the local values of the surface charge vary with the bias conditions. The enhancement in the value of $V_S$ due to the surface effects is only possible when the surface charge density has enough time to readapt its value to the applied bias. If the pulse width is much smaller than the charging time of the traps, the stem output corresponds only to the horizontal effect. In that case the distribution of surface charges at the central branch remains essentially as at equilibrium

(note that the base of the pulses is always 0 V). However, for longer pulses (of the order of the charging time of interface states) the surface traps evolve with the bias and lead to more negative values of $V_S$. This confirms our previous findings of Ref. [4], where Monte Carlo simulations provided different values of $V_S$ depending if the surface charge was allowed or not to evolve with the bias. We have checked that the values obtained for the longest pulses, $\delta_T$=100 μs, coincide with those obtained in DC (if the duty cycle of the pulse measurement is sufficiently short to produce similar thermal effects).

By plotting the value of the stem voltage versus the pulse width, as done in Fig. 5, it is possible to estimate the characteristic charging time of the traps. A regression fitting according to an expression $V_S = V_S^0/(1+\tau_c/\delta_T)$ is also plotted in Fig. 5, where $V_S^0$ is the stem voltage for long pulse widths (DC value) and $\tau_c$ the characteristic charging time of the traps. As observed, the estimated values of $\tau_c$ are around some tenths of μs, and depend of the amplitude of $V_{bias}$. Indeed, the calculated $\tau_c$ is longer for smaller applied voltages, taking a value of 0.54 μs for $V_{bias}$=0.2 V. The reason for this behavior lies in the fact that the charging time not only depends on the lifetime of the traps present at the sidewalls of the branches, but also on the faster or slower dynamics of the electrons that due to thermionic emission occupy such states, mainly at the stem, as explained in [4]. The higher the voltage $V_{bias}$, a stronger and quicker electron injection into the stem takes place, allowing for a faster response of the surface charge.

## 4. Conclusions

We have shown that pulse characterization can provide useful information about the time dependent surface effects in nanodevices. By means of pulse I-V measurements

performed in a TTJ we have confirmed that the surface charge at the air-semiconductor interfaces of the branches enhances the rectifying behavior of these devices, but simultaneously introduces a delay in their time response that could deteriorate their performance at frequencies well below the cut-off introduced by the RC decay. Several devices were tested, all giving analogous performance. The characteristic times of such response depend on the bias, varying from 0.54 μs for $V_{bias}$=0.2 V to 0.10 μs for $V_{bias}$=0.5 V.

## 5. Acknowledgements

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## FIGURE CAPTIONS

Fig. 1. (a) Three dimensional geometry and layer structure of the studied device. (b) AFM image of the T-shaped junction with height scale indicator. (b) Same image in 2D with the leads, labeled left, right and center, together with the DC bias scheme. AFM images were processed using the WSXM freeware software described in Ref. 24.

Fig. 2. (a) Shape of the pulses used in the time response characterization and the different involved parameters. It is to be noted that the pulse width, $\delta_T$, is defined at 50% of the amplitude. (b) Set-up for the pulse measurements.

Fig. 3. $V_S$ vs. $V_R$ curve obtained in DC (using the SMU) under push-fix bias ($V_L$=0). Inset: Horizontal current in the device.

Fig. 4. Zero-current output voltage $V_S$ vs. push-pull bias amplitude ($V_R$=-$V_L$=$V_{bias}$) obtained by means of the pulse measurement scheme shown in Fig. 2 for different pulse widths $\delta_T$.

Fig. 5. Evolution of the stem voltage with the pulse width under different bias conditions: $V_{bias}$=0.2 V, $V_{bias}$=0.3 V, $V_{bias}$=0.4 V and $V_{bias}$=0.5 V.

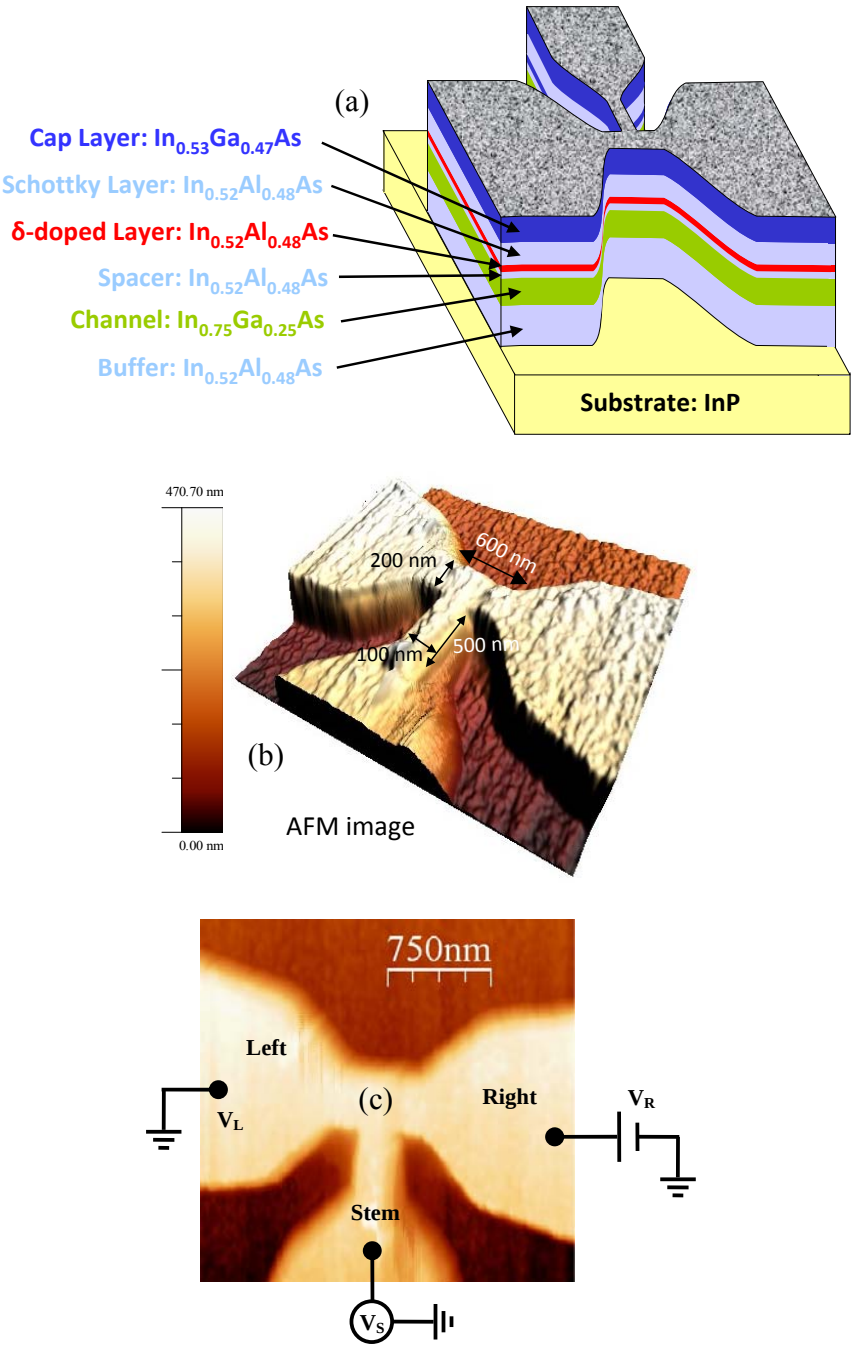
(a)
Cap Layer: In0.53Ga0.47As
Schottky Layer: In0.52Al0.48As
δ-doped Layer: In0.52Al0.48As
Spacer: In0.52Al0.48As
Channel: In0.75Ga0.25As
Buffer: In0.52Al0.48As
Substrate: InP
470.70 nm
0.00 nm
200 nm
600 nm
100 nm
500 nm
(b)
AFM image
750nm
Left
(c)
Right
VL
VR
Stem
VS

**Figure 1**

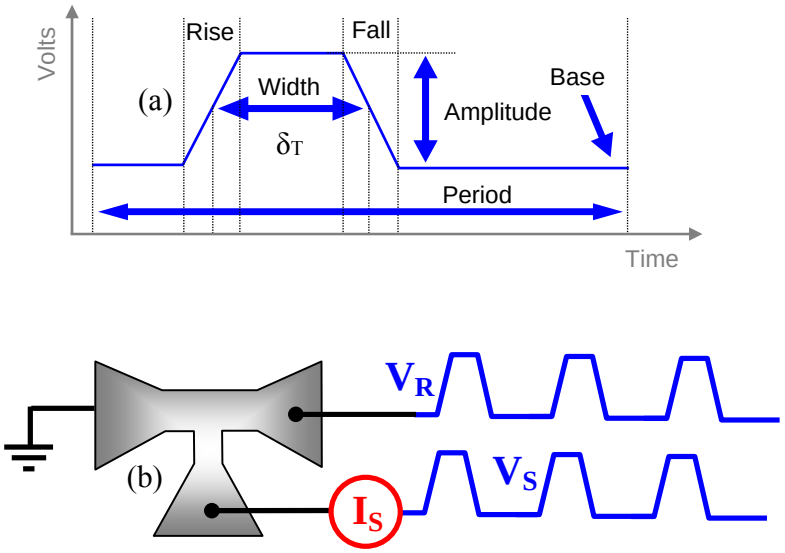
Volts
Rise
Fall
(a)
Width
$\delta_T$
Amplitude
Base
Period
Time
$V_R$
(b)
$V_S$
$I_S$

**Figure 2**

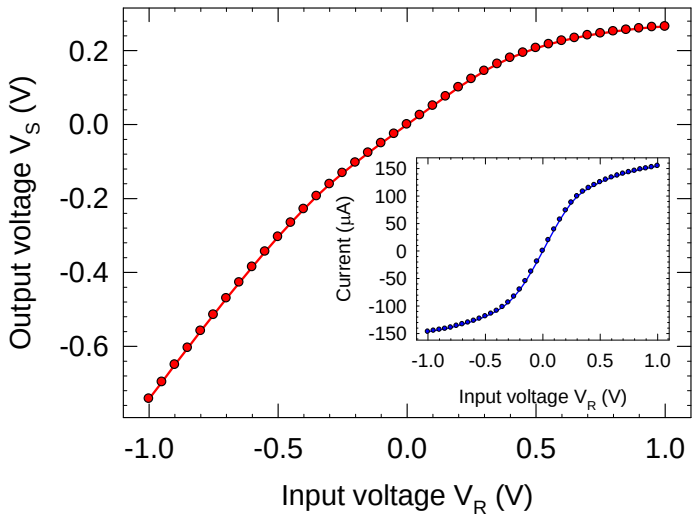
Output voltage $V_S$ (V)
0.2
0.0
-0.2
-0.4
-0.6
-1.0
-0.5
0.0
0.5
1.0
Input voltage $V_R$ (V)
Current (μA)
150
100
50
0
-50
-100
-150
-1.0
-0.5
0.0
0.5
1.0
Input voltage $V_R$ (V)

**Figure 3**

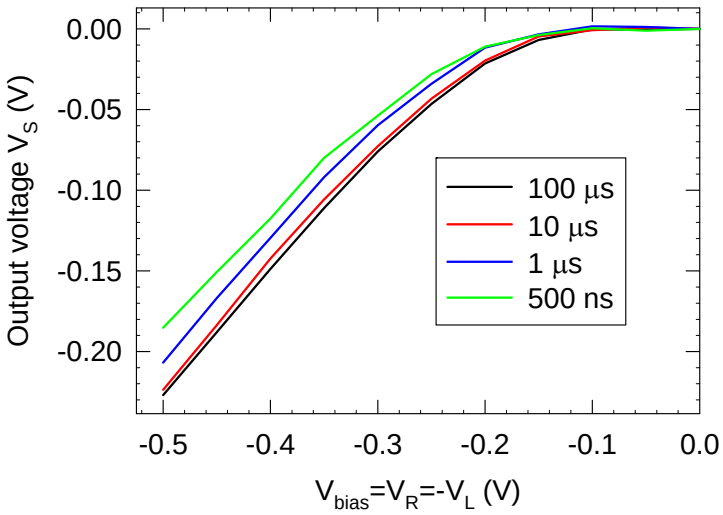
0.00
-0.05
-0.10
-0.15
-0.20
Output voltage $V_S$ (V)
-0.5
-0.4
-0.3
-0.2
-0.1
0.0
$V_{bias}=V_R=-V_L$ (V)
100 µs
10 µs
1 µs
500 ns

**Figure 4**

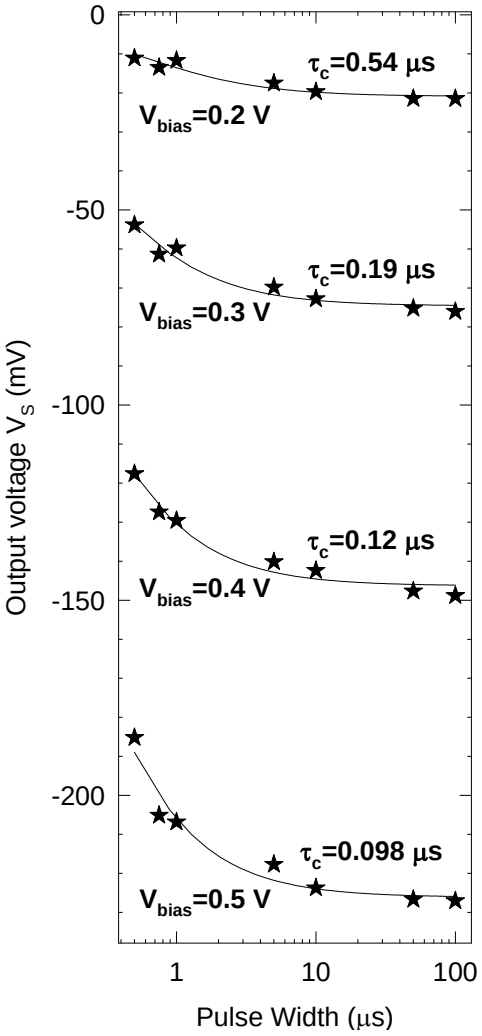
0
-50
-100
-150
-200
Output voltage $V_S$ (mV)
$\tau_c$=0.54 μs
$V_{bias}$=0.2 V
$\tau_c$=0.19 μs
$V_{bias}$=0.3 V
$\tau_c$=0.12 μs
$V_{bias}$=0.4 V
$\tau_c$=0.098 μs
$V_{bias}$=0.5 V
1
10
100
Pulse Width (μs)

**Figure 5**