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Modelling of Thermal Boundary Resistance in a GaN Diode by means of Electro-Thermal Monte Carlo Simulations

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Abstract. In this paper we evaluate heat diffusion in an AlGaN/GaN diode through a Monte Carlo simulator by expanding its capabilities with the implementation of two thermal methods. We present the impact on the device temperature of considering different substrates and die dimensions. We also evaluate the influence of the thermal boundary resistance (TBR) that appears in the growth process of dissimilar materials. We analyse the effect of the TBR when the diode is grown on two substrates, Si and SiC. As a conclusion, we can state that the TBR is a limiting factor to the thermal flow that becomes more relevant for substrates with high thermal conductivities.

1. Introduction

Self-heating properties are an important problem for high-power gallium nitride (GaN) electronic and opto-electronic devices because thermal effects can cause strong damages and premature failure. These effects are boosted by the TBR. The TBR is a measure of the resistance that an interface presents to the thermal flow due to different phonon dynamics and poor crystalline quality near the boundary. The TBR can be measured by employing 3-D micro-Raman thermography [1]. In order to include TBR effects in semiconductor device simulators, different techniques are used, from those based on 3-D finite-difference models [1] to others that employ a continuity condition for a finite interfacial conductance between the layers of interest [2]. But until nowadays the modelling of the TBR effects is still an open problem. In this work, thermal effects will be studied by means of two thermal approximations, both of them implemented in our electronic home-made Monte Carlo (MC) simulator. One is based on a simple Thermal Resistance Method (TRM) [3],[4],[5]. The other is based on the solution of the steady state heat-diffusion-equation (HDE) [4],[6].

This paper is organized as follows. In Sec. 2 the geometry and material components are described followed by a brief explanation of the used electro-thermal models. In Sec. 3 we show the main results for different substrates and die lengths of the diode, making emphasis on the effect of the inclusion of the TBR. Finally, Sec. 4 summarizes the main conclusions.

2. Device structure and electro-thermal simulations

In Figure 1 the geometry of the $Al_{0.27}Ga_{0.73}N$/GaN diode under analysis is presented. The electronic transport will take place in the called electronic domain (delimited by red dashed lines in Figure 1). Piezoelectric scattering and those with phonons and dislocations are included in the model. The influence of spontaneous and piezoelectric surface polarization charges P=12.12×10^{12} cm^{-2} have been incorporated. In addition, a surface charge density σ = - 4.12×10^{12} cm^{-2} is placed at the top of the

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AlGaN layer. The length of the diode is 2 μm. If not indicated, L_1=200 μm and L_2=300 μm. In this work, temperature-independent thermal conductivities will be employed: k_{AlGaN}=30 W/(K·m) [7], k_{GaN}=130 W/(K·m) [8], k_{Au}=300 W/(K·m) [6], $k_{diamond}$=1000 W/(K·m) [9], k_{Si}=156 W/(K·m) [6], k_{SiC}=300 W/(K·m) [10], and $k_{sapphire}$=42 W/(K·m) [11]. A more detailed analysis for temperature-dependent thermal conductivities can be found in Ref. [4].

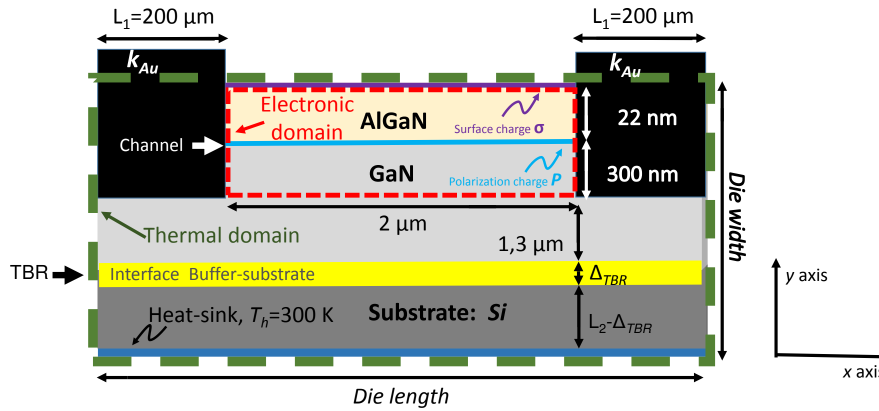

Figure 1. Structure of the $Al_{0.27}Ga_{0.73}N$/GaN diode under study.

Based on our home-made ensemble MC simulator coupled with a 2D Poisson solver [5], we have expanded its capabilities by including the two thermal approaches [4] sketched in Figure 2.

- (*i*) *Thermal Resistance Method* (TRM) (blue colour in Figure 2). This model is based on the use of an ad-hoc thermal resistance, R_{th}, and is only carried out in the electronic domain (delimited by red dashed lines in Figure 1). The lattice temperature is updated every N_{th}=5000 iterations according to the formula:

$$T_{latt}=300\text{ K}+P_{diss}\text{ x }R_{th}\ , \qquad (1)$$

with P_{diss},=I_{DC} x V_{DC} the dissipated power in the N_{th} iterations. The advantage of this model to evaluate the thermal behaviour of devices is the simplicity and low computational effort with respect to other algorithms.

- (*ii*) *Solution of the* HDE (we refer from now to this model HDEM, orange colour in Figure 2). In this case the lattice temperature is updated according to the solution of the HDE equation:

$$\nabla[k(r)\nabla T(r)]=-G(r)\ , \qquad (2)$$

where $k(r)$ is the temperature-independent and inhomogeneous thermal conductivity, T the temperature, and $G(r)$ the power density distribution generated by phonons. Note that the HDE is solved in the whole thermal domain (delimited by green dashed lines in Figure 1). In this case, the HDE is solved every N_{th}=10000.

Boundary conditions are extremely relevant in this kind of simulations. To correctly model the interfaces between layers, we use the continuity condition:

$$k_1\,\partial T/\partial r_n|_\gamma\ =k_2\,\partial T/\partial r_n|_\gamma, \qquad (3)$$

where γ is the interface between two layers with thermal conductivities k_1 and k_2, and r_n the normal position vector. At the two lateral edges, and at the top of the device, adiabatic boundary conditions are imposed, $k_1\,\partial T/\partial r_n|_\gamma\ =0$. At the bottom, a Dirichlet boundary condition is used; a heat sink at 300 K. Our approach to take into account the effect of *TBR* is very simple: we include a small layer of thickness Δ_{TBR} of a material with low thermal conductivity k_{TBR} between the GaN-buffer and the substrate (see Figure 1, yellow layer). In this framework the value of the simulated TBR will be:

$$\text{TBR}=\Delta_{\text{TBR}}/k_{TBR}\ . \qquad (4)$$

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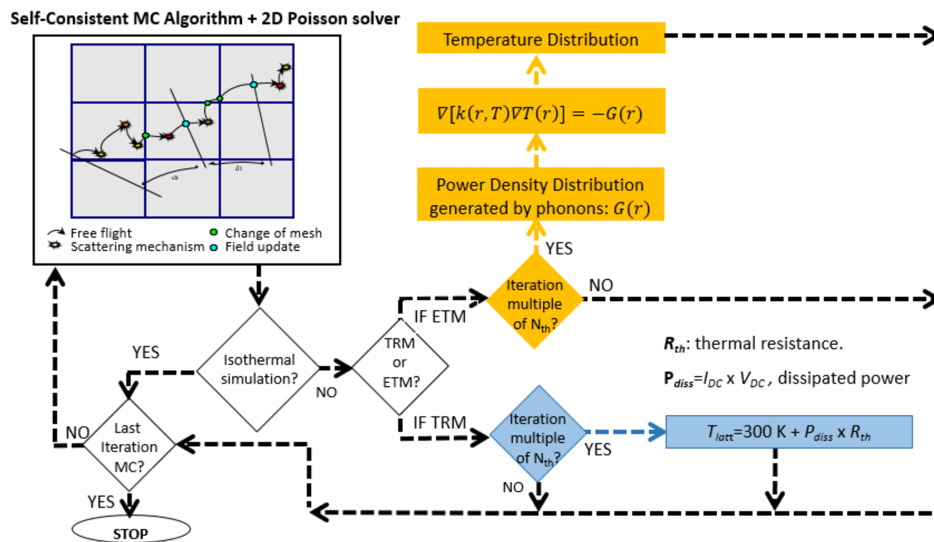

Figure 2. Flow chart of the electro-thermal simulations.

3. Main results

First of all, the effect of growing the device on different substrates is examined through the HDEM, but without the TBR layer. In Figure 3 we plot the *I-V* curves, Figure 3 (a), and the average temperature (T_{av}) in the electronic domain *vs*. the dissipated power, Figure 3 (b). The fitting of T_{av} *vs*. P_{diss} allows us to extract a thermal resistance R_{th}, which is in the range 3.5-38x10^{-3} K·m/W. Moreover, within the HDEM it is possible to study the dependence of that extracted R_{th} on the die dimensions. For example, the values of R_{th} *vs*. L_1 (for L_2 250 μm, 300 μm, and 350 μm) are shown for Si-substrate in the inset of Figure 3 (b). As L_2 is reduced, R_{th} becomes nearly constant with L_1 for lower values of L_1. For a given L_1, as L_2 is increased, the thermal resistance is higher, as expected, since the heat flux generated by the phonons is dissipated less efficiently due to the larger distance from the heat sink to the electronic domain. R_{th} is in the range 12-23x10^{-3} K·m/W.

Secondly, the effect of the TBR is analysed by choosing as reference two substrates, Si and SiC. A layer of thickness Δ_{TBR}=15 nm is introduced at the interface buffer-substrate. Simulations have been performed by considering two thermal conductivities (k_{TBR}) of 1 and 0.1 W/(K·m) for this layer. According to eq. (4) the TBR is equal to 1.5x10^{-8} and 15x10^{-8} m^{2}K/W, being consistent with the reported experimental [1] and numerical studies [12]. In Figure 4 (a) and (b), T_{av} *vs.* P_{diss} is analysed for both substrates. The insets show the profile of the lattice temperature in the middle of the structures of the interface buffer-substrate. As expected, SiC exhibits better thermal behaviour than Si, and lower temperatures are obtained inside the device. But if the TBR is very high (increasing the difficulty for the thermal flow to leave the device), it can be the critical parameter for the design of an appropriate heat sink. Note that the discontinuity ΔT at the interface increases when a higher conductivity substrate is chosen (as example for k_{TBR} =0.1 W/(K·m) ΔT of 125 K and 142 K are obtained for Si and SiC, respectively). Remarkably it may happen that a device grown on a substrate with poor k_s but with a good thermal interface resistance (low TBR) exhibits better thermal behaviour than other grown on a substrate with an excellent k_s but with a high TBR. This behaviour is also reflected in the values of R_{th} obtained, that are in the range 14-21x10^{-3} K·m/W, and 9-17x10^{-3} K·m/W, for Si and SiC, respectively.

Finally, we have proven that both thermal models are equivalent, i.e., a TRM simulation [symbols of Figure 3 (a)] with the thermal resistance extracted from the HDEM simulation (R_{th}=3.58x10^{-3} K·m/W for diamond, 8.9x10^{-3} K·m/W for SiC, 14.1x10^{-3} K·m/W for Si, and 38.2x10^{-3} K·m/W K·m/W for sapphire) provides the same *I-V* curve than HDEM. Obviously, once the TBR is included in the HDEM simulation, a TRM simulation (with the appropriate extracted R_{th}) would also provide the same result than the HDEM.

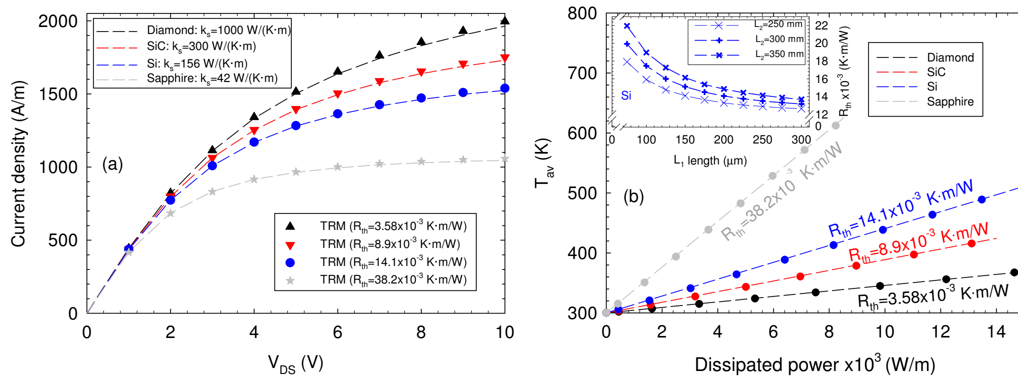

Figure 3. (a) *I-V* curves for different substrates obtained with the HDEM simulation. Symbols: TRM with R_{th}=3.58x10^{-3}, 8.9x10^{-3}, 14.1x10^{-3} and 38.2x10^{-3} K·m/W. (b) Average temperature, T_{av}, *vs*. the dissipated power, and linear fitting to extract the corresponding thermal resistance R_{th}. The inset shows R_{th} *vs*. die dimension L_1 for L_2=250 μm, 300 μm and 350 μm and Si-substrate. If not indicated, L_1=200 μm and L_2=300 μm.

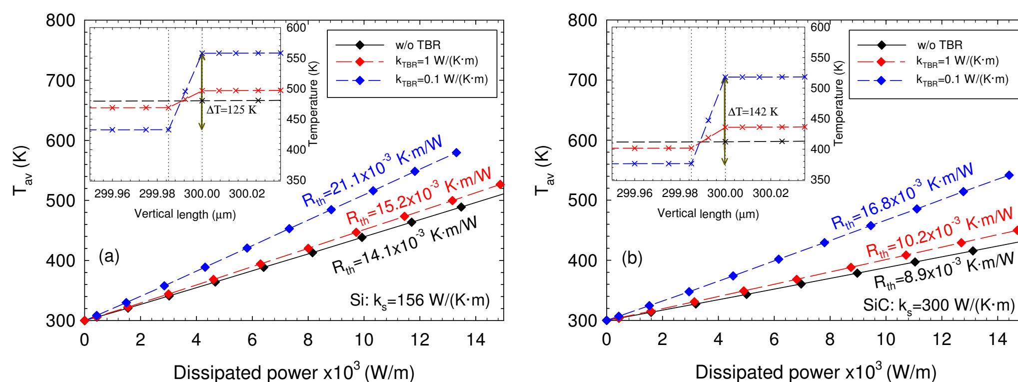

Figure 4. T_{av} *vs*. P_{diss} for two substrates (a) Si, and (b) SiC. A TBR layer of Δ_{TBR}=15 nm with k_{TBR} =1 and 0.1 W/(K·m) is studied. Note that the case without TBR layer from Fig. 3 are included for comparison. The inset shows the profile of the lattice temperature in the middle of the diode close to the TBR region, for a bias of 10 V.

4. Conclusions

In this paper we have presented the effect of the inclusion of the TBR in our MC simulator. Results show that the TBR may have a strong influence, limiting the thermal flux in the interface where it appears. Although the effect of the TBR is higher for the SiC substrate, the temperature reached in the electronic domain is lower compared to the temperature obtained with the Si substrate. The TBR has a strong influence on R_{th}. For a TBR=15x10^{-8} m^{2}K/m, R_{th} is increased respect the case w/o TBR a factor 1.5 for Si and 1.89 for SiC.

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