Evaluation of the Thermal Resistance in GaN-Diodes by means of Electro-Thermal Monte Carlo Simulations

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Abstract — In this paper we use an electro-thermal method [solver of the heat-flux equation coupled with an ensemble Monte Carlo (MC) simulator] to extract the value of the thermal resistance, R_{th}, in diodes consisting in un-gated $Al_{0.27}Ga_{0.73}N$/GaN heterostructures. Different substrates (polycrystalline diamond - PCD, diamond, silicon and sapphire), and die dimensions will be analysed. When a temperature-independent thermal conductivity is considered, the obtained values of R_{th} depend on the geometry and substrate material, and are constant with the dissipated power (P_{diss}). When a temperature-dependent thermal conductivity is needed to correctly reproduce the thermal behaviour of the device, R_{th} exhibits a strong dependence on P_{diss}.

Keywords — Electrothermal modeling, Monte Carlo (MC), thermal resistance, high-temperature, AlGaN/GaN

I. Introduction and Modeling Approach

In spite of the strong potentiality of GaN and AlGaN/GaN based devices for high-power and high-frequency applications, their utilization is limited by the elevated lattice temperatures reached inside them. This excessive overheating is the main hindrance to their reliability and use [1]. Therefore, the correct description of self-heating effects is essential for the accurate modelling of GaN-based devices. In order to take into account thermal effects different techniques can be employed, such as a simple thermal resistance method (TRM) [2], or more complex procedures which take into consideration the solution of the steady state heat-diffusion-equation (HDE) [3]-[4].

Our home-made, semi-classical Monte Carlo (MC) simulator has been proved to be a very efficient tool to investigate electron transport and optimize the static, dynamic and noise operation of semiconductor devices [5]-[6]. In this contribution, we have expanded our simulator to a full electro-thermal model. Specifically, it has been coupled with (i) a thermal resistance method, and (ii) the solution of the HDE [3]-[4]. A sufficient number of iterations of the HDE-MC solver must be carried out in order to reach the convergence of the static electro-thermal solution [7].

The TRM is typically employed to evaluate the thermal behaviour of devices due to their simplicity and lower time consumption with respect to another algorithms. The lattice temperature, T_{latt}, is updated according to the formula $T_{latt}=300+P_{diss}\times R_{th}$ (being P_{diss} the dissipated power). In this approach the value of R_{th} is usually extracted phenomenologically. As an interesting alternative, the HDE-MC simulator allows us not only to analyse the thermal behaviour itself, but also to extract the value of this thermal resistance, as illustrated in this work. Therefore the HDE-MC simulator can be used as a tool to evaluate the R_{th} dependence on the geometry and thermal parameters of the device.

The geometry of the $Al_{0.27}Ga_{0.73}N$/GaN diode under analysis is shown in Fig.1. The distance between the contacts is 2 µm. The electronic and thermal simulations take place in two different domains, also sketched in Fig. 1. Piezoelectric scattering and those with phonons and dislocations are included in the model. To correctly simulate the heterolayer we incorporate the influence of spontaneous and piezoelectric surface polarization charges: P=12.12×10^{12} cm^{-2}. In addition, a surface charge density σ = - 4.12×10^{12} cm^{-2} is placed at the top of the AlGaN layer, which appears as a result of polarization charges partially compensated by charge trapped in surface states [7].

A Dirichlet boundary condition for the HDE is imposed at the bottom of the structure (a heat sink with a constant temperature 300 K). To correctly model the interfaces between layers, we use the continuity condition:

$$k_1\,\partial T/\partial r_n|_\gamma = k_2\,\partial T/\partial r_n|_\gamma\,, \qquad (1)$$

where γ is the interface between two layers with thermal conductivities k_1 and k_2, r_n the normal position vector and T the temperature. The values considered for the thermal conductivities are: k_s=30 W/(K·m) [8], k_s=130 W/(K·m) [9] and k_s=300 W/(K·m) [4] for AlGaN, GaN and Au, respectively at 300 K. Temperature independent and

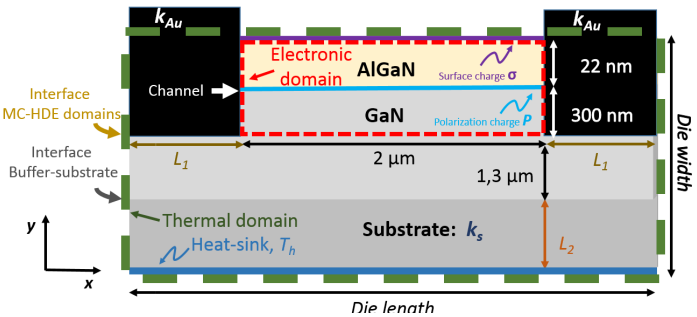

Fig. 1. Schematic structure of the $Al_{0.27}Ga_{0.73}N$/GaN diode under study.

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dependent thermal conductivities will be used in the simulations as it reported in next section.

II. RESULTS AND DISCUSSION

Firstly, considering temperature-independent thermal conductivities, we examine through the HDE-MC simulator the effect of varying (i) the thermal conductivity of the substrate (k_s) and (ii) the semiconductor die dimensions (L_1, L_2).

In Fig. 2 we plot, for devices grown on different substrates (PCD, k_s=2200 W/(K·m); diamond, k_s=1000 W/(K·m); Si, k_s=156 W/(K·m) and sapphire, k_s=42 W/(K·m)), the typical *I-V* curves, Fig. 2 (a), and the average temperature in the electronic domain (T_{av}) *vs.* dissipated power, Fig. 2 (b). For the lower values of k_s, the self-heating becomes crucial: the substrate exhibits a significant influence on the current saturation level; note that for V_{DS}=8 V T_{av}=612 K for sapphire and T_{av}=438 K for Si. In the case of materials with high k_s, although the PCD substrate has a thermal conductivity more than twice higher than the diamond substrate, the current level does not change significantly as a consequence of having similar T_{av}, (355 K and 365 K for V_{DS}=8 V, respectively). This reflects the fact that both substrates possess excellent thermal conductivities and can be considered as good heat-sinks.

Fig. 2 (b) allows us to calculate the values of R_{th} by fitting the T_{av} dependence *vs.* dissipated power obtained from HDE-MC simulations. The values of R_{th} are of the order of 10^{-2} K·m/W, well in the range of typical values for HEMTs [2] (R_{th}=38.2x10^{-3} K·m/W, R_{th}=14.1x10^{-3} K·m/W, R_{th}=4.6x10^{-3} K·m/W and R_{th}=3.58x10^{-3} K·m/W for sapphire, Si, diamond and PCD, respectively). We conclude that R_{th} is inversely proportional to k_s, inset of Fig 2 (b). Such estimated values for the thermal resistances will provide, within a TRM based model, the same *I-V* curves than the simulations with the HDE-MC model [7]. Therefore, the feedback between both models can be used to speed-up the optimization of the device thermal properties, as the TRM approach is faster and require less memory resources. However, with the TRM just a global value of the lattice temperature is calculated, while with the electro-thermal model a local temperature map can be analysed, being possible the identification of hot spots inside the device in more complex devices like HEMTs.

In Fig. 3 we plot, for a 6 V bias, the lattice temperature in the thermal and electronic domains, for the PCD, Si, and sapphire substrates. A strong degradation of the device operation can take place with the sapphire substrate due to the very high temperatures reached as a consequence of the poor thermal conductivity [Fig. 3 (e), (f)] in comparison with Si [Fig. 3 (c), (d)] and PCD [Fig. 3 (a), (b)]. In the electronic domain, the average temperatures are T_{av}=336 K, T_{av}=412 K and T_{av}=528 K (highest values of 345 K, 422 K and 535 K) for the PCD, Si and sapphire respectively.

In Fig. 4 we represent the profiles of the increase of lattice temperature for the same bias at three different *y*-positions (channel, interface MC-HDE domains and interface buffer-substrate). In all cases the temperature peak is located well in the GaN two-dimensional electron gas (2DEG) of the diode. It is noteworthy that when the thermal conductivity is low the lattice temperature for the three layers is almost the same and constant (the sapphire material causes an enormous temperature rise), both in the electronic domain and thermal domain. In this particular case, and if the die length is too short, the contacts will be subjected to high temperatures (which could damage them) in comparison with the cases of diamond or PCD substrates. As was expected, the substrate exerts a strong influence over the self-heating of the device.

In Fig. 5 the dependence of R_{th} respect to die dimensions L_1 (bottom axis, L_2=300 µm) and L_2 (top axis, L_1=200 µm) is represented. In all cases the substrate employed is Si. On the one hand, when L_1 increases above 250 µm, R_{th} remains almost constant, 13.3x10^{-3} K·m/W. We have checked that values of L_1 lower than 100 µm result in very high

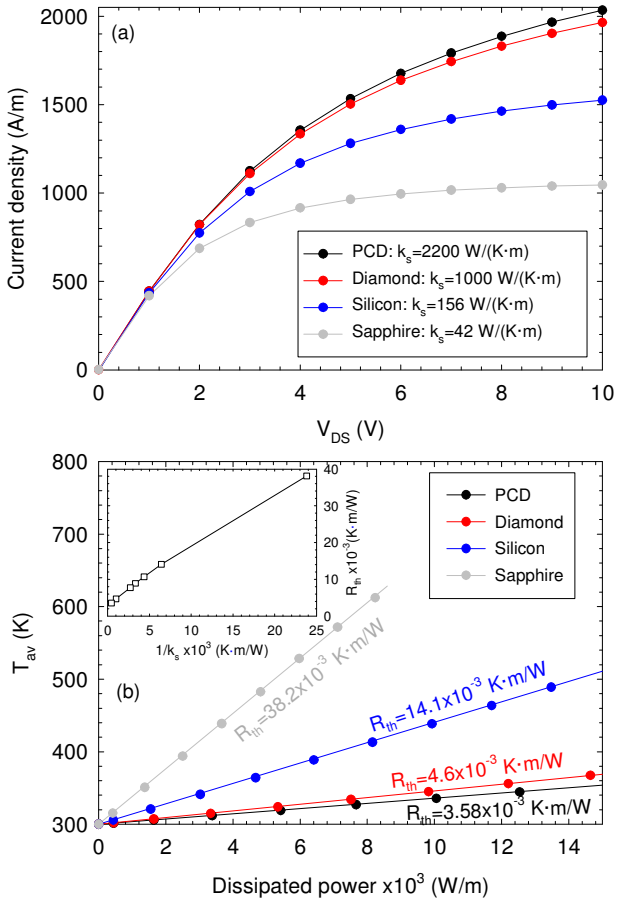

Fig. 2. (a) *I-V* curves for different substrates: PCD [k_s=2200 W/(K·m)], diamond [k_s=1000 W/(K·m)], silicon [k_s=156 W/(K·m)] and sapphire [k_s=42 W/(K·m)]. (b) Analysis to evaluate the influence of k_s in the simulations. Average temperature, T_{av}, *vs.* dissipated power and linear fitting to extract the corresponding thermal resistance. The inset shows R_{th} *vs.* 1/k_s. L_1=200 µm and L_2=300 µm.

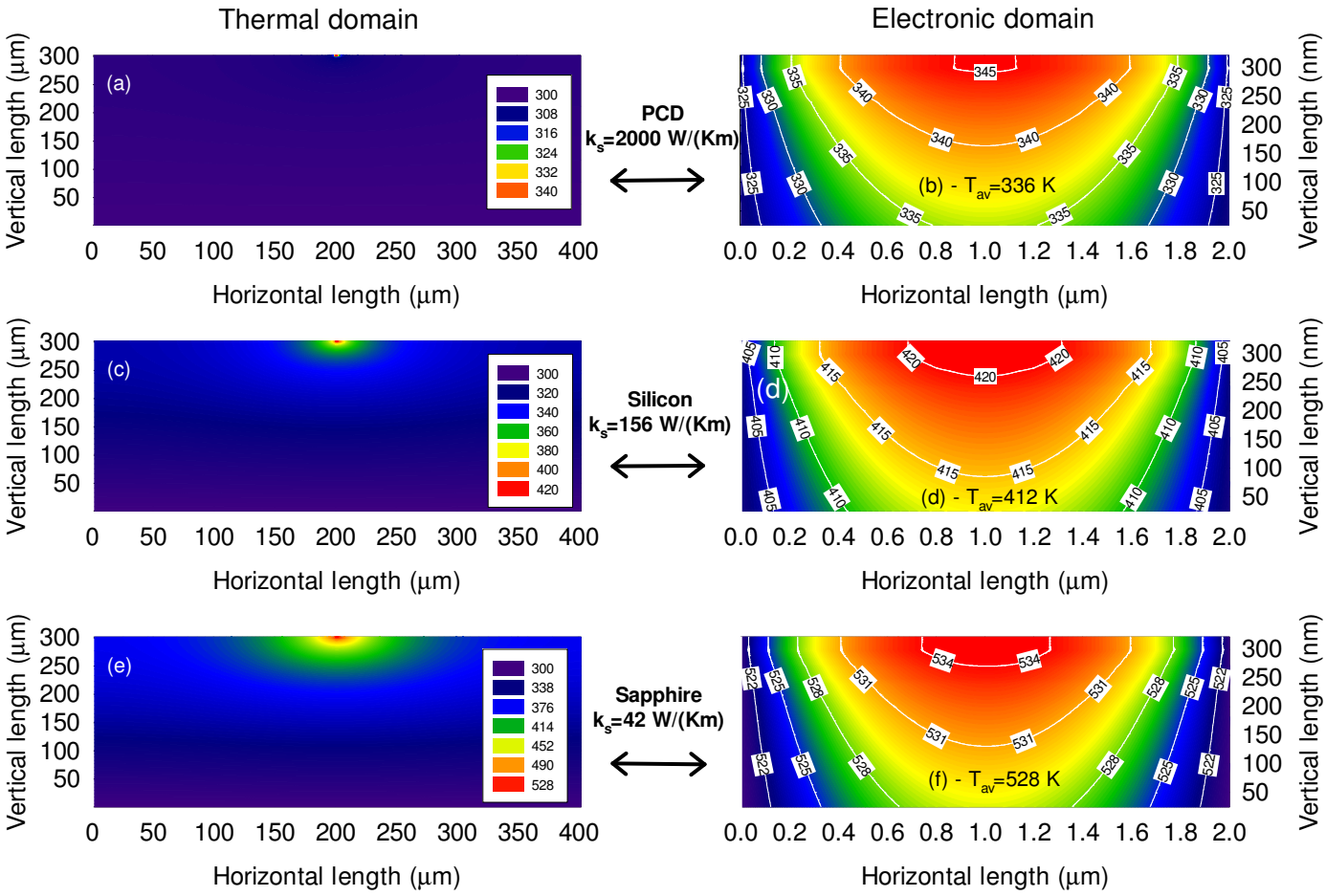

Fig. 3. Temperature distribution, for a bias of 6 V, to evaluate the influence of k_s: PCD, 2200 W/(K·m); silicon, 156 W/(K·m) and sapphire, 42 W/(K·m) in the simulations. Thermal domain (a), (c) and (e), and electronic domain (b), (d) and (f).

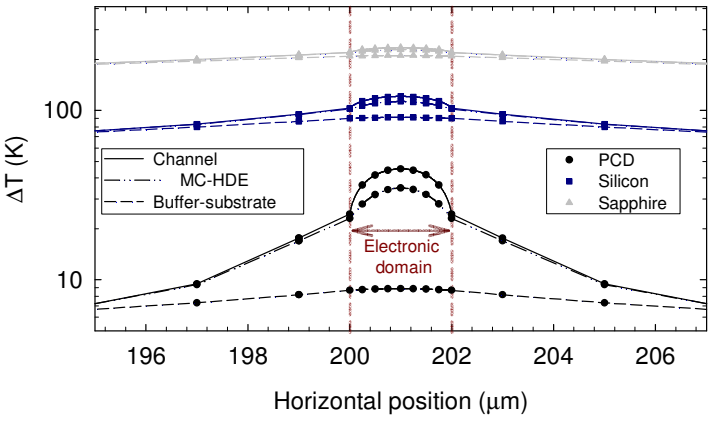

Fig. 4: Profile of the increase of lattice temperature ($\Delta T=T_{latt}-T_h$) for three different *y*-positions (channel, interface MC-HDE domains and interface buffer-substrate, see Fig. 1) for a bias of 6 V.

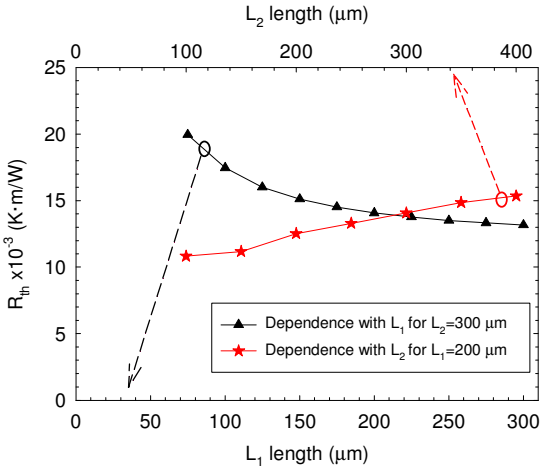

Fig. 5. R_{th} *vs.* die dimensions (a) L_1 (bottom axis, L_2=300 µm) and (b) L_2 (top axis, L_1=200 µm). Both cases are for k_s=156 W/(K·m).

temperatures >700 K at V~10 V, providing values of R_{th}>20x10^{-3} K·m/W. On the other hand, as L_2 is reduced, the thermal resistance is lower, as expected, and therefore heat flux generated by the phonons is dissipated more efficiently because the heat sink is closer to the electronic domain. R_{th} is in the range between 10-20x10^{-3} K·m/W in both cases.

As a second step, when the dissipated power is extremely high, it is appropriate to consider temperature-dependent thermal conductivities for each material. It is well-established that the thermal conductivity, k_i, depends on temperature as $AT^{-\alpha}$, where A and α are characteristics parameters of each material. In order to fulfil the temperature continuity, and furthermore properly resolve the HDE when the Kirchhoff transformation is used, it is necessary to consider the same functional relation $T^{-\alpha}$ for all the involved k_i [4]. For our particular study the value of α was set for all semiconductors to 1.3 [3]-[7]. It provides the best compromise for fitting the whole experimental ensemble of data in the temperature range of interest, and moreover it is the particular dependence of the k_i corresponding to the most relevant layer (Si) for the solution of the HDE, so that:

$$k_i(T) \approx k_i^{300} \cdot \left(\frac{300\ K}{T}\right)^{1.3} . \qquad (2)$$

In Fig. 6 we compare simulations using (i) a k-temperature independent model and (ii) a k-temperature dependent model, for Si substrate, L_2=300 µm and L_1=200 µm. Up to 3 V both models provide same current level. For voltages greater than 3 V, the reduction of the value of the thermal conductivities, according to Eq. 2, provokes an increase of temperature (see inset of Fig. 6), and obviously the current decreases.

Also it can be noted from the inset of Fig. 6 that the temperature-dependent thermal conductivity model does not give a linear response of the average temperature with respect to the dissipated power, being not possible to define a constant thermal resistance. As a consequence, a simple TRM cannot be applied and the HDE-MC scheme is required.

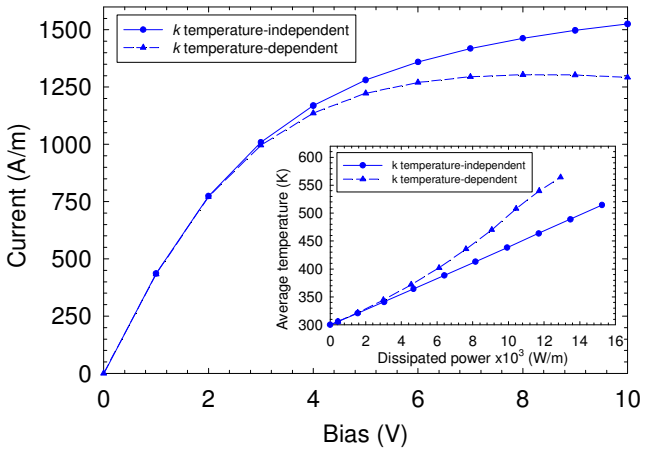

Fig. 6: (a) *I-V* curves obtained with both *k*-temperature independent and dependent models for Si substrate, L_2=300 µm and L_1=200 µm. The inset shows the T_{av} *vs*. dissipated power for the structure in both cases.

CONCLUSIONS

In this paper we have studied self-heating effects in an un-gated AlGaN/GaN diode. On the one hand, when a temperature-independent thermal conductivity is used in a HDE-MC simulator, it has been shown that by a linear fitting of T_{av} with respect to the intrinsic dissipated power it is possible to extract the value of R_{th}. The parameter that has the strongest impact on R_{th} is k_s, followed by L_1, and finally by L_2. R_{th} is extremely high for the sapphire substrate (38.2x10^{-3} K·m/W), and remains almost constant (~13.3x10^{-3} K·m/W) from a length of L_1=250 µm when the Si-substrate is employed. On the other hand, when a temperature-dependent thermal conductivity is employed, R_{th} is function not only of the geometry and materials of the die, but also of the dissipated power. In this later case it would be necessary to carry out the HDE-MC simulations for a proper thermal study of the device.

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