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# Impact of substrate and thermal boundary resistance on the performance of AlGaN/GaN HEMTs analyzed by means of electro-thermal Monte Carlo simulations

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**Abstract**

In this paper, we present results from the simulations of a submicrometer AlGaN/GaN high-electron-mobility transistor (HEMT) by using an in-house electro-thermal Monte Carlo simulator. We study the temperature distribution and the influence of heating on the transfer characteristics and the transconductance when the device is grown on different substrates (sapphire, silicon, silicon carbide and diamond). The effect of the inclusion of a thermal boundary resistance (TBR) is also investigated. It is found that, as expected, HEMTs fabricated on substrates with high thermal conductivities (diamond) exhibit lower temperatures, but the difference between hot-spot and average temperatures is higher. In addition, devices fabricated on substrates with higher thermal conductivities are more sensitive to the value of the TBR because the temperature discontinuity is greater in the TBR layer.

Keywords: AlGaN/GaN HEMT, Monte Carlo, electro-thermal simulations, GaN, self-heating

(Some figures may appear in colour only in the online journal)

## 1. Introduction

In the last decade, gallium nitride (GaN) semiconductors and their alloys (AlGaN, InGaN) have emerged as the most promising materials in a wide range of applications. Thanks to their properties, such as their elevated chemical and thermal stability and radiation hardness, they are robust and ideal candidates for work in aggressive environments [1, 2]. In the particular case of GaN technology, it seemed that it would only be affordable mainly for military purposes, and it was limited in civilian use. However, the evolution of the technology and the reduction in material costs have made GaN-based devices an economical option even for commercial use. This has led to much effort being devoted to the study of this technology, and in the future huge further investment is anticipated. The high breakdown electric field of GaN ($\sim$3.3 MV cm$^{-1}$) [3] and its mobility (900 cm$^2$ V$^{-1}$ $\cdot$ s$^{-1}$) [3] makes it an excellent material for working at very high powers and microwave frequencies [4, 5], as GaN-based devices can simultaneously support high current ($\sim$10 A) and high voltages ($\sim$100 V) [4]. For GaN-based microwave power devices, the thermal behavior due to the self-heating effect is a major limitation because power dissipation is very high [6], as compared to GaAs-based high-electron-mobility transistors (HEMTs) [7]. By way of example, AlGaN/GaN HEMTs begin to fail in the operating temperature range of 500 °C and InAlN/GaN HEMTs can operate up to 900 °C [8]. In addition, it is not only the thermal conductivity of the different layers that affects the heat dissipation of the wafer. It is important to remark that GaN does not have a native substrate, and typically it is grown over different substrates, such as sapphire, silicon (Si) silicon carbide (SiC) or diamond [6, 9]. As a consequence, thermal effects in these devices are also boosted by the so-called thermal boundary resistance (TBR) that appears in the growth process of dissimilar materials [10, 11]. It is a measure of the opposition that an

 

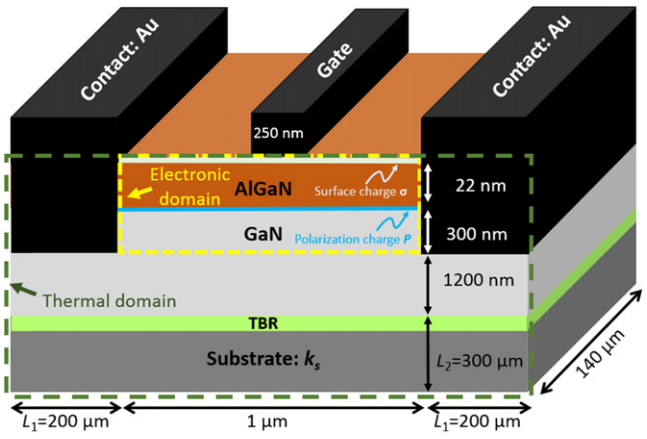


**Figure 1.** AlGaN/GaN HEMT geometry under study. The gate has a length of 250 nm. The area limited in yellow corresponds to the simulated electronic region of the transistor and the region limited in green is the thermal domain, where the heat-diffusion equation (HDE) is solved. The thermal boundary resistance (TBR) layer is included in the simulations of section 3.2.

interface exerts against the heat flow due to different phonon dynamics and poor crystalline quality near the boundary. The TBR can be obtained by employing 3D micro-Raman thermography [10, 11] or by using the thermo-reflectance measurement technique [12]. In order to include TBR effects in semiconductor device simulators, different techniques are used, ranging from those based on 3D finite-difference models [10, 12, 13] to others that employ a continuity condition for a finite interfacial conductance between the layers of interest [14]. However, to date the modelling of the TBR effects is still an open problem, but the consideration of the TBR could be important to investigate the thermal behavior for GaN-based devices. The aim of this paper is to simulate the effects of growing an AlGaN/GaN HEMTs on different substrates (sapphire, Si, SiC and diamond) and the influence of the TBR layer on them. We will make use of an in-house electronic Monte Carlo (MC) simulator proven to be a very powerful tool to investigate electron transport and optimize the static, dynamic and noise operation of semiconductor devices [15]. Self-consistent thermal modelling was recently included in this simulator, and was applied for the analysis of diodes, which allowed its calibration by comparison with measurements [16]. Once calibrated, in this paper the model is employed for the analysis of HEMTs. In particular, the aim of this contribution is (i) to study the performance of an AlGaN/GaN HEMT when the transistor is grown on different substrates (sapphire, Si, SiC and diamond), and (ii) to investigate the influence of the TBR between the GaN-buffer and the substrate.

The paper is organized as follows. In section 2 we present the device details of the HEMT under analysis and a brief explanation of the used electro-thermal models. In section 3 we show the main results. Firstly, we study the effect of considering different substrates (sapphire, Si, SiC and diamond) in the absence of the TBR layer. Secondly, we also include the influence of the TBR layer. Finally, conclusions are summarized in section 4.

## 2. Device details and simulation methods

The layer structure and the geometry of the HEMT used as a reference are shown in figure 1. The distance between drain and source contacts is 1 $\mu$m. The structure consists of a 22 nm-thick un-doped $Al_{0.27}Ga_{0.73}N$ barrier layer on top of a 1.5 $\mu$m-thick un-doped GaN buffer grown on different substrates (sapphire, Si, SiC and diamond). In recent years, as one way to improve the 2DEG (two-dimensional electron gas) density, mobility, drain current [17] or to grow high-quality GaN on Si [18] in manufactured HEMTs, additional layers are included in the fabrication of transistors. Such layers have been disregarded in our simulations, but our simplistic and symmetric structure is a good choice to analyze in detail electron transport and thermal effects in GaN-based HEMTs. The gate (Schottky contact) is positioned in the middle of the structure in the same way as was done in other simulation works [19], and has a length of $L_g = 250$ nm. We highlight that typically the gate is shifted towards the source in order to decrease the electric field between the gate and the drain. However, the study performed in our symmetric structure does not lose generality because once the gate-source distance is large enough, it is the length between the gate and drain contacts which exerts the more significant influence on the thermal study. Our Schottky contact does not inject electrons and it only acts as a point of exit for electrons that are able to reach the electrode. Note that for the sake of generality the value of the gate-to-source bias $V_{GS}$ represented in the figures includes the applied voltage and the built-in potential, which typically is in the 0.5 V–1.5 V range (for different metal work functions) [20]. To simulate the AlGaN/GaN heterolayer correctly, we incorporate the influence of spontaneous and piezoelectric surface polarization charges; for our particular heterolayer $P = 14.12 \times 10^{16}\,\mathrm{m}^{-2}$ [21–24]. In addition, we incorporate a surface charge density $\sigma$ at the top of the AlGaN layer that appears as a result of polarization charges partially compensated by charges trapped at the surface states. A value of $\sigma = -4.12 \times 10^{16}\,\mathrm{m}^{-2}$ has been chosen since it provides a sheet electron density, $n_s = 1 \times 10^{17}\,\mathrm{m}^{-2}$ ($n_s = P - \sigma$), in the range of values found experimentally [25]. The conduction band of the materials is modelled by three, non-parabolic, spherical valleys. $\Gamma_1$, U and $\Gamma_3$ valleys are considered for wurtzite-GaN, as well as for AlGaN. The main parameters used in the simulation can be found in [26]. We include ionized impurities, phonons, piezoelectric and dislocations scattering, all of them having a significant influence on the GaN mobility. Fermi–Dirac statistics are incorporated in the simulator through the rejection technique [27]. A heat-sink at room temperature ($T = 300$ K) is located at the bottom of the structure.

The simulation method used in this paper (heat diffusion equation model, HDEM) iteratively couples the MC electronic transport with the solution of the steady-state heat-diffusion equation (HDE) [16] (where radiation and convection losses are neglected):

$$\nabla[k(r, T)\nabla T(r)] = -G(r), \qquad (1)$$

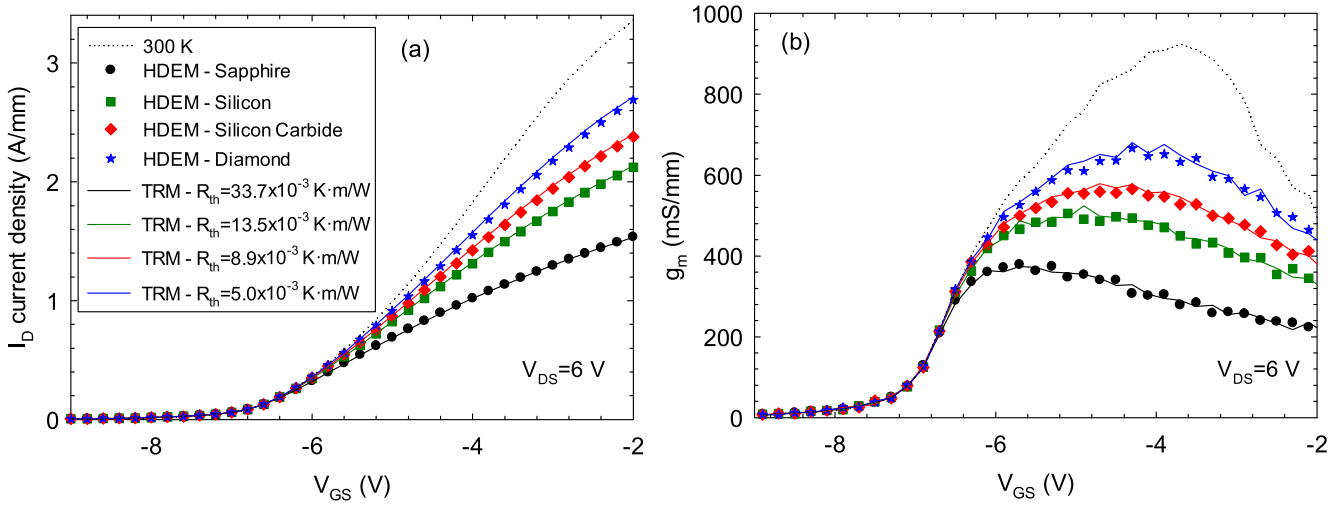


**Figure 2.** (a) Transfer characteristics of the current density $I_D$ versus $V_{GS}$. (b) Transconductance $g_m$ versus $V_{GS}$. The solid lines correspond to the results obtained with the TRM for the estimated thermal resistances.

where $T(r)$ and $G(r)$ are the temperature and the dissipated power density, respectively, at position $r$, and $k(r, T)$ is the temperature-dependent and inhomogeneous thermal conductivity. The thermal domain (region where the HDEM is applied), covers the whole device and is delimited by green dashed lines in figure 1. More details about the in-house electro-thermal simulator can be found in [16].

In addition, we have implemented a more simple procedure, called the thermal resistance method (TRM) [16]—similar to that used currently in circuit simulators [28]—in which the global temperature of the device varies at each operating point depending on the device power, $P_d$, according to:

$$T_{latt} = 300\ \text{K} + P_d \times R_{th}. \quad (2)$$

This model is based on the use of an ad hoc thermal resistance, $R_{th}$, and is only carried out in the electronic domain (region where the electronic transport is solved), delimited by yellow dashed lines in figure 1.

## 3. Results

In this section, we examine the effects of heating in the submicrometer HEMT of figure 1 using the two electro-thermal methods previously presented. The thermal conductivities of the different materials, at room temperature, are reported in table 1. Firstly, we will analyze the characteristic of the transistor by considering different substrates (sapphire, Si, SiC and diamond) without including the TBR layer. Secondly, we will incorporate the TBR.

### *3.1. Substrate effect*

We represent in figure 2(a) the drain current density $I_D$ versus the gate-to-source bias $V_{GS}$, and in figure 2(b) the transconductance $g_m$ versus $V_{GS}$, for a drain-to-source bias $V_{DS}$ equal to 6 V in both cases. For the sake of comparison, the results at the isothermal temperature of 300 K are also plotted. As expected, for all simulated substrates the pinch-off voltage is the same, independently of the substrate material. As the thermal conductivity of the substrate is lowered, a shift to more negative $V_{GS}$ values of the maximum of the transconductance, $g_{m,max}$, and a decrease $g_{m,max}$ are observed. $g_{m,max}$ takes the values of 379 mS mm$^{-1}$ ($V_{GS} = -5.7$ V), 506 mS mm$^{-1}$ ($V_{GS} = -5.1$ V), 565 mS mm$^{-1}$ ($V_{GS} = -4.3$ V), 666 mS mm$^{-1}$ ($V_{GS} = -4.3$ V) and 925 mS mm$^{-1}$ ($V_{GS} = -3.7$ V), for the sapphire, Si, SiC, diamond and for the isothermal simulation at 300 K, respectively. For $V_{GS} > -6.5$ V ($I_D > 300$–$400$ mA mm$^{-1}$) self-heating becomes crucial; the substrate with the lowest $k_s$ exhibits more significant heating effects in the drain current density level and $g_m$. Qualitatively, analogous results are found for lower $V_{DS}$ biasing. By means of the microscopic HDEM-MC simulations, we can evaluate the power density distribution generated by phonons, shown in figure 3(a) for the diamond substrate when $g_m$ is maximum. We remark that under these conditions electrons that mainly contribute to the current are not completely confined to the region very close to the heterojunction, but also expand into the GaN layer (with a deep of around 5 nm under the heterojunction), where the power density distribution is also observed (see zoom area of the gate-drain section). The maximum power density

**Table 1.** Values of the thermal conductivity at 300 K used in the simulation for the different materials.

| Material | $k^{300}$ (W · K$^{-1}$ · m$^{-1}$) |
|---|---|
| $Al_{0.27}Ga_{0.73}N$ | 30 [35] |
| GaN | 130 [36] |
| Polycrystalline SiC | 300 [6] |
| Si | 156 [37] |
| Au | 315 [37] |
| Diamond | 1000 [38] |
| Sapphire | 42 [19] |

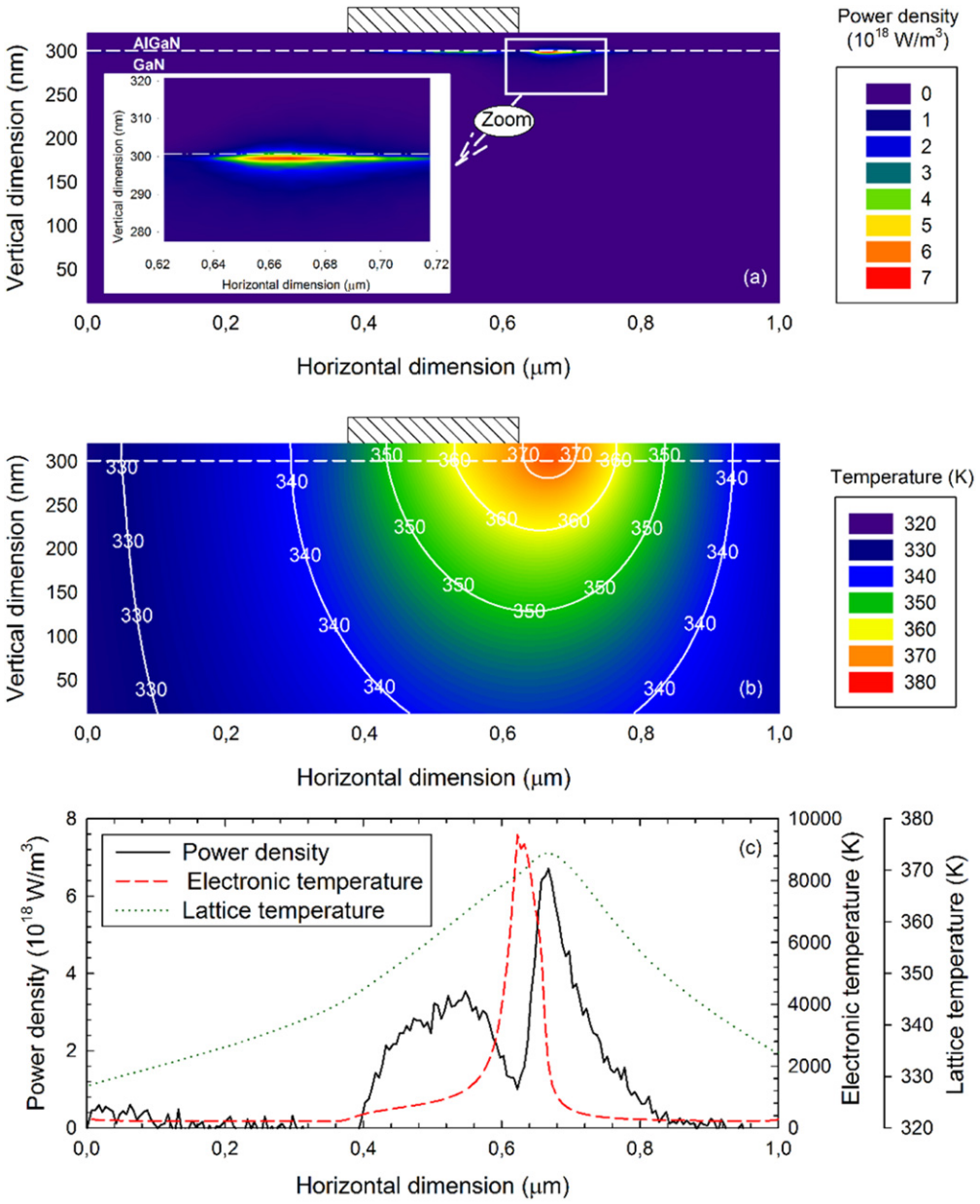


**Figure 3.** (a) Power density and (b) temperature distributions in the electronic domain, for $V_{DS} = 6$ V and $V_{GS} = -4.3$ V when the diamond substrate is employed. (c) Profiles of power density, electronic temperature and lattice temperature in the channel for the same bias conditions.

($6.71 \times 10^{18}$ W m$^{-3}$) is reached in the 2DEG-GaN of the HEMT at the drain side of the gate. The hot-spot can be found in the region where the power density takes its maximum value, reaching a temperature of 374 K, see figure 3(b). Note that in this device the average temperature ($T_{av}$) is 342 K. A more detailed analysis is carried out by studying the profiles of power density, lattice temperature and electronic temperature in the channel for the same bias conditions; see figure 3(c). The electronic temperature is calculated in a self-consistent way from the values of local carrier concentration and average energy at each valley by using the technique proposed in [29]. The electronic temperature is maximum in the region where the electric field takes its extreme value, at the drain edge of the gate. Here, transport is quasi-ballistic, and the emission of phonons decreases significantly, as observed in figure 3(c), then increases a lot towards the drain once the electric field is smaller, thus leading to the hot spot of the device. In figure 4(a) we analyze the average temperature versus the dissipated power at $V_{DS} = 6$ V. As expected, for all substrates the higher the $V_{GS}$ (larger dissipated power inside the device) the higher the $T_{av}$. At the bias conditions of $g_{m,max}$ for each substrate, the values of $T_{av}$ are 382 K (sapphire), 362 K (Si), 368 K (SiC) and 342 K (diamond), respectively. Note that $g_{m,max}$ is higher for SiC than for Si, but the $T_{av}$ for SiC is 6 K bigger. This is due to the shift of the $V_{GS}$ to higher values in SiC, leading to higher dissipated power. We have found that $T_{av}$ is linear with respect to the dissipated power, so that we can extract the slope of this linear fitting and define an

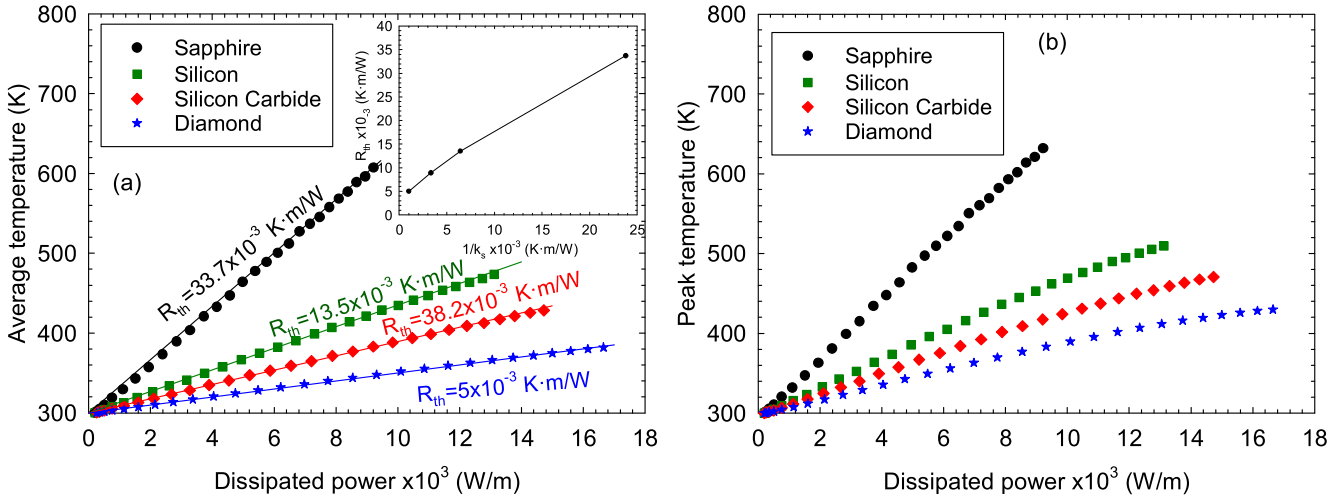


**Figure 4.** (a) Average temperature versus dissipated power and linear fitting to extract the corresponding thermal resistance. (b) Peak temperature versus dissipated power. In both graphs $V_{DS} = 6$ V. The inset shows $R_{th}$ versus $1/k_s$.

equivalent thermal resistance $R_{th}$ as shown in [16]. In figure 4(a) the extracted values of $R_{th}$ are indicated: $R_{th} = 33.7 \times 10^{-3}$ K · m/W, $R_{th} = 13.5 \times 10^{-3}$ K · m/W, $R_{th} = 8.9 \times 10^{-3}$ K · m/W, and $R_{th} = 5 \times 10^{-3}$ K · m/W for sapphire, Si, SiC and diamond, respectively. $R_{th}$ decreases with $k_s$ and its dependence is almost linear, see inset of figure 4(a). By means of the TRM with the mentioned extracted values of $R_{th}$ (from figure 4(a)) we obtain the same transfer characteristics and transconductance as those provided by the HDEM, as can be seen by the solid lines of figures 2(a) and (b). Thus, we conclude that the electronic behavior of the devices is dominated by the average temperature, which fixes the level of the current, and not by $T_p$. As observed, both models, HDEM and TRM, provide the same behavior, but we wish to highlight the importance of the HDEM in previously extracting an accurate value of $R_{th}$ to be used in the TRM. In figure 4(b), the peak temperature ($T_p$) versus the dissipated power at $V_{DS} = 6$ V is depicted. As with the average temperature, as $V_{GS}$ is bigger, the peak temperature increases. We analyze the particular case where $g_m$ is maximum. The values of $T_p$ at $g_{m,max}$ are 390 K, 380 K, 398 K and 374 K for the sapphire, Si, SiC and diamond substrates, respectively. The values of the predicted temperatures are in accordance with experimental observations. Temperatures in the 370 K–630 K, 300 K–360 K, and 300 K–330 K ranges were measured in AlGaN/GaN HEMTs ($L_g = 0.25$ $\mu$m) grown on sapphire [30], SiC [31] and diamond [31], respectively. In addition, temperatures in the 350 K–450 K and 300 K–490 K ranges are measured in HEMTs grown on Si [30] and SiC [32], with gate-lengths of 0.45 $\mu$m and 0.5 $\mu$m, respectively. It is striking that the difference between the peak and average temperatures ($T_p$-$T_{av}$) increases with the substrate thermal conductivity: 8 K, 18 K, 30 K and 32 K, for sapphire, Si, SiC and diamond substrates, respectively. In addition, note that the change between SiC and diamond is only 2 K. The large difference ($T_p$-$T_{av}$) in devices grown on good (high $k_s$) substrates could generate unexpected failures in their performance and cause the HEMTs to burn out. We finally remark that the difference between the values of $T_{av}$ obtained for sapphire and diamond is 40 K, whilst that in $T_p$ is only 16 K.

Techniques like the HDEM can be of great help to prevent abrupt temperature gradients and physically locate the hot-spots in the regions where the dissipated power is extremely high. Note that these effects cannot be studied with the traditional models based on a thermal resistance.

### 3.2. Thermal boundary resistance effect

The TBR plays an important role in the heat transfer because it blocks the dissipation of the heat originated by phonons [33, 34]. In our model, the effect of the TBR is accounted for by introducing a thin virtual layer (thickness $\Delta_{TBR}$) with a given low thermal conductivity, $k_{TBR}$, between the GaN-buffer and the substrate (see figure 1), in the same way as proposed in [33, 34]. The length $L_2$ (substrate thickness) will thus be 300 $\mu$m-$\Delta_{TBR}$. In this framework, the value of the simulated TBR is:

$$\mathrm{TBR} = \Delta_{TBR}/k_{TBR} \tag{3}$$

Typically, the thickness of the TBR layer $\Delta_{TBR}$ is of the order of nm. If this thickness is small enough with respect to the thickness of the rest of the layers, given a constant TBR, its effects can be introduced in the simulations by adjusting the pairs $\Delta_{TBR}$ and $k_{TBR}$. This fact is shown in figure 5, where we consider several pairs of values of $\Delta_{TBR}$ and $k_{TBR}$, providing the same TBR ($15 \times 10^{-8}$ m$^2$ · K/W) according to equation (3). We explore the profile of the lattice temperature close to the TBR region in the middle of the transistor depicted on figure 1 for a bias $V_{GS} = -4.2$ V and $V_{DS} = 6$ V. The results provided by the sets ($\Delta_{TBR} = 15$ nm, $k_{TBR} = 0.1$ W/(K · m)), ($\Delta_{TBR} = 9$ nm, $k_{TBR} = 0.06$ W/(K · m)), ($\Delta_{TBR} = 6$ nm, $k_{TBR} = 0.04$ W/(K · m)) and ($\Delta_{TBR} = 3$ nm, $k_{TBR} = 0.02$ W/(K · m)) are shown in figure 5. Note that the temperature discontinuity is 54 K in all four cases. Hereinafter, a layer of thickness $\Delta_{TBR} = 15$ nm is included at the buffer–substrate interface. Simulations were

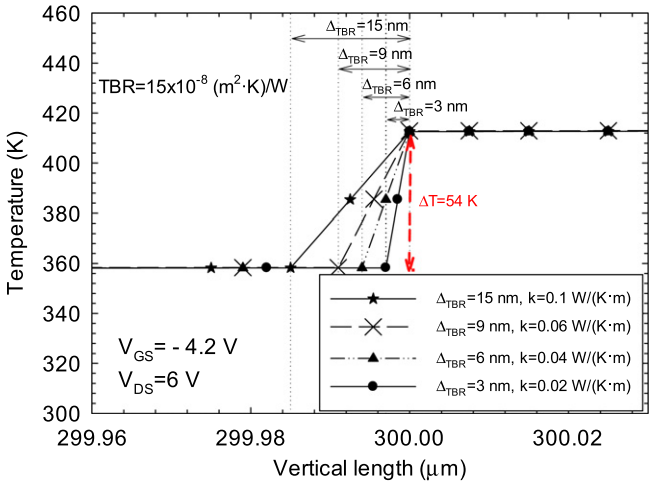


**Figure 5.** Profile of the lattice temperature in the middle of the transistor (grown on Si) close to the TBR region, for a bias of $V_{GS} = -4.2$ V and $V_{DS} = 6$ V when we consider TBR $= 15 \times 10^{-8}\,m^2 \cdot K/W$. Pairs of values of $\Delta_{TBR} = 15$ nm, $k_{TBR} = 0.1\,W/(K \cdot m)$; $\Delta_{TBR} = 9$ nm, $k_{TBR} = 0.06\,W/(K \cdot m)$; $\Delta_{TBR} = 6$ nm, $k_{TBR} = 0.04\,W/(K \cdot m)$ and $\Delta_{TBR} = 3$ nm, $k_{TBR} = 0.02\,W/(K \cdot m)$ are used.

performed by considering three temperature-independent thermal conductivities ($k_{TBR}$) of 1, 0.1 and $0.03\,W/(K \cdot m)$ for this layer. Therefore, according to equation (3), the TBR is equal to $1.5 \times 10^{-8}$, $15 \times 10^{-8}\,m^2 \cdot K/W$ and $50 \times 10^{-8}\,m^2 \cdot K/W$, respectively. These values are in the range of those reported experimentally [10–12]. The TBR for GaN on sapphire has been suggested to be higher than for SiC and Si because the interface between the epitaxial layers and the substrate contains nucleation layers and areas with a high concentration of defects and impurities [10]. In this section we analyze the effect of the TBR in devices fabricated on sapphire, Si, SiC and diamond substrates.

In figures 6(a) and (b), we plot for the sapphire and diamond substrates the curve $I_D$ versus $V_{GS}$ and the transconductance, respectively, for $V_{DS} = 6$ V and for the three values of the TBR mentioned above. In addition, the case without the TBR layer is included for the sake of comparison. Sapphire is less sensitive to the changes in the TBR. We observe that the current density does not vary significantly when the TBR layer is included, even for a high TBR of $50 \times 10^{-8}\,m^2 \cdot K/W$. In all cases, the maximum of the transconductance is reached at $V_{GS} \sim -5.7$ V and the difference between $T_p$ and $T_{av}$ is nearly constant (~8 K). In contrast, the device with the diamond substrate is much more sensitive to the changes in the TBR. In this case, the TBR causes a strong reduction in the current density, especially with high-dissipated powers, being more pronounced when the value of the TBR increases. As the TBR is bigger, a shift of the maximum of $g_m$ to lower $V_{GS}$ and a decrease in the maximum of $g_m$ are observed, because of the heating effects. The maximum of $g_m$ takes the values of $666\,mS\,mm^{-1}$ ($V_{GS} = -4.3$ V), $615\,mS\,mm^{-1}$ ($V_{GS} = -4.3$ V), $508\,mS\,mm^{-1}$ ($V_{GS} = -4.7$ V) and $438\,mS\,mm^{-1}$ ($V_{GS} = -4.9$ V) for the case without TBR, TBR $= 1.5 \times 10^{-8}\,m^2 \cdot K/W$, TBR $= 15 \times 10^{-8}\,m^2 \cdot K/W$ and TBR $= 50 \times 10^{-8}\,m^2 \cdot K/W$, respectively. A detailed inspection of the simulation results for this substrate shows that the value of ($T_p$-$T_{av}$) is much higher than for sapphire due to the better thermal conductivity. In the absence of TBR, $T_p$-$T_{av} \sim 32$ K for the diamond substrate where $g_m$ takes its maximum value. When TBR increases, the beneficial effect of a good thermal substrate is canceled, and $T_p$-$T_{av}$ decreases due to the impossibility of draining all the heat generated by the device. We highlight again the importance of the HDEM versus the traditional models based on a thermal resistance for the analysis of the peak temperature as this value would be able to influence the performance of our devices.

In figures 7(a) and (b), we analyze $T_{av}$ versus $P_{diss}$ for sapphire and diamond substrates. Obviously, at a given dissipated power, the diamond based device exhibits lower temperatures than sapphire. However, and especially for the diamond substrate, the value of $R_{th}$ is strongly affected by the TBR. Figures 7(c) and (d) show the profiles of lattice temperature in the middle of the structures at the vicinity of the

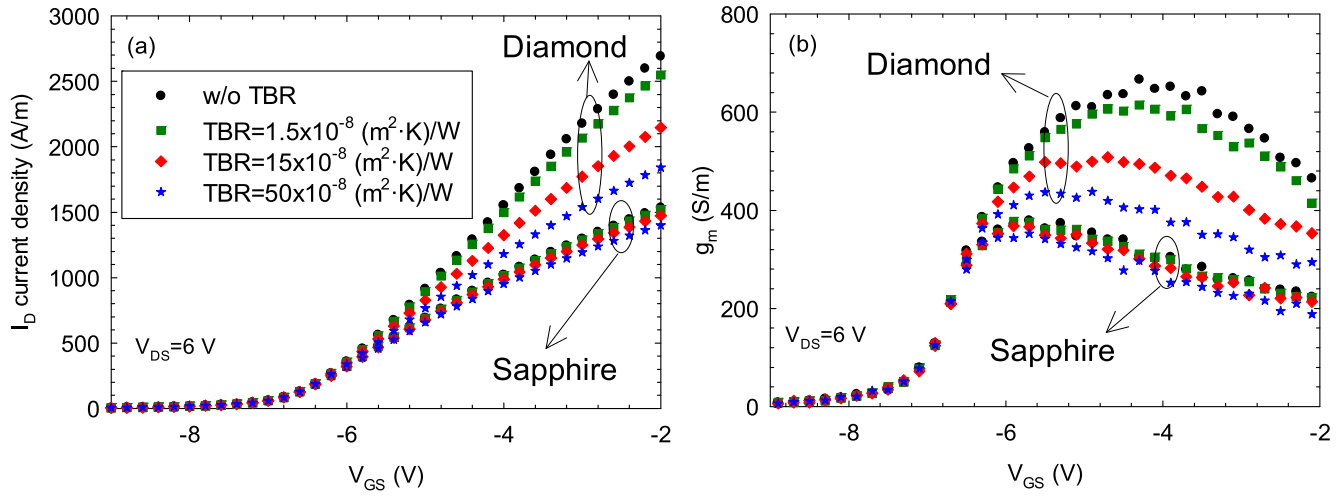


**Figure 6.** (a) Transfer characteristics. (b) Transconductance $g_m$ versus $V_{GS}$. A TBR layer of $\Delta_{TBR} = 15$ nm with $k_{TBR} = 1\,W/(K \cdot m)$, $0.1\,W/(K \cdot m)$ and $0.03\,W/(K \cdot m)$ is studied; the TBR is equal to $1.5 \times 10^{-8}$, $15 \times 10^{-8}$ and $50 \times 10^{-8}\,m^2 \cdot K/W$, respectively. The case without the TBR layer is included for the sake of comparison. Sapphire and diamond substrates are analyzed.

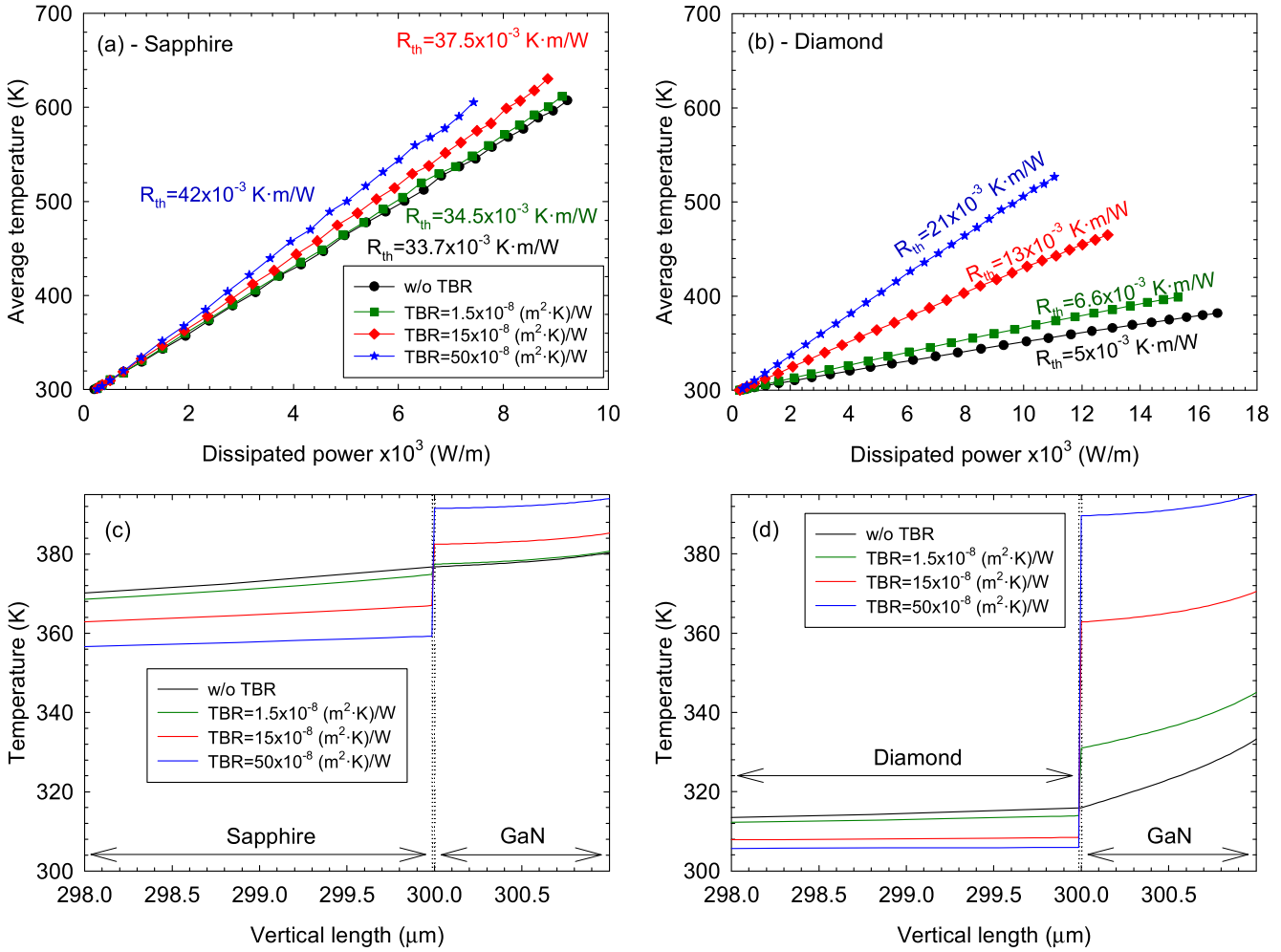


**Figure 7.** $T_{av}$ versus $P_{diss}$ for (a) sapphire and (b) diamond. A TBR layer of $\Delta_{TBR} = 15$ nm with $k_{TBR} = 1$ W/(K · m), 0.1 W/(K · m) and 0.03 W/(K · m) is studied; the TBR is equal to $1.5 \times 10^{-8}$, $15 \times 10^{-8}$ and $50 \times 10^{-8}$ m$^2$ · K/W, respectively. The case without the TBR layer is included for the sake of comparison. Profiles of the lattice temperature in the middle of the transistor close to the TBR region for the bias at which the transconductance takes its maximum value: (c) sapphire ($V_{GS} = -5.7$ V) and (d) diamond ($V_{GS} = -4.3$ V, $-4.3$ V, $-4.7$ V and $-4.9$ V for the case without TBR, TBR = $1.5 \times 10^{-8}$ m$^2$ · K/W, $15 \times 10^{-8}$ m$^2$ · K/W and $50 \times 10^{-8}$ m$^2$ · K/W, respectively). In both graphs $V_{DS} = 6$ V.

buffer–substrate interface for the bias corresponding to $g_{m,max}$. Note that the discontinuity $\Delta T$ at the interface increases when a higher conductivity substrate is chosen. By way of example, the discontinuity $\Delta T$ in the TBR layer is 2.6 K, 15.5 K and 32.5 K (for the sapphire) and 17 K, 55 K and 84 K (for the diamond) for the TBR values of $1.5 \times 10^{-8}$ m$^2$ · K/W, $15 \times 10^{-8}$ m$^2$ · K/W, and $50 \times 10^{-8}$ m$^2$ · K/W, respectively. The consequences of the TBR are also reflected in the extracted values of $R_{th}$, which are in the 33–37 $\times 10^{-3}$ K · m/W and 5–21 $\times 10^{-3}$ K · m/W ranges for sapphire and diamond, respectively. A more detailed study of the effect of the TBR for the four substrates (sapphire, Si, SiC and diamond) is summarized in figure 8. In all cases $R_{th}$ increases with TBR, but the dependence is not linear. Remarkably, it may occur that a device grown on a substrate with poor $k_s$ but with a good thermal interface resistance (low TBR) exhibits better thermal behavior than another grown on

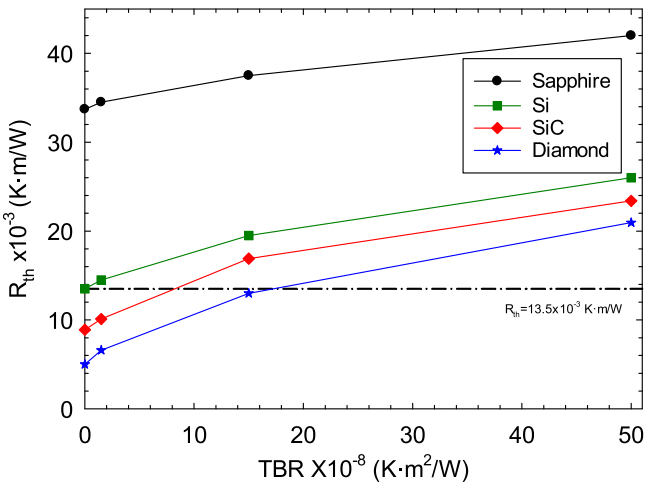


**Figure 8.** $R_{th}$ versus TBR when the device is grown on sapphire, Si, SiC and diamond.

a substrate with an excellent $k_s$ but with a high TBR. By way of example, identical $R_{th}$ ($13.5 \times 10^{-3}$ K · m/W), dash-dot line, can be extracted from our simulations if Si (without TBR), SiC (with TBR = $8.22 \times 10^{-8}$ m$^2$ · K/W) or diamond (with TBR = $17 \times 10^{-8}$ m$^2$ · K/W) are employed.

## 4. Conclusions

In this paper, we have analyzed the effect of growing an AlGaN/GaN HEMT over different substrates (sapphire, Si, SiC and diamond) and the influence of the TBR on their performance. To that end, an in-house electro-thermal MC simulator has been used. We have confirmed the advantages of the HDEM versus simple models based on a thermal resistance (TRM). Firstly, the HDEM allows us to extract the proper equivalent $R_{th}$ for each geometry. Another advantage of the HDEM is that this model provides a local temperature map, and it is able to identify the position and the temperature of hot-spots inside the HEMT, always located at the drain side of the gate. Devices grown on substrates with higher $k_s$ in the absence of TBR (or under the effect of low TBR) provide a more significant difference ($T_p$-$T_{av}$). A peak temperature far beyond the average temperature could cause sudden failures in the performance of the device. The temperatures obtained through the MC simulations are in accordance with experimental measurements. On the one hand, although the temperature varies in the electronic domain, it seems that the electronic transport of the devices is dominated by the average temperature. This is confirmed by using the extracted $R_{th}$ value within a TRM because the simulation results are the same as the HDEM ones. On the other hand, $g_{m,max}$ is always shifted to more negative $V_{GS}$ when a substrate with lower thermal conductivity is employed, but the value of $g_{m,max}$ is not necessary linked to the lower average temperature. In addition, the higher $k_s$, the greater TBR effect because a superior temperature discontinuity in the TBR layer appears.

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