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Operation and high-frequency performance of nanoscale unipolar rectifying diodes

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By means of the microscopic transport description supplied by a semiclassical two-dimensional Monte Carlo simulator, we provide an in depth explanation of the operation (based on electrostatic effects) of the nanoscale unipolar rectifying diode, so called self-switching diode, recently proposed in A. M. Song, M. Missous, P. Omling, A. R. Peaker, L. Samuelson, and W. Seifert, Appl. Phys. Lett. **83**, 1881 (2003). The simple downscaling of this device and the intrinsically high electron velocity of InGaAs channels allows one to envisaging the fabrication of structures working in the THz range. We analyze the high-frequency performance of the diodes and provide design considerations for the optimization of the downscaling process. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1931051]

A nanoscale unipolar rectifying diode based on electrostatic effects [so called self-switching diode (SSD)], was recently proposed in Ref. 1. This device provides an attractive rectifying current-voltage (*I-V*) characteristic without the use of any doping junction or barrier structure. Moreover, its threshold voltage can be tuned from almost zero to more than 10 V by adjusting the channel width and other geometric parameters. The simplicity of the technological process used for the fabrication of these diodes is also remarkable, since it only involves the etching of insulating trenches on a semiconductor surface (a single step of high-resolution lithography). The downscaling of SSDs is so simple that, together with the intrinsically high electron velocity in some material systems, like those involving InGaAs channels, the fabrication of devices working in the THz range can be envisaged.

The basic operation of SSDs has been explained just in terms of the opening of the channel due to the accumulation of charges in the surrounding regions.[1] A detailed microscopic analysis of the behavior of this device is essential to improve its performance. In this work, we will make use of a semiclassical two-dimensional (2D) Monte Carlo (MC) simulation [(employed in previous works for the modelling of different types of InGaAs-based nanodevices: T- and Y-branch junctions and ballistic rectifiers)[2–4]] to explain the physics of the self-switching operation in InAlAs/InGaAs-based SSDs. We will mainly focus on the high-frequency operation of SSDs in order to optimize the downscaling process.

The modeling of these devices would require a three-dimensional simulation to exactly describe the influence of the lateral surface charges and the actual layer structure. For simplicity, a 2D MC model will be used, where some assumptions, described in Refs. 2–4, are made. The real layer structure of the device is not included in the (top-view) simulations and only the InGaAs channel is considered. To account for the fixed positive charges of the whole layer structure, a net background doping N_{Db} is assigned to the channel, but impurity scattering is switched off; in this way, the electron transport through the undoped channel is well described. On the other hand, a negative surface charge density σ is assigned to the semiconductor-air interfaces to account for the influence of the surface states. Finally, since contact injection is a critical point when dealing with ballistic transport, the velocity distribution and time statistics of injected carriers will be accurately modeled following Ref. 5, and characterized by the carrier density of the injecting contacts N_c. The 2D top-view simulations of the SSDs are performed by considering a contact density $N_c=10^{17}$ cm^{-3}, a background doping $N_{Db}=10^{17}$ cm^{-3}, and a surface charge density $\sigma=0.3\times10^{12}$ cm^{-2}. The nonsimulated dimension Z (which allows the comparison of the simulated values of current with those measured in real devices) was estimated as $Z=n_s/N_{Db}=10^{-5}$ cm, with $n_s=10^{12}$ cm^{-2}, typical value of sheet electron density in InGaAs channels.[1]

We have simulated SSDs with the geometry shown in the inset of Fig. 1, and different channel widths W. The thickness of the lateral trenches has been reduced with respect to that of the fabricated devices reported in Ref. 1 in order to achieve a better charge control in the channel. The main findings in the *I-V* curves of experimental devices are

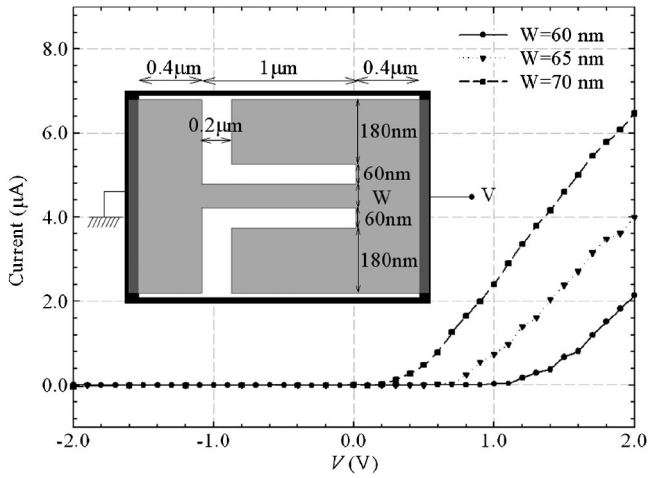

FIG. 1. *I-V* curves of the devices with the geometry shown in the inset and different values of channel width W.

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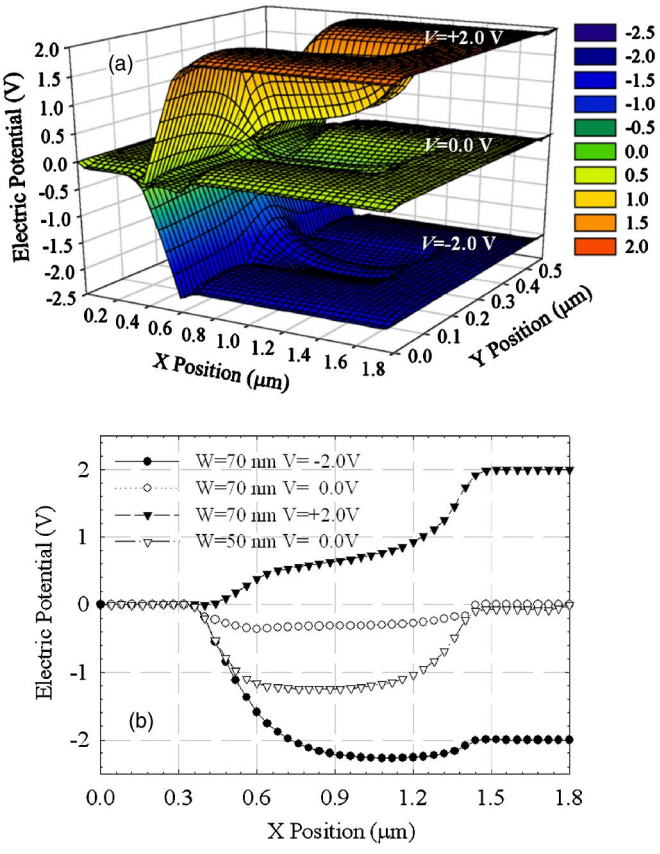

FIG. 2. Electric potential in the SSD of Fig. 1 with $W=70$ nm for applied voltages $V=-2.0$ V, 0.0 V, and +2.0 V: (a) 2D chart and (b) one-dimensional profile along the channel. The equilibrium case for the SSD with $W=50$ nm is also plotted in (b).

well reproduced by the MC results reported in Fig. 1, namely, the current rectification and the increase of the threshold voltage when the channel is narrowed. This behavior can be explained in terms of the internal quantities provided by MC simulations. Figure 2 shows the electric potential inside the SSD with $W=70$ nm for $V=+2.0$ V, 0.0 V, and -2.0 V. It can be observed that the voltage applied to the anode (right contact) propagates to the vicinity of the channel, while in the cathode region (at the left of the trenches) the potential is always essentially zero. In equilibrium, the channel is closed due to the depletion induced by the surface charges located at the lateral walls, which lead to the appearance of the longitudinal potential barrier observed in Fig. 2(b). When $V>0$, the positive voltage reaches the lateral regions of the SSD channel, so that the potential barrier is lowered (or even removed, as observed for $V=2.0$ V), thus allowing the electron flow (the channel is open). On the contrary, when $V<0$ the potential profile in the right part of the device is almost unchanged with respect to the equilibrium situation (it is just shifted to lower values), the channel thus remaining closed. This evolution can be better appreciated in Fig. 2(b), where the potential profile along the center of the channel is plotted for different applied voltages. For $V=0.0$ V and $V=-2.0$ V, the potential barrier obstructing the electron flow is present in both directions, while for $V=2.0$ V it has disappeared for carriers going from cathode to anode, thus allowing the increase of the current. As observed in Fig. 2(b) in the equilibrium case, the height of the barrier becomes larger when the channel is narrowed, so that the threshold voltage needed to switch on conduction is higher,

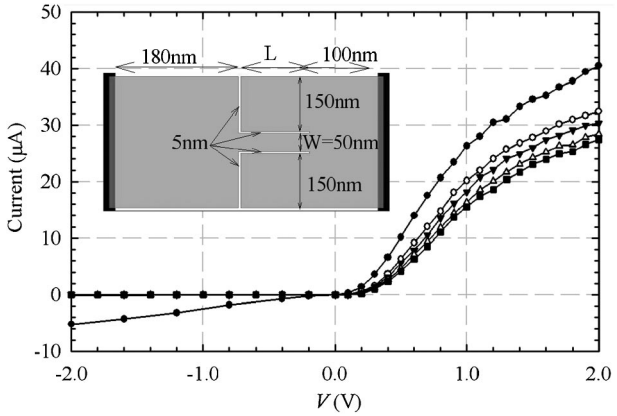

FIG. 3. *I-V* curves of SSDs with the geometry shown in the inset ($W=50$ nm, 5 nm wide trenches) for different channel lengths L.

thus explaining the behavior of the *I-V* characteristics shown in Fig. 1. Therefore, the operation principle of this device is similar to that of an enhanced mode field effect transistor (pinched off at equilibrium) in which lateral gates (in this case short circuited to the drain) control the current flow through the channel.

It is important to remark that the operating principle of SSDs, unlike other semiconductor nanodevices (T- and Y-branch junctions, ballistic rectifiers),[6–8] is not based on ballistic transport or high mobility, and therefore SSDs could also be fabricated on Si, thus taking advantage of the well-established Si technology. However, when downscaling the size of SSDs fabricated on high mobility materials, the high-frequency performance of the devices can be dramatically improved thanks to a much shorter transit time, due not only to the shorter channel length but also to the enhanced electron velocity associated with ballistic transport. The *I-V* curves of SSDs with $W=50$ nm and different channel lengths (ranging from $L=1.0$ μm to $L=100$ nm) are shown in Fig. 3. In order to further optimize the current control of SSDs, we have reduced the width of the trenches to 5 nm (near the limits of up-to-date technology), so that the potential applied to the right contact affects more strongly the population of the channel. As observed in the figure, short-channel effects (comparable to those found in traditional field effect transistors) appear when the aspect ratio of the channel (L/W) decreases. In such a case, under inverse bias, the potential of the lateral regions may not be able to deplete the channel, so that the barrier preventing the current flow disappears and an inverse leakage current flows (as observed for $L=100$ nm). This may happen because of a too wide channel or too wide lateral trenches. The very thin trenches of the devices analyzed in Fig. 3 not only prevent the presence of inverse leakage current for very short channels (it only appears for $L=100$ nm), but also the forward current is much improved. For high applied voltages, a tendency to saturation associated with hot-carrier effects is observed in the current.

The dynamic behavior of these optimized devices can be tested by means of the MC simulation of their response to sinusoidal input voltage signals of increasing frequency. Figure 4 shows the time-dependent current in the SSDs of Fig. 3 with $L=100$ nm and $L=300$ nm for input voltages with an amplitude of 0.5 V and different frequencies (100 GHz, 0.5 THz, and 1 THz). The displacement current associated with the variation of the applied voltage is not considered

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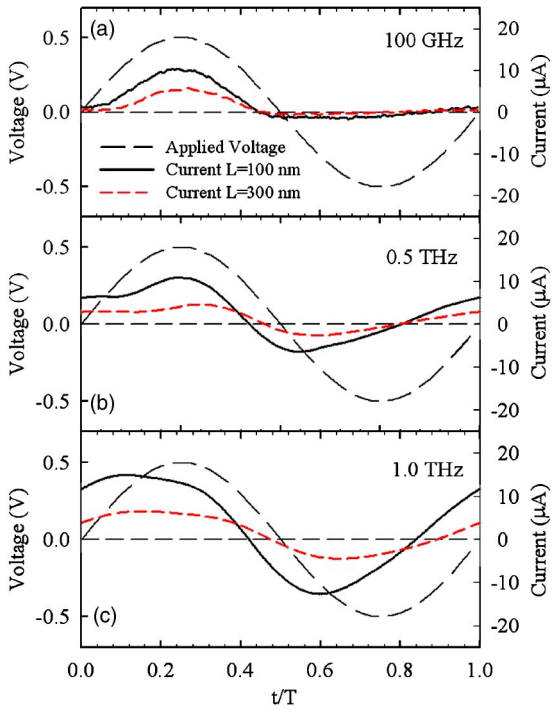

FIG. 4. Current response to sinusoidal input voltages (also shown) with amplitude of 0.5 V and frequencies of (a) 100 GHz, (b) 0.5 THz, and (c) 1.0 THz applied to the SSDs of Fig. 3 with channel lengths of $L=100$ nm and $L=300$ nm.

here since its average value is null, and for high frequency it conceals the overall current response. For 100 GHz, the rectification is quite good (nearly following the static behavior), the shorter structure exhibiting a higher forward current even if a small inverse conduction is present, as expected from the static *I-V* characteristics. When increasing the frequency of the applied signal (0.5 and 1.0 THz), the shape of the current is degraded and a dephase in the response appears, but it still shows a positive average value. This is better observed in Fig. 5, where the mean value of the current is represented as

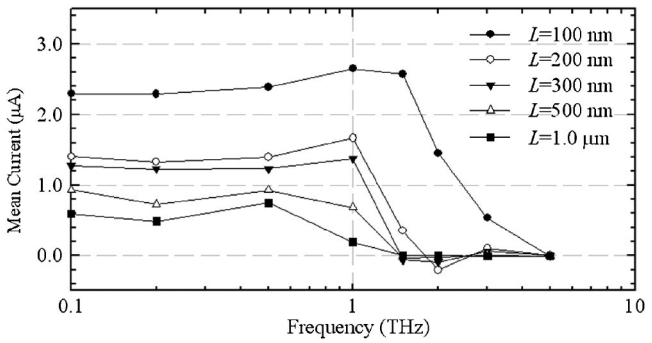

FIG. 5. Mean response current vs frequency of the periodic input voltage (with amplitude of 0.5 V) applied to the SSDs of Fig. 3.

a function of the frequency of the periodic input voltage. As expected, the cut-off frequency of the rectifying behavior of SSDs depends on the channel length, being lower for longer channels. The current overshoot observed in Fig. 4(c) leads to an increase in the dc response for input signal frequencies around 1 THz (Fig. 5). This overshoot comes from a kind of resonance originated, when transport is ballistic, by the coincidence between the transit time of electrons and the period of the applied signal. In fact, only for ballistic channels ($L<300$ nm) an increase of dc response is observed before its decay, while the diffusive ones show a normal cutoff (Fig. 5). The structure with $L=100$ nm is correctly responding up to frequencies over 2.0 THz, thus making possible the operation of these devices as, for example, power detectors of THz waves.[9] However, we have to note that these intrinsic high-frequency capabilities are likely to be deteriorated by the extrinsic contact resistances and capacitances. Therefore, strong efforts (both at technologic and design levels) must be made to minimize their effect.

In conclusion, we have explained the operating principle of SSDs by means of MC simulations, showing that the performance of these devices can be optimized by reducing the channel length and the thickness of the trenches used to define their topology. If correctly designed, the intrinsic cut-off frequency of an optimized SSD can reach the THz range. Even if a worse dynamic performance can be expected, SSDs could also be fabricated with Si technology reaching very high frequencies, possibility that we plan to explore in the future.

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