Abstract—This letter presents a first successful integration of a high-k dielectric, Al₂O₃, with III-V semiconductors in ballistic deflection transistors (BDT). The Al₂O₃ is deposited by means of atomic layer deposition allowing the formation of uniform layers along the walls of etched trenches. The BDT transfer characteristic shows a strong dependence on the dielectric permittivity of the material filling the etched trenches. The transconductance of the BDT is enhanced and shifted to lower gate bias when the Al₂O₃ is deposited in the trenches. Moreover, the ratio between output and leakage currents was also enhanced.

Index Terms—high-k dielectric, III-V semiconductors, nanodevices.

I. INTRODUCTION

Room temperature (RT) ballistic devices have emerged as possible candidate to fabricate high speed circuits for analog and digital applications [1]. Advance methods like focused ion beam and e-beam lithography (EBL) allow us to “write” insulating lines to strategically define shapes and edges in semiconductor heterostructures [2, 3]. Two devices which exhibit nonlinear electrical properties at RT are: Ballistic Rectifier [4] and Y-Branch Junction [5, 6]. In the same context, based on the pioneer work [7], we proposed a novel Ballistic Deflection Transistor (BDT) [8]. BDT has positive and negative transconductance regions, which enable inverting or non-inverting circuits depending only on gate offset voltage [9]. The non-linear transfer characteristic makes the BDT an ideal frequency doubler [10] and it provides logic capability [11, 12]. Monte Carlo (MC) simulations estimated a maximum operation of 400 GHz at RT as frequency doubler [12].

In the BDT, the presence of a confined electric field parallel to the 2DEG can be used to improve the electrostatic coupling between gate and the channel through the dielectric trenches. In this letter, we integrate InGaAs/InAlAs/InP with Al₂O₃, a high-k dielectric, and study the performance of the BDT in terms of its transconductance (gm) and leakage. The deposition of Al₂O₃ in the trenches enhances the capacitive coupling, which increases the gate control over the channel conduction. Gate control can also be increased by reducing the trench width, but it increases the gate leakage significantly.

II. BDT DESCRIPTION AND IMPORTANCE OF HIGH-K

Fig. 1(a) shows the heterostructure of BDT. BDT consists of lattice matched InGaAs and InAlAs layers on an InP substrate. In particular, a 450 nm InAlAs buffer layer, a 50 nm InGaAs channel layer, 20 nm of InAlAs spacer layer followed by a planar silicon δ-doped (Nδ=2×10¹² cm⁻²) InAlAs layer, a 30 nm Schottky barrier layer and finally a 10 nm InGaAs undoped cap layer. The measured RT mobility μ and sheet electron density nₛ of 2DEG were 1.1×10⁶ cm²/Vs and 1×10¹² cm⁻², respectively. The BDT is a six-terminal coplanar structure fabricated by etching into an InGaAs 2DEG with dimensions of the order of the mean free path (~ 200 nm [1]) at RT, so that transport exhibits quasi-ballistic features. It consists of a grounded source, left and right gates, and three biased drains depicted in the 3D image of Fig. 1(a). The gate control over the channel can be attributed to three effects, classic channel pinch-off due to field effect, electron steering due to gate bias and deflection due to a deflector. A detailed explanation of the principle of operation can be found in Ref. 13.

The functionality of in-plane gates has already been demonstrated [7]. Recently incorporation of high-k dielectrics into III-V heterostructure devices has been reported [14]. A very recent work shows that by spin-coating a high-k dielectric material onto nanodevices (based on ZnO) enables a higher degree of control over the channel conductance [15]. In addition, MC and TCAD-Medi simulations have shown that the device performance is very sensitive to the depth of insulating trenches and the presence of dielectric layers on the device surface [16, 17]. However, experimentally, high-k dielectric has never been used to fill the trenches in III-V ballistic planar devices. Based on our previous MC results on BDTs [9], we expect that the use of high-k dielectrics (Al₂O₃, HfO₂ or HfAlO) will result in a significant drop in the pinch off voltage and improved transconductance due to higher capacitance in the trenches and better gate-channel coupling.

Vikas Kaushal, Ignacio Íñiguez-de-la-Torre, Tomás González, Senior Member, IEEE, Javier Mateos, Member, IEEE, Bongmook Lee, Veena Misra, and Martin Margala, Senior Member, IEEE

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For the realization of a BDT, a two step EBL is employed. For the first step, a positive resist 950K PMMA (~170 nm) is spun over a 40 nm Si₃N₄ hard mask before the ICP-RIE was done to define the active region of 2DEG layer. The resulting mesa typically has a step height of 130 nm so that all the layers above InAlAs buffer are completely etched away. For the second step of fabrication, EBL is used again to pattern contacts, which are formed using a standard Ni-Ge-Au stack that was annealed at 420 °C for 30 sec. The metal layer thickness and the annealing temperature have been optimized, giving an acceptably low contact resistance (~0.2 Ω·mm).

Al₂O₃ dielectric film was deposited by Atomic Layer Deposition (ALD) at 200 °C of substrate temperature. ALD Al₂O₃ is a high-quality dielectric on III-V compound semiconductors widely used due to its excellent dielectric properties, strong adhesion to dissimilar materials, high thermal / chemical stabilities and low defect density. Al₂O₃ has a high band gap (~9 eV), a high breakdown electric field (5–30 MV/cm) and a high permittivity (8.6–10). The base pressure of ALD chamber was 400 mTorr with constantly flowing N₂ carrier gas. Trimethylaluminum was used as Al precursor and water was used as a reactant. The ALD Al₂O₃ film can be uniformly deposited at the bottom and at the side walls of the trenches, thus modulating the air trench width. The resulting width of the trench (initially t) after Al₂O₃ deposition (d at both sides) is t–2×d. The idea is to study the coupling effect on the device performance by depositing different thicknesses of Al₂O₃ in the trenches of devices with diverse trench and channel widths. The air trench width chosen is 100 nm. 35 nm and 50 nm of Al₂O₃ layers were deposited atomically, which resulted into 30 nm and 0 nm of air trenches and 70 nm and 100 nm of Al₂O₃ trenches, respectively. SEM images of the devices are shown in Fig. 1(b), (c) and (d).

IV. EXPERIMENTAL RESULTS

Two main effects occur when a high-k dielectric is deposited in the trenches of BDT. First is the generation of surface states at the interface of Al₂O₃ and III-V, which degrades mobility due to an increase in the interface traps, and second is the increase of gate-channel coupling due to an increase in the capacitance in the trenches. Both of these effects reduce the channel current (I_LD).

Downscaling BDT from c=200 nm to 140 nm, it is observed from Fig. 2(a) that downscaling BDT from c=200 nm to 140 nm increases the output current per unit length and leads to an earlier pinch off. Fig. 2(b) shows a slight increase in g_m from c=200 nm to c=140 nm. It is thus confirmed that an increase in g_m can be achieved by either depositing high-k dielectrics in the trenches or by downscaling the devices.

The two main leakage sources in the BDT are the gate leakage (I_{GD}) and the top drain leakage (I_{TD}). We saw from the inset of Fig. 2(a) that the deposition of Al₂O₃ in the trenches does not increase the gate leakage significantly. To enhance the performance of BDT, it is imperative that the leakage through the top drain doesn’t increase with Al₂O₃ deposition. Therefore, we studied the influence of high-k dielectric on the performance of BDT in terms of I_{TD}. In Fig. 3 we plot the ratio between the output currents and I_{TD} (I_{LD}/I_{TD}) against the top.
We have fabricated BDTs and successfully integrated a high-k dielectric, Al₂O₃, with III-V semiconductors. This is the first successful deposition of Al₂O₃ into the trenches of any ballistic devices to enhance its performance, to the best of our knowledge. It is confirmed that $g_m$ can be increased (×2) by depositing high-k dielectric in the trenches and by downsampling the devices. It is also observed that the improvement in the $I_{LD}/I_{TD}$ ratio could be up to 30% with high-k dielectric. Smaller devices showed a 2.5× improvement in the $I_{LD}/I_{TD}$ ratio.

REFERENCES


