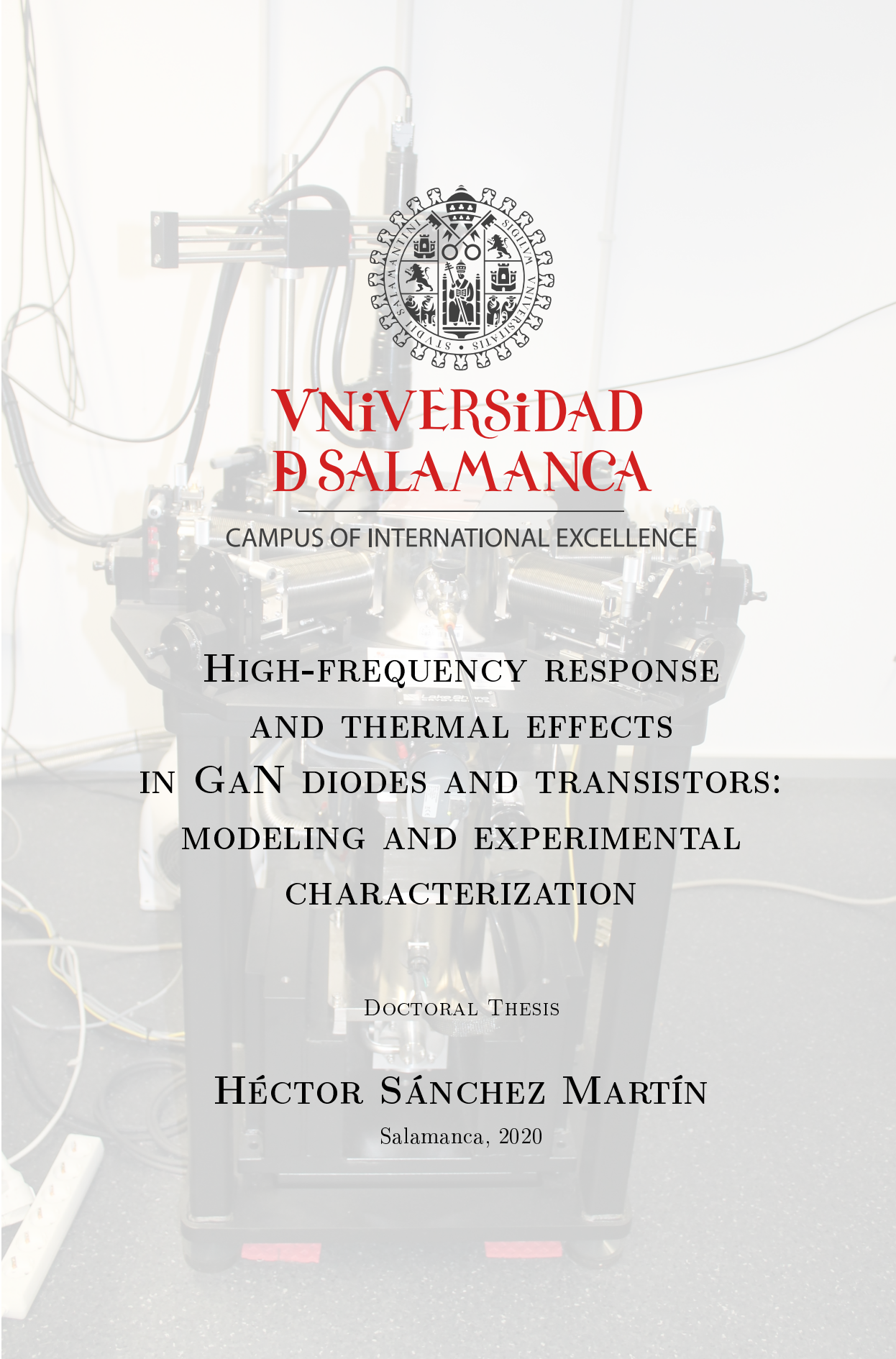

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High-frequency response and thermal effects in GaN diodes and transistors: modeling and experimental characterization

Doctoral Thesis

Héctor Sánchez Martín

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CERTIFICAN:

Que la memoria de trabajo de investigación titulado "*High-frequency response and thermal effects in GaN diodes and transistors: modeling and experimental characterization"* ha sido realizada por **D. HÉCTOR SÁNCHEZ MARTÍN** para optar al TÍTULO DE DOCTOR CON MENCIÓN DE DOCTOR INTERNACIONAL por la Universidad de Salamanca, bajo el marco del programa de doctorado **FÍSICA APLICADA Y TECNOLOGÍA**, y que ha sido desarrollada en su totalidad bajo la dirección de los directores de Tesis, en el Área de Electrónica del Departamento de Física Aplicada de la Universidad de Salamanca.

En Salamanca, a 6 de junio de 2020

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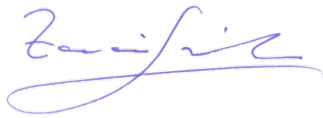

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Dedicado a mi familia

Gizonen lana jakintza dugu: ezagutuz aldatzea,
naturarekin bat izan eta harremanentan sartzea.
Eta indarrak ongi errotuz, gure sustraiak lurrari lotuz,
bertatikan irautea: ezaren gudaz baietza sortuz,
ukazioa legetzat hartuz beti aurrera joatea.
Mikel Laboa

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Abstract

GaN-based self-switching diodes (SSDs) and high-electron-mobility transistors (HEMTs) have been analyzed in DC and AC regimes both from the point of view of experiments and simulations. The non-linearities present in their current-voltage curves allow their operation as zero-bias microwave detectors. Despite of the good properties of GaN, technological problems often related to defects, traps and heating are still issues that need to be investigated to boost the performance of future power electronics.

Pulsed and transient measurements performed in SSDs reveal the influence of surface and bulk traps on the DC characteristic and AC impedance. Surface trapping effects become relevant in narrow-channel SSDs as the surface-to-volume ratio of the device is increased, while in wider diodes bulk trapping effects prevail. Measurements show an anomalous enhancement of the microwave detection at low temperature, while the detected voltage exhibits a roll-off in frequency, which can be attributed to the presence of surface and bulk traps.

Virgin AlGaN/AlN/GaN HEMTs exhibit strong low-frequency dispersion in the microwave range both in the transconductance and output conductance, attributed to the presence of traps and defects both in the volume of the GaN channel and in the source and drain contacts. These effects have been modeled by means of a modified small-signal equivalent circuit (SSEC), achieving an excellent agreement with the measured S-parameters. The device geometry affects the values of the SSEC elements and hence the cutoff frequencies, the gate length being the most determinant geometrical parameter. For $L_G = 75$ nm, f_t and f_{max} are 72 and 89 GHz, respectively, in the HEMTs under analysis.

In the SSDs, a noise equivalent power (NEP) of 100-500 pW/Hz$^{1/2}$ and a responsivity of tens of V/W was observed with a 50 Ω source. A cutoff frequency of about 200 GHz, along with a square-law response up to 20 dBm of input power, have been demonstrated. At low frequency, RF measurements exhibit a responsivity that agrees well with the calculations performed by means of a quasi-static (QS) model based on

the slope and curvature of the current-voltage curve. Biasing the devices increases the detected voltage with the disadvantage of the power consumption and the excitation of $1/f$ noise. The QS model predicts that the reduction of the channel width improves the responsivity, what was confirmed by experiments. The increase of the number of diodes in parallel reduces the device impedance; when it coincides with 3 times that of the transmission line (or antenna) to which they are connected, the NEP reaches a minimum value. Diodes with a top-gate electrode, called gated SSDs (G-SSDs), exhibit, in free-space measurements at 300 GHz, a responsivity around 600 V/W and a NEP around 50 pW/Hz$^{1/2}$ when the gate bias approaches the threshold voltage. Again, a good agreement is found, but only above sub-threshold gate bias, between the results coming from the QS model and those obtained at low frequency (900 MHz) and in free space at 300 GHz. The NEP value can be improved by increasing the number of channels in parallel.

A comparison between the injection of the RF signal at the drain (DCS) or the gate (GCS) electrode in the HEMTs operating as detectors is performed up to 40 GHz. For DCS, a responsitivy around 400 V/W and a NEP around 30 pW/Hz$^{1/2}$ were obtained in a HEMT with $L_G = 150$ nm at room temperature under zero drain current and when the gate is biased near pinch-off conditions. On the other hand, the responsivity is strongly enhanced in GCS, up to 1.4 kV/W, but with the drawback that it is necessary to apply a supplementary drain bias of $I_D = 1.2$ mA. Both configurations show a similar cutoff frequency, with a -3 dB roll-off at about 40 GHz. Interestingly, in GCS, at a frequency high enough for the gate-to-drain branch to effectively short the RF signal to the non-linearity, a non-zero detected voltage has been recorded at zero drain current.

When devices work at high-power conditions, the study of self-heating becomes relevant. Simulations were done by means of an in-house Monte Carlo (MC) tool coupled with two thermal models: (i) a thermal resistance model (TRM) and (ii) an advanced electrothermal model (ETM) based on the self-consistent solution of the steady-state heat conduction equation. At room-temperature, the MC tool was first calibrated by comparison with experimental results in TLMs (transfer length measurement), so that sheet-carrier density and mobility values were replicated. Including the effects of the contact resistance, the Schottky barrier and the thermal boundary resistance, our results are validated with experimental measurements of a HEMT with $L_{DS} = 1.5$ μm and $L_G = 150$ nm, finding a reasonably good agreement. The TRM with well-calibrated values of thermal resistances (R_{TH}) provides a similar behavior to ETM simulations. The advantage of the ETM is that it provides the temperature map inside the channel and allows to identify the hotspot location. In addition, the SSEC was obtained with MC simulations, finding a good correspondence with the

experimental values of the parameters. Impact of the biasing on the SSEC elements and discrepancies between TRM and ETM calculations are discussed. Pulsed measurements up to 500 K are used to estimate the channel temperature and the value of the R_{TH}. For $T < 250$ K, the responsivity in the DCS decreases abruptly in the sub-threshold region after reaching a maximum, while it remains practically constant for $T > 250$ K.

Keywords: gallium nitride (GaN), self-switching diode (SSD), high-electron-mobility transistor (HEMT), zero-bias microwave detectors, responsivity, noise-equivalent power, Monte Carlo, small-signal equivalent circuit, trapping effects, heating, thermal resistance.

Resumen

Se han analizado diodos autoconmutantes (SSDs) y transitores de alta movilidad de electrones (HEMTs) de GaN, tanto en el régimen DC como en AC, tanto desde el punto de vista experimental como de simulaciones. Las no linealidades presentes en las curvas corriente-voltaje permiten su operación como detectores de microondas a polarización nula. A pesar de las buenas propiedades del GaN, existen problemas tecnológicos relacionados con defectos, trampas y calentamiento que deben ser investigados para perfeccionar la electrónica de potencia en el futuro.

Medidas pulsadas y de transitorios de corriente realizadas sobre el SSD han revelado la influencia de trampas volúmicas y superficiales, observándose anomalías en las características DC e impedancia AC. Los efectos superficiales son relevantes en canales estrechos puesto que la relación superficie-volumen del dispositivo aumenta, mientras que en los dispositivos más anchos prevalece la influencia de las trampas de tipo volúmico. Las medidas muestran un incremento anómalo de la detección a bajas temperaturas, mientras que a altas frecuencias el voltaje detectado muestra una caída que atribuimos a la presencia de trampas de tipo superficial y volúmico.

Se ha observado una fuerte dispersión a baja frecuencia tanto de la transconductancia como de la conductancia de salida en HEMTs de AlGaN/AlN/GaN en el rango de microondas, que atribuimos a la presencia de trampas y defectos tanto en el volumen de canal de GaN como en los contactos de fuente y drenador. Estos efectos han sido modelados mediante un circuito equivalente (SSEC) modificado, obteniéndose un acuerdo excelente con los parámetros S medidos. La geometría del dispositivo afecta a los valores de los elementos del circuito equivalente y con ello a las frecuencias de corte, siendo la longitud de puerta el parámetro más influyente. Para $L_G = 75$ nm, f_t y f_{max} son 72 y 89 GHz, respectivamente, en los HEMTs estudiados.

En los SSDs caracterizados, se ha observado una potencia equivalente del ruido (NEP) de 100 - 500 pW/Hz$^{1/2}$ y una responsividad de decenas de V/W con una fuente de 50 Ω. Se ha demostrado una frecuencia de corte de unos 200 GHz junto a una respuesta cuadrática hasta 20 dBm de potencia de entrada. A bajas frecuencias, las

medidas RF muestran una responsividad que reproduce bien los cálculos realizados mediante un modelo cuasiestático (QS) basado en la pendiente y la curvatura de las curvas corriente-voltaje. Polarizar los dispositivos aumenta el voltaje detectado a costa del consumo de potencia y la aparición de ruido $1/f$. El modelo QS predice que la reducción de la anchura del canal mejora la responsividad, hecho que ha sido confirmado experimentalmente. El aumento del número de diodos en paralelo reduce la impedancia; cuando coincide con el triple de la impedancia de la linea de transmisión o la antena, la NEP alcanza su valor mínimo. Los diodos con puerta (G-SSDs) muestran, en espacio libre a 300 GHz, una responsividad en torno a 600 V/W y una NEP en torno a 50 pW/Hz$^{1/2}$ cerca del voltaje umbral. De nuevo, se obtiene un buen acuerdo entre los resultados del modelo QS, las medidas a 900 MHz y las medidas en espacio libre a 300 GHz, todo ello por encima de la zona subumbral. La NEP mejora al aumentar el número de canales en paralelo.

Se han comparado los resultados de la detección inyectando la señal por el drenador (DCS) y la puerta (GCS) de los HEMTs hasta 40 GHz. Para DCS, se han obtenido una responsividad en torno a 400 V/W y una NEP de 30 pW/Hz$^{1/2}$, en un HEMT con $L_G = 150$ nm a temperatura ambiente bajo condiciones de polarización nula y puerta polarizada cerca del umbral. Por otro lado, la responsividad se incrementa en GCS hasta 1.4 kV/W, con la desventaja de polarizar con una corriente de drenador de $I_D = 1.2$ mA. Ambas configuraciones muestran una frecuencia de corte, con -3 dB de caída, en torno a 40 GHz. Resulta interesante que en GCS y a una frecuencia suficientemente alta para cortocircuitar la rama puerta-drenador con la de la no linealidad, se consigue detectar una responsividad no nula.

El estudio del autocalentamiento se vuelve relevante cuando los dispositivos trabajan en condiciones de alta potencia. Las simulaciones se han realizado con una herramienta Monte Carlo (MC) desarrollada por el grupo y acoplada con dos modelos térmicos: (i) modelo de resistencia térmica (TRM) y (ii) un modelo electrotérmico avanzado y que se basa en la resolución autoconsistente de la ecuación del calor independiente del tiempo. A temperatura ambiente la herramienta MC se calibró comparando con resultados experimentales de TLMs (*transfer length measurement*), lográndose reproducir la densidad superficial de portadores y la movilidad. Incluyendo la resistencia de contactos, la barrera Schottky y la barrera térmica, nuestros resultados se han validado con medidas experimentales de un HEMT de dimensiones $L_{DS} = 1.5$ μm y $L_G = 150$ nm, encontrándose un acuerdo razonable. El TRM da unos resultados similares al ETM con valores de la resistencia térmica (R_{TH}) bien calibradas. La principal ventaja del ETM es la posibilidad de obtener mapas de temperatura dentro del canal e identificar la localización de los puntos calientes. También se discute el impacto de la polarización en el SSEC y las discrepancias entre los modelos ETM

y TRM. Se utilizan medidas pulsadas hasta 500 K para estimar la temperatura del canal y el valor de la R_{TH}. Para $T < 250$ K, la responsividad en DCS decrece abruptamente en la región subumbral tras alcanzar un máximo, mientras que permanece constante a temperaturas $T > 250$ K.

Palabras clave: nitruro de galio (GaN), diodo autoconmutante (SSD), transistor de alta movilidad de electrones (HEMT), detectores de microondas a polarización nula, responsividad, potencia equivalente del ruido, Monte Carlo, circuito equivalente de pequeña señal, efectos de trampas, calentamiento, resistencia térmica.

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List of Abbreviations and Symbols

Abbreviations

2DEG	Two-dimensional electron gas
AlGaN	Aluminium gallium nitride
AlN	Aluminum nitride
DCS	Drain-coupling scheme
DUT	Device under test
ETM	Electrothermal model
GaN	Gallium nitride
GCS	Gate-coupling scheme
G-SSD	Gated self-switching diode
HCE	Heat conduction equation
HEMT	High-electron-mobility transistor
HPC	High-power condition
IL	Insertion losses
MC	Monte Carlo
NEP	Noise equivalent power
PDR	Percentage of diffusive reflections
Q-point	Quiescent point
QS	Quasi-static model
RF	Radiofrequency
SSD	Self-switching diode
Si	Silicon
SiC	Silicon carbide
SSEC	Small-signal equivalent circuit

TBR	Thermal boundary resistance
TLM	Transfer length measurement
TRM	Thermal resistance model
VNA	Vector network analyzer

Symbols

β	Responsivity
κ	Thermal conductivity
μ	Mobility
σ	Surface charge density
H	Hybrid parameter
I_D	Drain current
I_G	Gate current
k	Stability factor
L_{DS}	Drain-to-source length
L_G	Gate length
n_s	Sheet carrier density
P_{Diss}	Dissipated power
P	Polarization charge
R_{TH}	Thermal resistance
R_C	Contact resistance
$R_\square$	Sheet resistance
S	Scattering parameter
T_{amb}	Temperature of the holder (experimental)
$T_{heat-sink}$	Heat-sink temperature (MC)
T_{latt}	Lattice temperature
U	Unilateral power gain
V_{DS}	Drain-to-source voltage
V_{DS}^{MC}	MC drain-to-source voltage
V_{GS}	Gate-to-source voltage
V_{GS}^{MC}	MC gate-to-source voltage
V_{TH}	Threshold voltage
Y	Admittance parameter
Z	Impedance parameter

Universal constants

e	Elementary charge	$1.60217656 \cdot 10^{-19}$ C
k_B	Boltzmann constant	$1.38064881 \cdot 10^{-23}$ J/K
$\hbar$	Reduced Planck constant	$1.054571817 \cdot 10^{-34}$ J·s

Introduction

Over the last decade, gallium nitride (GaN) has become a semiconductor of great interest to develop high-power RF electronics required for applications like radar, electronic warfare, electric power generation and management, or personal telecommunications. The main advantage of GaN, compared with other wide bandgap competitors like SiC, is its higher electron mobility, thus making it possible to provide large power gain up to very high frequencies [1]. An overview of the characteristics of GaN compared with its commercial competitors is shown in Figure 1 [2]. The high breakdown field (~ 3.3 MV/cm) and bandgap (3.4 eV) makes it an excellent material for working at high power. The high electron mobility (~ 2000 cm^2/Vs) and saturation electron velocity ($\sim 1.5\ 10^7$ cm/s) make it also an ideal candidate for high-frequency applications. Although GaN it is not the best material for high-temperature applications, since it has worse thermal conductivity than Si and SiC, it maintains its properties up to relatively high temperatures.

Due to the combination of these properties (high-frequency, high-temperature and high-power operation), GaN-based devices have also led the research in the improve-

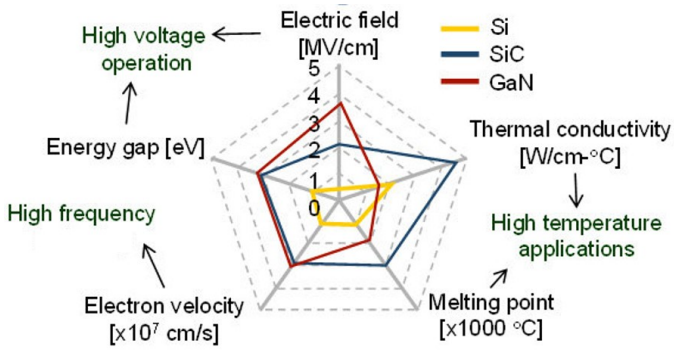

Figure 1: Comparison of material properties for high-power and high-frequency applications: Si, SiC and GaN [2].

ment of energy efficiency in high-power applications [3]. For all of these reasons, GaN has great potential in current application areas of different industrial sectors [4, 5].

On the other hand, GaN is a material in which negative differential resistance (NDR) has been predicted. Therefore, GaN is one of the few materials that could act as a source of THz radiation (T-rays) by exploiting Gunn oscillations [6, 7]. Despite technological efforts to fabricate GaN-based devices that could act as THz sources, Gunn oscillations have not been experimentally achieved yet [8, 9]. Nowadays, as alternative to traditional vertical Gunn diodes, other type of structures are being investigated, based on planar topologies, like the self-switching diode (SSD) [10]. This type of structure is very promising because of its geometry. In addition, detection up to hundreds of GHz has been experimentally demonstrated in GaN SSDs [11, 12]. Hence, based on these devices, a THz emitter-detector system could be integrated by using the same GaN technology. We will pay special attention to SSDs operating as detectors in this thesis.

GaN-based detectors

One of the main goals of high-frequency electronics is to develop a compact, high speed, and highly sensitive detector working at sub-THz and THz ranges. Solid-state devices like field effect transistors or diodes have been used to fabricate THz detectors [13]. Schottky barrier diodes (SBDs) are one of the basic elements in THz technologies, which are fabricated in different materials like GaAs (the most popular in this type of devices) [14], InP and GaN [15]. They are used both in direct detection and as non linear elements in heterodyne receiver mixers operating in a temperature range of 4-300 K. The first Schottky diode based on GaN that experimentally demonstrates detection in THz range was fabricated in 2006 [16]. However, other types of detectors based on diodes have been developed, like the mentioned SSD to be studied in this dissertation [11, 17]. Regarding the use of transistors as detectors, metal-oxide-semiconductor field-effect transistors (MOSFETs) and high-electron-mobility transistors (HEMTs) are typically used with materials like Si, GaAs, InP, and GaN [15]; the latter being the transistors of interest in this thesis. Detection in GaN-based HEMTs has also been demonstrated via self-mixing [18]. Other types of GaN based devices for THz detection have been proposed, like antenna coupled FETs (TeraFETs) working based in an asymmetrical geometry [19, 20].

On the other hand, there are different types of measurement techniques for detection of THz and microwave signals. The first alternative is the direct detection (an homodyne method) based on detecting a continuous-wave signal with the use of a nonlinear device able to rectify the RF signal, with the result of a DC rectified

voltage or current. This detection technique is usually based on an on/off switch and it is common in optical applications. An alternative method to detect an AC signal is the so-called heterodyne detection. This option requires a nonlinear device which mixes the RF radiation to be detected with a signal generated by a local oscillator (reference frequency), and it is usually applied in telecommunications and astronomy [12]. The diodes and transistors to be analyzed in this work can be integrated in both configurations, however, we will study their capabilities only in direct detection schemes.

Limiting effects in GaN: traps and heating

Despite the higher power per unit die area of GaN respect to other materials and its benefits in reduction of costs and system complexity, the costs of production of GaN-based devices are still high. In order to decrease the price of the starting material, large area Si substrates are used to grow GaN epitaxial structures, becoming the most promising solution for future technologies in the power electronics industry. However, even if there are already commercial GaN-based devices, the last generations of devices fabricated on optimized heterojunctions (AlGaN/GaN) still suffer some reliability limitations and exhibit undesired transient effects, usually related to traps, located mainly at the top surface, at the channel heterojunction [21, 22] and also in the GaN buffer [23].

Surface states at the air-semiconductor interface, typically at the top of the AlGaN layer in the vicinity of the gate contact, generate a negatively charged area, the so-called 'virtual gate' [24]. The charges at the surface contribute to the channel depletion, which extends the effect of the gate along the gate-to-drain region. These traps are typically evidenced by gate lag measurements, showing drain-current transient effects associated with the characteristic rate of trapping and detrapping processes [25], which can be mitigated by means of surface passivation [26]. Traps located at the channel heterojunction or at the interface between the semiconductor and the ohmic contacts can also have an important influence on the device characteristics. Perhaps these are the most known traps, however, as the size of the devices is shrunk and the surface-to-volume ratio increases, surface trapping effects become relevant in other regions of the devices, especially when transport takes place near etched boundaries where surface states are present, like in the SSDs to be analyzed in this thesis.

Regarding the traps located in the GaN buffer, they may capture electrons flowing through the channel. This trapped negative charge causes the so-called 'current collapse', which was also observed in the very first implementations of GaAs and GaN MESFETs [27]. Current collapse can be identified in measured current-voltage curves

as a reduction of the drain current after applying high-voltage conditions, with the consequence of a dramatic increase of the on-state resistance of the transistors and the subsequent reduction of the maximum current [28, 29]. In addition, these effects have a strong influence on the RF performance of diodes and transistors [30].

Another issue to be addressed in GaN devices is heating. The miniaturization of device characteristics and the associated increase in packing density have resulted in an exponential increase of the heat generated inside devices and integrated circuits [31]. For GaN-based devices, the thermal effects due to self-heating are not a negligible problem [32]. Despite the influence of mechanisms like (non-radiative) recombination heat or convection, the power dissipation due to Joule effect is considered the main source of temperature increase [33]. The temperature rise produced during the operation of high-power devices affects their reliability and lifetime, whose characterization and mitigation is essential for industrial applications [34]. Different methods to measure the temperature distribution inside the devices have been investigated, such as electrical coincidence method, micro Raman, scanning thermal microscopy, and infrared thermal imaging [32]. These measurement techniques allows to find hotspots in the devices. Figure 2 shows the thermal reflectance cartography of a two-finger gate AlGaN/GaN HEMT [35]. Modeling tools are also extremely useful to study the influence of these thermal effects in the performance of the devices. There are both commercial and home-made simulators that can deal with thermal effects. Different models have been suggested like the thermal resistance approach [36], the solution of the steady-state heat conduction equation self-consistently with the microscopic transport in the device [37, 38], or models based on analytical formulations [39, 40].

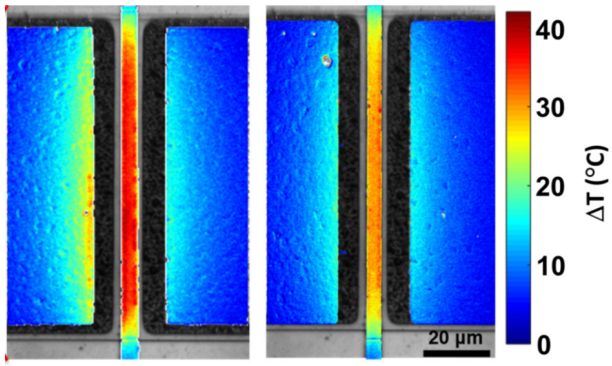

Figure 2: Thermoreflectance cartography of an AlGaN/GaN HEMT, where the temperature scale on top right indicates the temperature increase with respect to room temperature [41].

Key objectives

In this context, the main objective of this work is the characterization of GaN-based diodes and transistors to contribute to the design of devices that improve the performance of RF power systems. We will focus our attention on two type of GaN devices, SSDs and HEMTs, and we will combine electrical measurements and Monte Carlo (MC) simulations in their analysis. Special attention will be paid to thermal and trapping effects that deteriorate the device performance. In particular:

- In the case of AlGaN/GaN SSDs we will try to identify the trapping effects typically present in these devices, expected to be enhanced by the use of GaN-based materials. Also, the influence of geometry, bias conditions and temperature will be analyzed, mainly on the detection capabilities of the diodes. A measurement protocol will be designed both in DC and RF (specifically for detection) in order to identify the impact of different parameters on the operation of the diodes.
- We also plan to analyze the improvement in detection capabilities that could be achieved by adding a gate terminal on the top of the channel of SSDs, thus having a three-terminal device called Gated SSD (G-SSD) [42, 43]. By modulating the carrier concentration in the channel, the gate terminal is expected to improve the device performance.
- In the case of AlGaN/GaN HEMTs we will characterize them both from the simulation and experimental points of view. In order to investigate the influence of thermal effects in the devices, we will use MC simulations, previously calibrated by comparison with experimental results. Since transistors are part of amplifiers and the equivalent circuit is a useful tool for their design, a study of the equivalent circuit will been carried out, analyzing the influence of the bias conditions, self-heating and geometry. Finally, we plan to study the HEMT as detector, comparing the operation when the signal is coupled to drain and gate, and also the influence of temperature.

Thesis outline

As previously explained, this dissertation addresses the high-frequency behavior and thermal effects in GaN-based diodes and transistors. According to the previous objectives, the devices under study and the tools to be used in their analysis, the thesis is divided in four chapters:

In Chapter 1, the electrical characterization methods and numerical models to be used in the analysis of the devices are presented. First, we describe a quasi-static (QS) model developed from the measured DC current-voltage curve to estimate the

detection capabilities of the devices. Then, we explain the electrical characterization setups used for analysis of diodes and transistors, showing the equipment of the R&D facilities of the University of Salamanca (USAL) (see Figure 3). From the modeling point of view, we describe the home-made MC simulator developed by the group, paying special attention to the treatment of thermal effects. Finally, we explain the tools (models and measurements) employed for the characterization of the high-frequency small-signal regime of transistors.

Chapter 2 is devoted to GaN SSDs. We describe the geometry of the diodes, the physical working principles, the layer structure and the fabrication process. The diodes under analysis in this work were fabricated in the Institut d'Électronique de Microélectronique et de Nanotechnologie (IEMN), University of Lille, but at present, the fabrication process is already available at the USAL, as illustrated in Figure 4(a), which shows devices fabricated in Salamanca. Initially, effects related to traps originated in the fabrication process of SSDs are investigated. Then, we study the detection capabilities of the diodes by means of measurements and the mathematical QS model presented in Chapter 1. The two main figures of merit, responsivity and noise equivalent power, have been studied for several geometries and dimensions of the diodes. Finally, we study the G-SSD, an SSD with a Schottky gate deposited on the channel to control electron concentration. Direct microwave on-wafer and free-space measurements will be compared with the QS mathematical model. Moreover, we show results of the influence of temperature on the behavior of these devices. These measurements were done at the end of my PhD, when the laboratory received a cryogenic probe station (LakeShore CRX-VF), Figure 4(b). For this reason, the reader may find this part of the work less exhaustive.

In Chapter 3, the DC characterization of the GaN-based HEMTs is reported. The physical working principles, fabrication process (also performed at IEMN) and main characteristics of the transistors are initially presented. The wafer with the measured

Figure 3: Picture of the RF Devices Laboratory of the USAL. `http://nanoelec.usal.es/facilities`

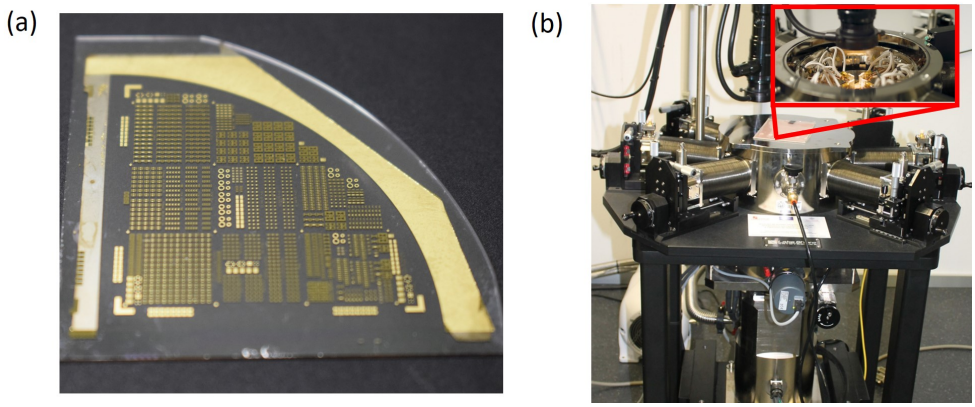

Figure 4: (a) Picture of the wafer with the GaN-SSDs processed in the clean room of the R&D facilities of USAL. (b) Cryogenic probe station.

transistors is shown in Figure 5(a). Then, we explain the protocol and the parameters to be adjusted in the MC tool to reproduce, as first step, the experimental DC curves of the transfer length measurement (TLM) fabricated on the same wafer. As second step, we also replicate the experimental output and transfer DC curves of the transistor using simulations, paying special attention to the models that account for self-heating previously presented in Chapter 1. Finally, we investigate the effects of high operation temperatures in the current-voltage characteristics of transistors.

Chapter 4 is dedicated to the analysis of the equivalent circuit and RF behavior of the transistor along with the influence of traps and thermal effects. Figure 5(b) shows the equipment used to this end. We start by describing the fundamentals of the AC characteristics of a transistor. We extract the parameters of the small-signal equivalent circuit (SSEC) of the HEMTs under analysis and investigate trap-related

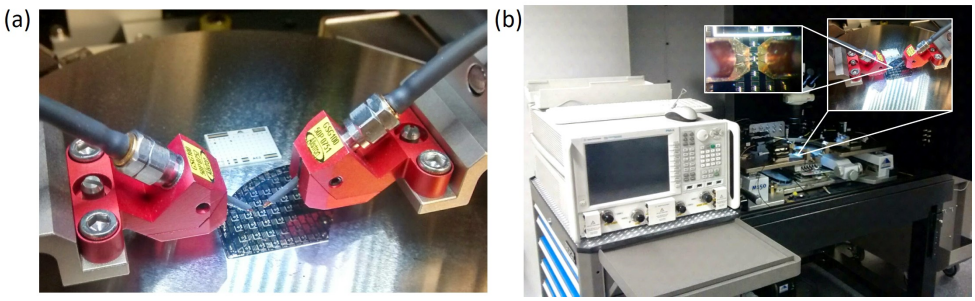

Figure 5: (a) Picture of the wafer with the HEMTs, calibration substrate and RF probes. (b) Probe station and equipment used in the microwave characterization.

dispersion effects found in some of these parameters. The influence of self-heating on the SSEC of the transistor is studied by means of simulations, using the models explained in Chapter 1 to account for thermal effects. Then, we study the influence of the geometry on the cutoff frequencies of the transistors. Finally, we investigate the detection capabilities of the transistors and their limit in frequency, as well as the influence of temperature. As previously pointed out, the temperature analysis is less exhaustive because it was done during a short period of time towards the end of the PhD.

We finish by summarizing the main conclusions and possible future research lines derived from this work.

Chapter 1

Models and Measurement Techniques

In this chapter, the tools used for the analysis of the devices are introduced. We describe the physical and mathematical models employed to predict their behavior and the experimental setups for DC and RF measurements. Since RF detectors are one of the main topics of this work, we will start describing the two figures of merit of detectors, responsivity and noise equivalent power (NEP), and how they can be estimated by means of an analytical quasi-static (QS) model based on the DC current-voltage curves. Then, the various equipment and experimental techniques required for the characterization of the devices, to be used in following chapters, will be introduced.

In order to study the physics of the devices, we perform simulations with the Monte Carlo (MC) tool developed by the group. We will describe the basics of the MC ensemble simulator coupled with a Poisson solver. Heating is the second main topic of this dissertation. The two models implemented in our MC code in order to take into account thermal effects, one called thermal resistance model (TRM) and other electrothermal model (ETM), are presented. On the other hand, we will comment on different aspects about the frequency response of transistors, including the well-known small-signal equivalent circuit (SSEC), both from the point of view of simulations and measurements. Since transistors are also used as detectors, we will explain the corresponding experimental setups and the possibility of using different electrodes (gate and drain) as input for the detection of microwave signals.

1.1. Detection with diodes

In this dissertation, we will study two- and three-contact devices (diodes and transistors). In this section, we introduce the QS analytical model to characterize detectors only with two contacts (one-port devices). The extension of the model for transistors is straightforward, so it will be explained just when the results will be shown. In addition, we explain the setup used to measure the RF detection capability of these devices.

1.1.1. Quasi-static model

This model was developed by Sorensen and Cowley [44]. It is based on the Taylor series expansion of the current as a function of the voltage, $I(V)$. Considering a DC bias term $I_0 = I(V_0)$, the response of the device to a $V_0 + V(t)$ excitation can be written by expanding the function $I\ (V)$ in series up to second order,[1]

$$I(V) - I_0 = \left(\frac{\partial I}{\partial V}\right) V(t) + 1/2 \left(\frac{\partial^2 I}{\partial V^2}\right) V^2(t). \tag{1.1}$$

In Equation 1.1 it can be observed that the first-order term is related with the resistance, while the second-order term or second derivative is related with the curvature. Indeed, this is an important parameter for a detector, since a device with linear $I(V)$ (only first-order term) does not detect. I_0 is the bias current. In small-signal operation, we can consider a harmonic signal $V(t) = vcos(\omega t)$, and the equation can be transformed into [45]

$$\begin{aligned} I(V) &\approx I_0 + \left(\frac{\partial I}{\partial V}\right) vcos(\omega t) + 1/2 \left(\frac{\partial^2 I}{\partial V^2}\right) v^2 cos^2(\omega t) \\ &\approx \left(\frac{\partial I}{\partial V}\right) vcos(\omega t) + 1/2 \left(\frac{\partial^2 I}{\partial V^2}\right) v^2 \left(\frac{1 + cos(2\omega t)}{2}\right). \end{aligned} \tag{1.2}$$

Equation 1.2 has three terms, one independent of time and two dependent of time. The one independent of time indicates the presence of a rectified signal,

$$\bar{I_d} = \frac{v^2}{4} \left(\frac{\partial^2 I}{\partial V^2}\right). \tag{1.3}$$

The corresponding rectified voltage $\bar{v_d}$ is the rectified current multiplied by the resistance of the device R_d, which is extracted from the first derivative as $R_d = \left(\frac{\partial I}{\partial V}\right)^{-1}$ and takes the following expression,

$$\bar{v_d} = \frac{v^2}{4} \frac{\left(\frac{\partial^2 I}{\partial V^2}\right)}{\left(\frac{\partial I}{\partial V}\right)} = \frac{v^2}{4} \left(\frac{\partial^2 I}{\partial V^2}\right) R_d. \tag{1.4}$$

[1] Derivatives have to be evaluated around the bias point (V_0, I_0).

On the other hand, in a real experiment an incident RF power signal P_{in} is the final responsible of the shift ($\Delta V = \bar{v_d} - V_0$) in the voltage across the device. For simplicity we consider now a zero-bias detector, $V_0 = 0$. So, we can define a parameter to characterize the detection capability of the diode as the ratio between them, called responsivity, $\beta = \frac{\Delta V}{P_{in}}$ [46]. The incident power of a harmonic signal can be also analytically calculated. In the small-signal approximation, we can use again the first order in the Taylor series expansion of the current and evaluate the incident power as,

$$P_{in} = \frac{1}{T}\int_0^T P(t)dt = \frac{1}{T}\int_0^T I(t)V(t)dt = \frac{v^2}{T2R_d}T = \frac{v^2}{2R_d}. \tag{1.5}$$

Substituting the Equations 1.4 and 1.5 in the definition of β, we have an analytical expression for the responsivity

$$\beta = 1/2\frac{\left(\frac{\partial^2 I}{\partial V^2}\right)}{\left(\frac{\partial I}{\partial V}\right)^2}. \tag{1.6}$$

In Equation 1.6, two parameters are typically defined, the resistance of the device $R_d = \left(\frac{\partial I}{\partial V}\right)^{-1}$ and the bowing coefficient

$$\gamma = \frac{\left(\frac{\partial^2 I}{\partial V^2}\right)}{\left(\frac{\partial I}{\partial V}\right)}. \tag{1.7}$$

Therefore, the responsivity in optimally matched conditions, β_{opt}, can be rewritten as[2]

$$\beta_{opt} = -1/2R_d\gamma. \tag{1.8}$$

However, the impedance of the detector[3] Z_d is not usually matched with the impedance of the source Z_s, so that the responsivity should account for the mismatch. The unmatched responsivity, β_{Z_s}, is calculated according to

$$\beta_{Z_s} = -1/2R_d\gamma(1 - |\Gamma|^2), \tag{1.9}$$

where $\Gamma = (Z_d - Z_s)/(Z_d + Z_s)$ is the reflection coefficient, which measures the mismatch between the impedance of the device and the impedance of the source. Under very mismatched conditions ($Z_d >> Z_s$),[4]

$$\beta_{Z_s} = -2Z_s\gamma. \tag{1.10}$$

[2] In results of Chapter 2, we consider the absolute value of β_{opt}, with the exception of Figures 2.22 and 2.24

[3] R_d is the DC resistance obtained from the I-V curve, while Z_d is the experimental impedance dependent on frequency. Both parameters are similar at lower frequencies, at which the QS model is applied.

[4] Z_s is typically 50 Ω and we will use the notation $\beta_{50\Omega}$ for β_{Z_s} in the following.

Other important figure of merit is the noise equivalent power (NEP), defined as the input power that provides an output voltage that coincides with the voltage noise of the detector per square root bandwidth [47]. It is used to measure the sensitivity of a detector, the minimum detectable power over the noise level. The devices in this work will operate as zero-bias detectors, in which Johnson-Nyquist noise is the main source of noise. It appears in a conductor or semiconductor at thermal equilibrium because of the thermal agitation of the carriers, and it can be written in terms of the root mean square voltage as [48, 49]

$$V_{J-N} = \sqrt{4k_B T B R_d}, \tag{1.11}$$

with k_B the Boltzmann constant, T the temperature and B the post-detection bandwidth. In a matched system, the NEP of a zero-bias detector is

$$NEP_{opt} = \sqrt{4k_B T R_d}/\beta_{opt}. \tag{1.12}$$

In a mismatched device, the definition of the NEP is analogous to the definition in a matched one, but considering β_{Z_s},

$$NEP_{Z_s} = \sqrt{4k_B T R_d}/\beta_{Z_s}. \tag{1.13}$$

1.1.2. Experimental setups

In the previous subsection, we have introduced a QS analytical model to study the detection performance of a two-terminal device, starting from its I-V characteristic. In this subsection, we will explain the experimental methods used to characterize the RF detection, showing the required setup for two-contact devices, also starting from the measurement of the I-V curve.

In order to apply the QS model and predict the detection performance, it is necessary to measure the DC current-voltage characteristic of the device. In Figure 1.1(a), we show the back panel of our semiconductor analyzer, a Keithley 4200-SCS, with: (i) three source measurement units or SMUs, connected with the black cables in the image, two of them for medium power (210 V, 105 mA and 2 W) and the other one for high power (210 V, 1.05 A and 22 W), (ii) one pulse measurement unit or PMU with two channels, connected with white cables in the image and (iii) a C-V unit, connected with the red cables in the image, for impedance characterization. In Figure 1.1(b), we show two RPM-4225 remote amplifiers, which also allow to change between different the type of measurements (DC, pulsed or C-V). The advantage of including RPMs in the setup is not only expand the low current level and reduce cable capacitance effects but also supports switching automatically between different experiments without reconnecting the probes after every measurement.

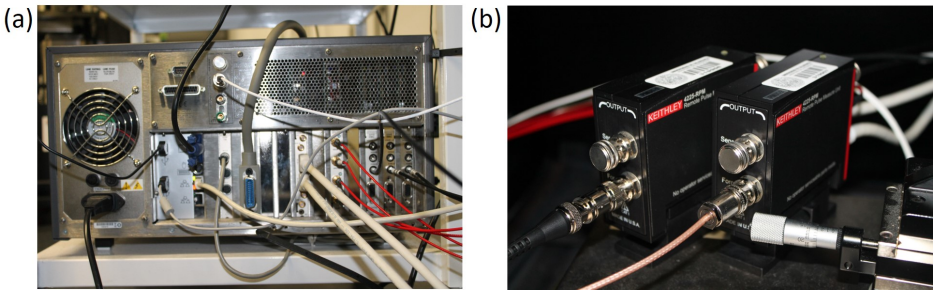

Figure 1.1: (a) SMUs, PMUs and C-V connectors of the Keithley 4200-SCS semiconductor analyzer and (b) RPM-4225 remote amplifiers/switches.

The measurements at room temperature are done in a Cascade M150 probe station, shown in Figure 1.2(a), where the micropositioners of the DC probes required for on-wafer measurements can also be observed. They are connected to the RPMs shown in Figure 1.1(b). On the other hand, in Figure 1.2(b) the DC needles used for the DC characterization of the devices are shown

The QS model is used as a preliminary test to find the devices with best detection figures of merit. After that, we measure the detection in the RF regime excluding devices with poor performance. Each setup has its own source and is designed for a given frequency range: (i) lower than 1 GHz, designed for on-wafer measurements, (ii) frequencies between 100 MHz and 43.5 GHz, also designed for on-wafer measurements, and (iii) frequencies of 150 and 300 GHz in free space. The responsivity is calculated accounting for the power losses of the experimental setup as

$$\beta_{50\Omega} = \frac{\Delta V}{P_{IN}} = \frac{\Delta V}{P_{Source} - IL}, \tag{1.14}$$

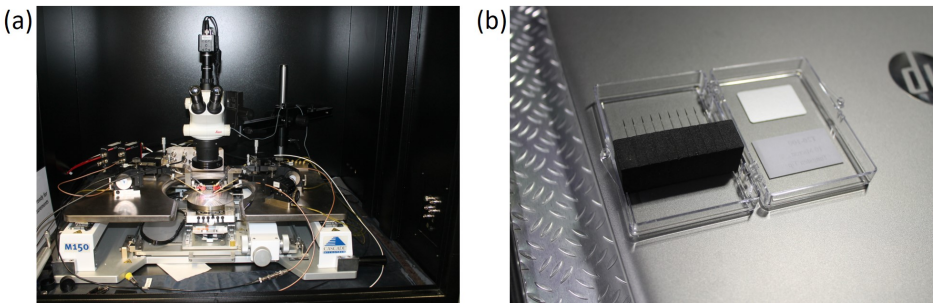

Figure 1.2: (a) Room temperature Cascade M150 probe station and (b) needles used in the DC measurements.

where IL are the input losses, generated by cables, fixtures, probes and optical losses, which need to be calibrated.

In Figure 1.3, the setup for frequencies up to 1 GHz is shown. This is a setup thought to measure with the DC probes (needles) previously shown in Figure 1.2(b). It includes the Keithley 4200-SCS semiconductor analyzer, used as source measurement unit (SMU). According to the definition of responsivity in the QS model (see subsection 1.1.1), as output we should measure the variation given by the DC voltage in the presence of the RF signal, so the SMU fixes the current and measures the DC voltage.

The second equipment in the setup is a Vector Network Analyzer (VNA), N5244A PNA-X of Keysight Technologies, used here as a source of RF signals up to 1 GHz in this case. We employ this measurement setup when the devices do not have coplanar waveguide (CPW) accesses. Of course, the insertion losses are high and limit the detection results; a careful calibration must be done (see section 2.4). In Figure 1.4(a), we show an image of the VNA. This VNA has 4 ports, which work with power up to 27 dBm and allow a maximum bias current of 500 mA and 250 V of maximum voltage in the internal bias-tee. The frequency of the output signal is in the range from 10 MHz to 43.5 GHz. The VNA has an internal bias-tee in the DC input/output connection to combine DC and RF signals while isolating the internal detectors of the VNA from DC signals and the SMU from RF signals. In our setup, this DC connection is also used as the output where the detected voltage is measured. The VNA has also installed the option 029 to measure the noise power spectrum.

In order to perform high-frequency measurements in devices with CPW accesses, we include a variation in the previous setup. We use RF probes of 100 μm pitch

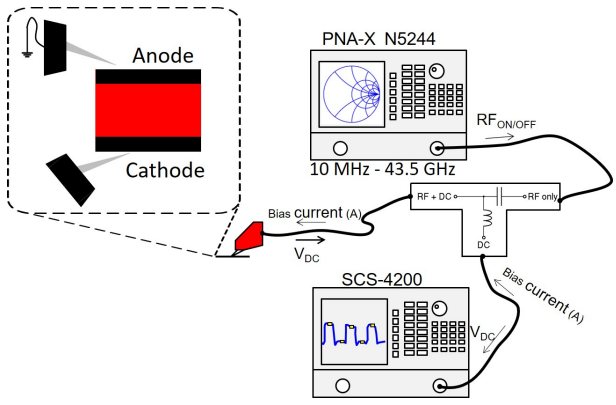

Figure 1.3: Setup to measure detection for frequencies up to 1 GHz. The zoom shows the DC needles used in this setup.

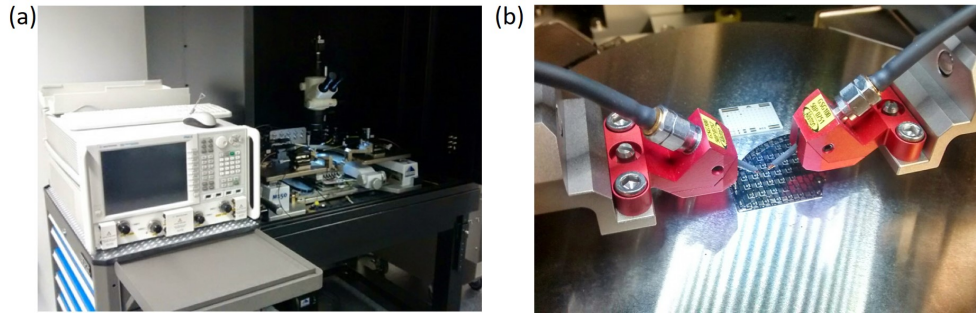

Figure 1.4: Images of (a) the Vector Network Analyzer N5244A PNA-X and (b) the GSG RF probes (100 μm pitch) used for the on-wafer characterization.

with a maximum operation frequency of 50 GHz, which is also the limit frequency of the 2.4 mm cables. In Figure 1.4(b), we show the RF probes of Allstron with a pitch of 100 μm (the laboratory also has the option of using a pitch of 50 μm). The configuration of these probes is ground-signal-ground (GSG), prepared for the CPW shape of pads like the one shown in Figure 1.5. The higher limit frequency of the fixtures and the VNA (maximum frequency of 43.5 GHz) allows us to extend the characterization range. Figure 1.5 shows the setup including the modifications due to this different type of contacts. Indeed, the pads shown in the figure are thought for on-wafer measurements up to higher frequencies than those covered by our VNA.[5] Insertion losses are also present in this setup, and a calibration step previous to the measurement is necessary.

As mentioned in the introduction, at the end of my PhD a LakeShore CRX-VF cryogenic probe station was installed in the laboratory (see Figure 1.6). This probe station has six micro-manipulated probe arms (4 DC and 2 RF), each one providing position control to land the probe tip accurately on the device pads. Combined with the previous setup, the use of the CRX-VF station allows to change the operation temperature of a device in a very wide range, from below 10 K to 500 K (Model 336 temperature controller) [50]. Moreover, the cryogenic probe station is equipped with a vertical field superconducting magnet (Model 625 superconducting magnet power supply), which is capable of maximum field of 2.5 T (temperatures < 10 K), 2 T (temperatures between 10 and 400 K) and 1 T (temperatures between 400 and

[5]It is to be noted that at present our group is developing a LabView software to automatize this kind of experiments, controlling a SMU (in this case Agilent B2902A) and the VNA. This software allows the new users, which are not familiar with the equipment, to easily perform the measurements. In particular, the LabView code controls not only the DC operating conditions, but also the RF power and frequency of the injected signals, and it is able to correct the losses of the setup (previously charged in the program).

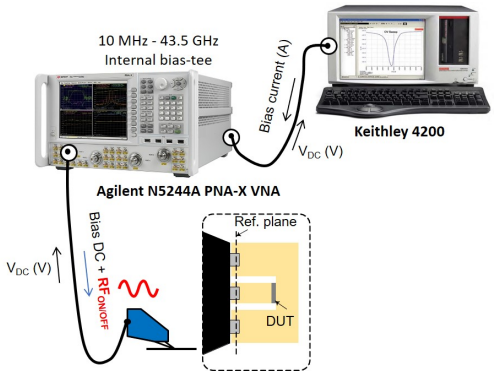

Figure 1.5: Setup to measure detection for frequencies between 10 MHz and 43.5 GHz. The zoom shows the CPW access and GSG RF probe used in this setup.

500 K). Software 8400 series HMS is used in the Hall measurements. Thanks to the available probes, both DC and RF measurements as a function of temperature can be performed with this probe station. All the equipments and setups previously described are available at the RF Devices Laboratory, which our Research Group on High-Frequency Nanoelectronic Devices is responsible for, sited in the Edificio Multiusos I+D+i of the USAL.

The third type of setup, corresponding to free-space measurements, is completely different to the previous ones. Now, the signal is generated by a free-space THz source (without a waveguide) and part of the setup is designed to focus the radiation in the detector effective area. In Figure 1.7, there is a schematic of the setup conceived for image mapping, thus including a x-y stage to move the analyzed sample and an image of the solid-state THz source (based on a Gunn diode), with output frequencies of 150 and 300 GHz. The output power is 4 mW at 150 GHz and $\sim$ 6 mW at 300 GHz.

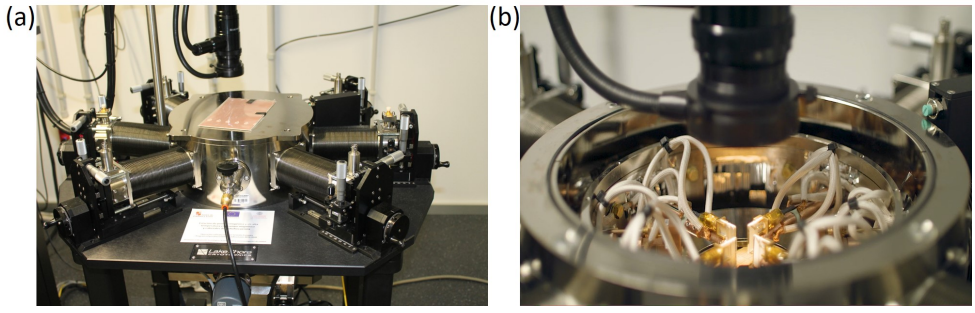

Figure 1.6: Picture of (a) the LakeShore CRX-VF cryogenic probe station and (b) vacuum chamber with the probes and the sample holder.

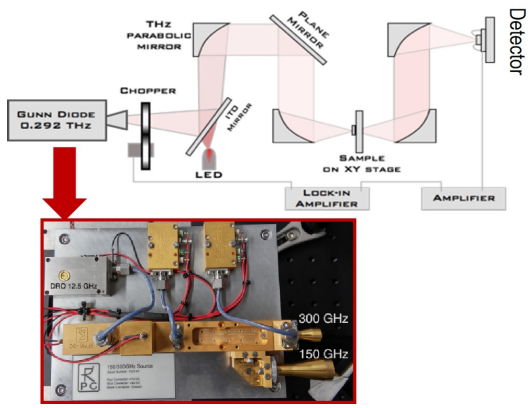

Figure 1.7: Description of the free-space setup and the THz source.

The photoresponse is measured using the lock-in method shown in the schematic of the setup. A lock-in amplifier measures the amplitude of a periodic signal. In order to measure this signal, the lock-in is excited with a reference voltage synchronous with the signal whose amplitude is to be measured. The lock-in amplifier uses the reference signal to compare it with the signal to be measured, ignoring anything which is not synchronized with the reference voltage [51]. This measurement setup is available in the THz laboratory of Prof. Y. M. Meziani, also located at the Edificio Multiusos I+D+i of the USAL.

1.2. Monte Carlo simulations

In this section, we introduce the models included in the simulations used to study the devices of Chapters 3 and 4, based on the MC method. This method is used to solve many physical problems where highly-complex probability distributions are involved and non-analytical solutions are obtained. Other approaches commonly used in the simulation of semiconductor devices are the *drift-diffusion* and *hydrodynamic* models, which are not accurate enough for the simulation of small devices [52].

The MC method was created to deal with integrals whose solution cannot be found with analytical methods. Its name comes from the generation of random numbers and its relationship with the roulette of casinos in the capital of Monaco. The implementation of the method in computational science can be related with the development of nuclear weapons. In electronics, MC simulations consist on the microscopic treatment of the dynamics of one or a group of carriers moving inside a semiconductor material subjected to the action of an electric field and the crystal lattice. Since MC

is a microscopic model, it takes into account intrinsically scattering mechanisms, hot-carrier effects, non-stationary and ballistic transport. In addition, it is a very suitable tool to study physical phenomena related with noise and fluctuations. By means of MC technique, it is possible to generate values of a variable following a complicated probability distribution through random numbers distributed between 0 and 1 [53]. In this work, we will apply MC simulations to study transport in resistors made of semiconductors used for the transfer length measurement (we will call them TLMs from now on) and high-electron-mobility transistors (HEMTs).

As mentioned before, the MC method is based on the use of known random distributions to obtain the values of different physical quantities that obey complex probability distributions [54]. If $p(\Phi)$ is the complex probability density distribution associated to the variable Φ and $p(r)$ is the known random probability density distribution associated with r, it is always possible to find values of Φ and r fulfilling [55]

$$\int_0^{\Phi} p(\Phi^{'})d\Phi^{'} = \int_0^{r} p(r^{'})dr^{'}. \tag{1.15}$$

If the random distribution is a uniform distribution between 0 and 1, $p(r) = 1$, and therefore Equation 1.15 can be written as

$$r = \int_0^{\Phi} p(\Phi^{'})d\Phi^{'} \rightarrow \Phi = \Phi(r). \tag{1.16}$$

The inversion of the previous expression provides random values of Φ, obeying the distribution $p(\Phi)$, as a function of r, where r is a random number uniformly distributed between 0 and 1. If the integral of Equation 1.16 is impossible to evaluate analytically, or the expression can not be inverted directly, there are different techniques that allow the inversion, like importance sampling, rejection sampling, Metropolis method and Gibbs sampling [56].

In a typical MC simulation, the described method is applied every time the value of a physical quantity obeying a given probability distribution is needed, like in the case of the calculations of the free-flight time, the electron state after a scattering mechanism, the times of electron injection at the contacts, etc.

1.2.1. Monte Carlo tool

There are three scenarios of MC simulations depending on the type of problem under study:

- The **single particle MC technique** is used in homogeneous and stationary transport problems, where the electric field is constant. The basic philosophy of the single particle MC technique, applied to charge transport in semiconductors,

consist in simulating the dynamics of a single carrier inside an uniform electric field for a long time and, by ergodicity, obtaining information about the physical properties of the whole electron gas. The carrier dynamics to be simulated is a sequence of free flights of the particle accelerated by an applied electric field between instantaneous scattering events. Figure 1.8(a) describes this process. The free-flight time of the particle, the scattering mechanism taking place at the end of the free flight and the state after the scattering event (energy and momentum) are randomly determined (according to the appropriate distributions) by means of MC algorithms. By monitoring the particle motion during a long enough simulation, several physical quantities are estimated, such as the distribution function, average drift velocity or average energy.

- The second level is the so called **ensemble MC**, used in homogeneous and non-stationary problems. For this type of problems, in which the dependence on time of different quantities is of interest, it is not enough to simulate just one particle, but an ensemble of particles is necessary. For example, in order to study a transient behavior, a synchronous simulation of a reasonable number of particles, M, during N iterations of Δt time is performed. The previously explained single-particle algorithm (free flights and scattering mechanisms) is repeated for each particle. The individual carriers are simulated independently of the others, with the particularity that the quantities of interest are sampled at every time-step Δt [57]. Such instantaneous values are averaged among the M particles at the end of the simulation, thus obtaining time-dependent values of the quantities of interest averaged over the ensemble of particles.
- The third scenario, adequate to study our TLMs and transistors, is the **MC device simulator**, which corresponds to non-homogeneous and non-stationary problems where boundary conditions (BCs) at the limits of the simulation domain are present, like in the case of semiconductor devices. This technique is a modified ensemble MC where all the carriers are simultaneously simulated every Δt, at the end of which Poisson's equation is solved in a spatial grid to update the electric field profile. Two type of BCs must be considered in the simulations, for the movement of carriers and for the solution of Poisson's equation [58]. At the end of each time step Δt, carriers are frozen and the potential to be used in the next time-step is calculated self-consistently with the charge distribution [53]. The scheme of the 2D device simulator is shown in Figure 1.8(b).

In this work we will make use of the MC device simulator developed by the group. In order to correctly analyze transport in the devices, some physical conditions must be satisfied by the temporal and spatial discretization of the problem [58]. To account for the local value of the electric field, the simulation domain is divided in meshes,

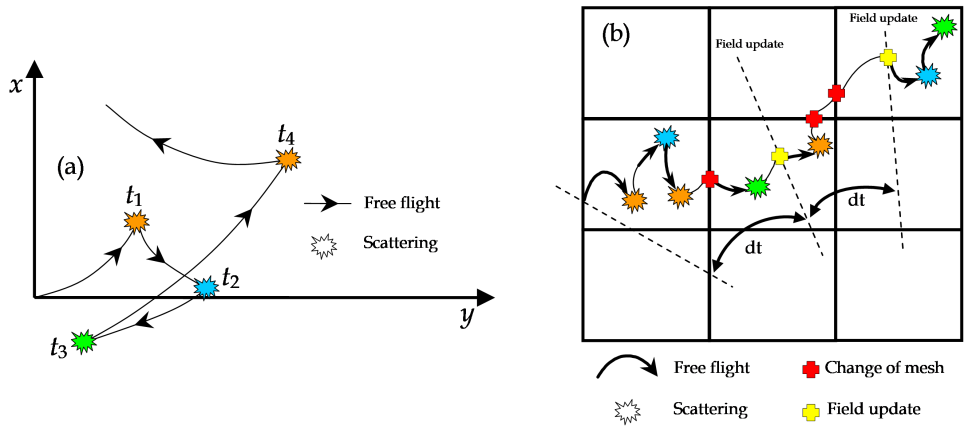

Figure 1.8: (a) Simple diagram of the single particle simulation in real space under a uniform electric field applied in the x-direction. (b) Scheme of the 2D device simulator with the main events indicated by symbols.

used to solve Poisson's equation. The size of this meshes (Δd) should be smaller than the Debye length to have a correct solution of the electric field [59]. On the other hand, the time step (Δt) at which the electric field is updated is limited by the plasma frequency (ω_p) (its inverse) and the dielectric relaxation time τ_d. The time step should satisfy the conditions $\omega_p \Delta t < 2$ and $\Delta t < \tau_d$ [56]. In our simulations, we consider Δt as small as 1 fs and Δd as small as 5 nm. On the other hand, the exact study of the device would require the simulation of the huge number of N carriers present inside it, which is impossible from the point of view of CPU resources. In the simulation, a smaller number of *superparticles* (N_s), with a charge of eN/N_s, is considered. The ratio N/N_s is defined as the electron particle equivalent, EPE.

1.2.1.1. Semiconductor physical model

The influence of the semiconductor crystal lattice on the carrier motion takes place by means of the band structure and the scattering mechanisms. There are different possibilities to model the band structure in the simulations, like using a full-band model calculated by tight-binding or pseudopotential approaches [60]. In our case, we use an analytical model consisting in a spherical non-parabolic approximation for the energy of the electrons

$$\epsilon(\vec{k})(1 + \alpha\varepsilon(\vec{k})) = \frac{\hbar\vec{k}}{2m^*}, \tag{1.17}$$

with ε the energy, $\vec{k}$ the wave vector, m^* the effective mass of the carriers, $\hbar$ the normalized Planck constant, and α the non-parabolicity coefficient. In this work, we

Parameter	GaN			$Al_{0.29}Ga_{0.71}N$		
Density (Kg/m^3)	6150			5302.2		
Sound velocity (m/s)	6560			57285		
Optic dielectric constant	5.35			5.1818		
Static dielectric constant	8.9			8.784		
Polar optical phonon energy (eV)	0.09120			0.09336		
Non-polar optical phonon energy (eV)	0			0		
Bandgap (eV)	3.44			4.1244		
Lattice constant (Å)	5.185			5.1255		
	Γ_1	U	Γ_3	Γ_1	U	Γ_3
Effective mass (m^*/m_0)	0.22	0.39	0.28	0.2548	0.4132	0.3090
Non-parabolicity (eV^{-1})	0.37	0.50	0.22	0.3439	0.3666	0.2403
Energy level from Γ (eV)	0.0	2.2	2.4	0.0	1.91	2.43
Number of equivalent valleys	1	6	1	1	6	1
Acoustic deformation potential (eV)	8.3	8.3	8.3	8.648	8.648	8.648
Optical deformation potential	0.0	0.0	0.0	0.0	0.0	0.0
Intervalley deformation potential (10^{10}eV/m)						
from Γ_1 to	0	10.0	10.0	0	10.0	10.0
from U to	10.0	10.0	10.0	10.0	10.0	10.0
from Γ_3 to	10.0	10.0	0.0	10.0	10.0	0.0
Intervalley phonon energy (eV)						
from Γ_1 to	0	0.09120	0.09120	0	0.09352	0.09352
from U to	0.09120	0.09120	0.09120	0.09352	0.09352	0.09352
from Γ_3 to	0.09120	0.09120	0.0	0.09352	0.09352	0.0

Table 1.1: GaN and AlGaN electron parameters.

consider a three valley model formed by Γ_1, U and Γ_3 valleys for the conduction band of the nitride materials involved in the devices under analysis, GaN and AlGaN.

The parameters used in our MC model for the simulation of electrons in these semiconductors can be found in Table 1.1. Apart from the data of the band structure, other parameters related to the scattering mechanisms, to be described in next subsection, are also included in the table.

1.2.1.2. Scattering mechanisms

The free flights are finished by scattering mechanisms. These mechanisms can be classified according to different criteria:

- In terms of energy of the electron after the interaction, we consider:
  - Elastic: the electron conserves its energy after the interaction. Ionized impurity scattering and electron-electron scattering are examples of this type of scattering.
  - Inelastic: the electron gains or losses energy in the collision. Scattering with optical phonons is an example.

- In terms of the wave vector of the electron before and after the scattering:
  - Isotropic: the wave vector after the scattering does not depend on the direction of the initial wave vector. The probability for the final state to be in any direction is the same. Examples of isotropic scattering are the optical (non-polar) and intervalley scatterings.
  - Anisotropic: the direction of the final wave-vector is dependent on the initial wave vector of the electron. The probability for the direction of the final wave vector with respect to the initial one is typically higher for small angles. An example is acoustic (non-polar) scattering.
- In terms of the physical origin of the mechanisms:
  - Scattering with defects: the interaction with ionized impurities is included here. It is a Coulombic interaction, elastic and anisotropic. In our simulations, this scattering is implemented following Brooks Herring model [61]. Alloy scattering (ternary materials) and dislocation scattering (GaN layer) are also considered as scatterings with defects and they are relevant in our heterostructures [62].
  - Carrier-carrier scattering: this interaction is not taken into account in our simulations because it is only significant for very high carrier concentrations.
  - Lattice scattering: this includes the interactions with phonons caused by the vibrations of the lattice [63]. They can be intravalley or intervalley depending if the valley of the final state of the carrier after the interaction is the same as initial one or not. Intravalley scattering involves phonons with small wave vectors and intervalley scattering involves phonons with large wave vectors. Additionally, there are two types of intervalley mechanisms, equivalent or non-equivalent, depending if the type of valley of the final state is the same as the initial one or not [63].

In our simulations, the following scattering mechanisms are considered for both GaN and AlGaN:

* Intervalley (equivalent and non-equivalent): inelastic and isotropic processes.
* Alloy scattering: elastic and isotropic.
* Scattering with dislocations: elastic and anisotropic.
* Acoustic (polar) scattering: elastic and isotropic.
* Acoustic (non-polar) or piezoelectric scattering: elastic and isotropic.
* Optical (polar) scattering: inelastic and anisotropic.

We do not consider optical non-polar scattering, since this mechanism takes place only in L-valleys and it is not significant in GaN. More details about the scattering mechanisms can be found in previous dissertations by the group [53, 55, 56, 58, 64]. The probabilities of scattering mechanisms, dependent on the electron energy, are calculated at the beginning of the simulation and accumulated in a matrix [58, 65]. These probabilities will then be used during the simulation to determine the free-flight time and select the scattering mechanisms taking place. The exception is the probability of scattering with defects, which must be calculated during the simulation with the self-consistent update of the Fermi level and the electronic temperature [66].

1.2.1.3. Carrier dynamics

As mentioned, carrier dynamics in the MC method consists in a sequence of free flights and scattering mechanisms. In this subsection, we describe the motion of carriers under the action of the electric field during the free flight, how the duration of the free flight is determined, and the process to select the scattering mechanism at the end of the free flight and to determine the final state after scattering.

Free-flight motion

Within a semiclassical approximation, the equation describing the time evolution of the wave vector under the action of the electric field is [63, 67]

$$\hbar \frac{\partial \vec{k}}{\partial t} = \vec{F}, \tag{1.18}$$

where $\vec{k}$ is the wave vector and $\vec{F} = -e\vec{E}$ the external force. Moreover, in the non-parabolic band approximation used in our simulations, the electron velocity can be obtained as [63]

$$\vec{v} = \frac{1}{\hbar}\vec{\nabla}_k \varepsilon_n = \frac{\hbar \vec{k}}{m^*(1+2\alpha\varepsilon)}. \tag{1.19}$$

According to these equations, the position and the wave vector of the electron at a time t during the free flight can be calculated as

$$\vec{r} = \vec{r}_0 - \frac{e\vec{E}t^2}{2m^*(1+2\alpha\varepsilon)} + \frac{\hbar\vec{k}_0 t}{m^*(1+2\alpha\varepsilon)}, \tag{1.20}$$

$$\vec{k} = \vec{k}_0 - \frac{e\vec{E}t}{\hbar}, \tag{1.21}$$

where $\vec{r}_0$ and $\vec{k}_0$ are the position and wave vector of the carrier at the beginning of the free flight, respectively.

Free-flight time

The free-flight time is randomly calculated according to the total scattering probability for the energy of the electron. The probability (per unit of time) that an electron experiences a free flight of length t and at the end suffers a scattering mechanism is [58, 52]

$$P(t) = \Gamma e^{-\Gamma t}, \tag{1.22}$$

where Γ is the (constant) total probability of scattering. Γ is made constant with energy by including a fictitious scattering mechanism called self-scattering [68], which has no effect in the final state of the electron.

$$\Gamma = \Gamma_{self}(\varepsilon) + \Gamma_1(\varepsilon) + ... + \Gamma_N(\varepsilon), \tag{1.23}$$

where $\Gamma_i(\varepsilon)$ is the probability of the i-th scattering mechanism and $\Gamma_{self}(\varepsilon)$ the self-scattering probability.

Self-scattering is introduced in the simulation because the integral of the total scattering probability can not be analytically evaluated and we could not directly apply the MC method. Once Γ is made constant with energy by including self-scattering, Equation 1.16 can be used with the free-flight time probability expressed in Equation 1.22, and we can obtain a random value of the the free-flight time as

$$t = -\frac{1}{\Gamma} ln(r), \tag{1.24}$$

with r a random number between 0 and 1. Since Γ is higher than the value of the total scattering probability without the self-scattering, an excess of fictitious mechanisms takes place, increasing the computational time. To mitigate this negative effect, other algorithms that reduce the number of fictitious mechanisms can be included in the simulations [69]. One of these algorithms consists in modifying the value of Γ according to the range of energy where the electron is moving.

Scattering mechanisms

The end of the free flight is caused by a scattering mechanism. The concrete type of scattering taking place has to be chosen according to the probabilities of the different scattering mechanisms corresponding to the energy of the electron at the end of the free flight. Once the type of scattering is chosen, the final state of the electron after the collision must be determined.

In order to select the scattering mechanism, we use a random number r between 0 and 1. Previously to the simulation, the scattering probabilities of every mechanism Γ_i are calculated as a function of the electron energy (see subsection 1.2.1.2).

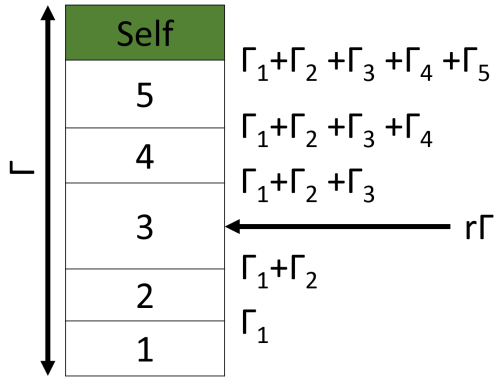

Figure 1.9: Election of the type of scattering mechanism after a free flight.

The chosen scattering mechanism l is the one that satisfies the following condition $\sum_{i=1}^{l-1} \Gamma_i < r\ \Gamma < \sum_{1}^{l} \Gamma_i$, with Γ_i the scattering probability of the i-th mechanism for the energy of the electron at the end of the free flight. The Figure 1.9 illustrates the method.

Final state after the scattering mechanism

Once the type of scattering is chosen, the final state (energy and wave vector) after the scattering must be calculated. Self-scattering does not change the state of the electron. In case of selecting a real scattering mechanism, the final energy is $\varepsilon_f = \varepsilon_i + \Delta\varepsilon$, with ε the increment of energy associated to the collision. If the scattering is elastic, the increment of energy is $\Delta\varepsilon = 0$. In inelastic scattering mechanisms, $\Delta\varepsilon = \pm\hbar\omega$, with $\hbar\omega$ the energy of the involved phonon. The sign + is for absorption and the sign - for emission. In the case of intervalley scattering mechanisms $\Delta\varepsilon = \pm\hbar\omega \pm\Delta\varepsilon_{ij}$, with $\Delta\varepsilon_{ij}$ the energy gap between valleys, the sign + for a change to an upper valley and - to a lower one [58]. Once the energy is known, the direction of wave vector in the final state must be determined, again using MC techniques. The calculation of the final wave vector depending if the mechanism is isotropic or anisotropic is detailed in [58].

Additionally, there is a rejection possibility related to the Pauli exclusion principle and that is locally applied to account for degeneracy. Electron concentration in some regions of the devices may be very high (like in the 2-DEG present in the channel of transistors), so that if the final state after scattering is occupied the scattering mechanisms should be rejected. The program includes an algorithm to calculate locally the Fermi level (ε_F) and the electronic temperature (T_{el}) self-consistently with the

average electron energy and electron concentration [66]. The occupation of the final state of the electron after scattering, corresponding to an energy ε, is given by the Fermi-Dirac distribution

$$f_{FD}(\varepsilon) = \frac{1}{1 + exp\left[\frac{\varepsilon - \varepsilon_F}{k_B T_{el}}\right]}. \tag{1.25}$$

The probability that a random number r has a value between 0 and $f_{FD}(\varepsilon)$ is the same as the probability that the final state is occupied, and in such a case the mechanism is rejected.

1.2.1.4. Boundary conditions and electric field

Two type of BCs must be considered at the time of simulating an electronic device: for the movement of carriers and for the solutions of Poisson's equation.

At the contacts, Dirichlet BCs are applied for the potential (fixed value). As concerns carrier movement, in Schottky contacts the current can only flow out of the device (carriers reaching the contact leave the device, but there is not injection of particles), while in ohmic contacts the flow is bidireccional and carriers are injected to ensure charge neutrality in the vicinity of the contact by the algorithms explained in next subsection. In free surfaces, Neumann BCs are imposed to solve the potential (zero normal derivative) and specular reflection is applied to carrier movement. In the case of heterojunctions (present in the devices under analysis), the continuity of the displacement vector is applied, including the term corresponding to surface charges in case these are present (like in the top of the devices or at heterojunctions with piezoelectric charges) [53].

Physical model of ohmic contacts

In our devices, ohmic contacts are present at the source and the drain of transistors (the gate is a Schottky contact). The model for ohmic contacts establishes, apart for the fact that carriers reaching the contact leave the device, that charge neutrality should be maintained in the mesh close to the contact. This is achieved by injecting periodically, typically every time the electric field is updated (every time step Δt), the number of thermal electrons necessary to equal the free-carrier concentration to the impurity density in that mesh. Therefore, at the end of every time step we have to determine the number of electrons that should be injected, the moment at which they enter the device, their coordinates and their state (energy and wave vector) [70].

To accomplish the charge neutrality condition, it is necessary to know the free-carrier concentration (n_c) in the meshes adjacent to the contact at every Δt. If

$n_c > N_c$, with N_c the doping density in the cell, there is no carrier injection and the excess is naturally eliminated by diffusion. If $n_c < N_c$, there is injection of carriers as follows. A first carrier is injected with an initial position x = 0 (position of the cell adjacent to the contact) and its dynamics inside the device is simulated during a time $r\Delta t$, where r is a random number uniformly distributed between 0 and 1. After that, if n_c remains lower than N_c, a new carrier is injected in the same way. This is repeated until $n_c = N_c$ is achieved [70].

At the contact, the electrons cross the border between the contact itself and the adjacent cell inside the device. Therefore, the carriers with higher velocity have more probability to enter the device. To model this effect a thermal velocity distribution $f_{th}(v)$ is weighted by the velocity perpendicular to the contact $v_\perp$, since an electron with $v_\perp = 0$ would never cross the barrier. Thus, as model for the velocity distribution we use [53]

$$\begin{aligned} f_{iny}(v_x) &= v_x f_{th}(v), \\ f_{iny}(v_y) &= f_{th}(v), \\ f_{iny}(v_z) &= f_{th}(v). \end{aligned} \tag{1.26}$$

In a general simulation the thermal distribution is the Fermi-Dirac one (analogue to Equation 1.25). However, if contacts are non-degenerate, the Maxwell-Boltzmann distribution is a good approximation. The weight v_x, is positive in the left contact and negative in the right one according to the direction of carrier injection.

The Maxwellian distribution function is given by

$$f_{th}(v) = \sqrt{\frac{m^*}{2\pi k_B T}} exp\left[-\frac{m^* v^2}{2k_B T}\right]. \tag{1.27}$$

Applying the MC method and integrating in polar coordinates, the components of the velocity are

$$\begin{aligned} v_x &= v_{th}\sqrt{-\pi ln r_1}, \\ v_y &= v_{th}\sqrt{-\pi ln r_2} cos(2\pi r_3), \\ v_y &= v_{th}\sqrt{-\pi ln r_2} sin(2\pi r_3), \end{aligned} \tag{1.28}$$

where r_1, r_2 and r_3 are three random numbers between 0 and 1, while the parameter $v_{th} = \sqrt{(2k_B T)/(m^*\pi)}$ is the thermal velocity. In case of degenerate contacts, the Fermi-Dirac distribution must be used, the direct integration is not possible, and a rejection technique is necessary to determine the three velocity components.

In the simulations of this work, contacts will be placed in the lateral sides of the devices, where heterostructures are present. Therefore, the electrodes are in contact

with different semiconductors. In such a case, potential and carrier injection profiles are necessary, since both of them are not constant along the contact. To this end, we start with simulations in which the contact is in the top of the device. The potential and concentration profiles in the center of the device are registered at zero bias. These profiles are then used as equilibrium condition for the lateral injection. This method has the disadvantage of lacking of a reference for the potential. In this work we will establish the reference of the potential at the bottom of the device. In subsection 3.3.1.2, the details of these calculations are provided.

Poisson's solver

In order to solve Poisson's equation, the device, a HEMT in our case, is divided into cells. The size of the cells is different depending on the expected inhomogeneity of the electric field in each region of the device and the required precision. Moreover, the size of the cells is subjected to the physical restriction mentioned in subsection 1.2.1.1. Poisson's equation, which relates the sources (the charge) with the electric field, is

$$\nabla[\varepsilon\nabla\varphi(\vec{r})] = -\rho(\vec{r}), \tag{1.29}$$

with ρ the charge density at position $\vec{r}$, φ the potential at position $\vec{r}$ and ε the dielectric permitivity, which is considered as homogeneous and independent of $\vec{E}$ in each material. Equation 1.29 is discretized in a 2D rectangular mesh using a a finite differences scheme. The details can be found in [53, 55, 58, 64]. The discretization of the equation in each node of the mesh results in a linear system of equations, which is solved by LU decomposition [71].

1.2.2. Thermal models

In subsection 1.2.1, we have explained the model for the electrical part of the simulation (electric potential and charge transport). In such a model, the temperature is assumed to be constant and used to calculate energy distributions and scattering probabilities. Self-heating effects and their influence on the behavior of the devices is not considered. The devices we will analyze are based on GaN, a wide bandgap semiconductor, and may operate under high-power conditions. Therefore, we need algorithms to study the impact of heating and the associated temperature variation during the simulations. In [56], García-Sánchez summarizes different simulators in which thermal effects are taken into account combined with transport models as MC, hydrodynamic or drift diffusion approaches. In this work, we will use our MC tool self-consistently coupled with two alternative algorithms to update the temperature. Figure 1.10 shows the coupling of the thermal algorithms with the MC tool. The thermal subroutines

are employed after a given number of iterations N_{th}, when the temperature is updated and the scattering probabilities and energy distributions are modified accordingly. The MC algorithm + 2D Poisson solver is ran at the updated temperature during the subsequent N_{th} iterations, after which the temperature is updated again.

In this work, we have employed two ways to model thermal effects: the thermal resistance model (TRM), in which an uniform temperature is considered in the device, and the electrothermal model (ETM), which provides local values of temperature in the device by solving the heat conduction equation (HCE) self-consistently with the electrical MC simulation.

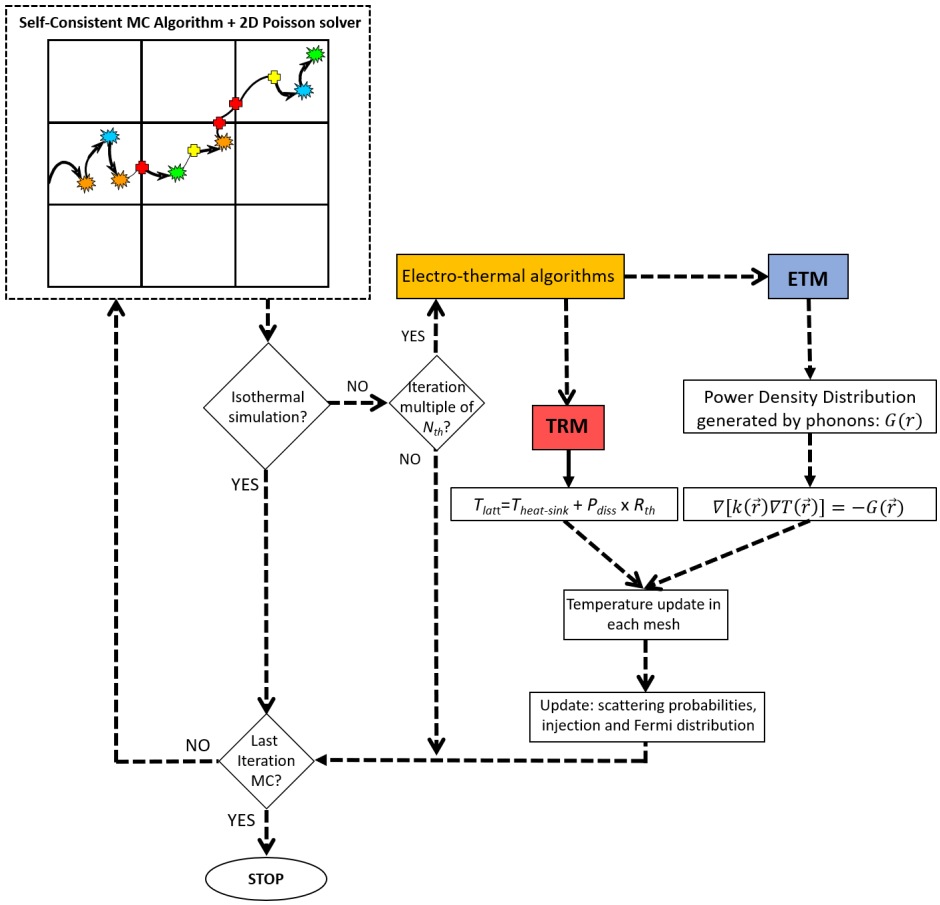

Figure 1.10: Scheme of the coupling of thermal algorithms with the 2D-MC electrical device simulation.

1.2.2.1. Thermal resistance model

In this approach, the whole device is at uniform temperature, calculated considering a linear dependence between the lattice temperature T_{latt} and the dissipated power P_{Diss},

$$T_{latt} = T_{heat-sink} + P_{Diss} \times R_{TH}, \tag{1.30}$$

where $T_{heat-sink}$ is the temperature of the heat-sink, typically the bottom of the device, where the temperature is fixed [72]. P_{Diss} is calculated at each bias point, determined by drain-to-source bias (V_{DS}) and drain current (I_D), with the expression $P_{Diss} = V_{DS} \times I_D$. The power is expressed in W/m because the 2D MC provides currents expressed in A/m. R_{TH} is the thermal resistance of the device, accounting for the temperature rise per W/m [73]. The name is due to the similarity of this parameter with the electrical resistance, since the thermal resistance represents the opposition of the device materials to the heat flow.

1.2.2.2. Electrothermal model

The second model is more accurate, since the update of the temperature is performed with the resolution of the steady-state HCE. In order to solve the equation, the device is also divided in meshes, as shown in Figure 1.11. The thermal domain is delimited in green lines, while the electronic domain corresponds to the yellow shadow. A and C are the horizontal and vertical lengths of the contacts, respectively, and B is the depth of the region not considered in the electronic domain. In the electronic domain, the MC tool records the heat sources by accumulating the increments of energy of the every scattering mechanisms. Afterwards, the HCE is solved in the thermal domain to update the temperature according to the heat dissipation in the device.

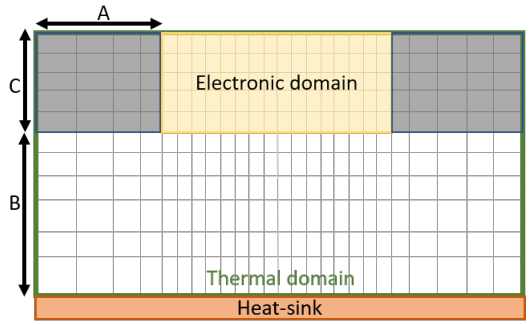

Figure 1.11: Scheme of the electronic and thermal domains and the division of the device into cells.

The ETM couples the MC tool with the resolution of the steady-state HCE [74]

$$\nabla[\kappa(\vec{r})\nabla T(\vec{r})] = -G(\vec{r}), \tag{1.31}$$

where $T(\vec{r})$ and $G(\vec{r})$ are the local temperature and dissipated power density, respectively, and $\kappa(\vec{r})$ the thermal conductivity. In a comparison with the Poisson equation, κ is the equivalent to ε, T the equivalent to the electric potential and G the equivalent to the charge density. The heat sources are only evaluated in the electronic domain by means of the MC simulation as the energy per unit time associated to the net emission/absortion of phonons by the carriers present in each cell. Mimicking the Poisson's solver subroutine, Equation 1.31 is discretized using a a finite differences scheme. Again, the resulting linear system of equations is solved by LU decomposition. In our approach, only a steady-state solution of the HCE can be achieved, because the electronic transport timescale is much shorter than that of thermal phenomena [75]. Figure 1.10 shows the flowchart of the ETM subroutine. Note that we have considered the thermal conductivity independent of the temperature.

Like in the electrical part of the simulation, the thermal one requires of proper boundary conditions. In this case Dirichlet boundary conditions are imposed at the bottom of the device, our heat-sink, a region at fixed temperature. At a surface γ between two regions of different material, Neumann boundary conditions are imposed

$$\kappa_1 \hat{n} \left.\frac{\partial T}{\partial r_n}\right|_{\gamma} = \kappa_2 \hat{n} \left.\frac{\partial T}{\partial r_n}\right|_{\gamma}, \tag{1.32}$$

where κ_1 and κ_2 are the thermal conductivities of each material, $\hat{n}$ the unit vector normal to the boundary surface γ and r_n a vector normal to γ. Additionally, the continuity of T across the border γ must be satisfied [76]. Finally, in the top and side boundaries adiabatic conditions are imposed [31]

$$\kappa_1 \left.\frac{\partial T}{\partial r_n}\right|_{\gamma} = 0. \tag{1.33}$$

1.3. Small-signal characterization

Part of the interest of transistors lies in their high-frequency applications, like the amplification of signals. A physics based model of the high-frequency behavior of transistors is useful in the development of microwave integrated circuits. Such a model, when described in terms of discrete elements, takes the form of an equivalent circuit, which allows studying the influence of the different circuit parameters on the device performance [77]. Moreover, such elements are connected with the physics of the device [78, 79]. In this work, we study the small-signal regime both with simulations and measurements.

1.3.1. Experimental setup

The experimental small-signal characterization of a device is done in terms of S-parameters. The abbreviation S comes from the word scattering. The reason for the use of S-parameters is the convenience to describe a given network in terms of waves rather than voltages or currents when it is working at high frequencies, since it allows an easier definition of reference planes. The S-parameters are a matrix representation of a circuit in terms of incident and reflected power [80]. In particular, a transistor is a four-pole network, which in this description turns into a two-port network. There is an input port (gate) and an output port (drain), assuming the source as ground. The definitions of a four-pole (or two-port) device can be seen in Figure 1.12. The arrows determine the positive directions, a_i and b_i are the incident and reflected waves, respectively, and the dashed lines define the reference planes in ports 1 and 2.

Therefore, in our work the S-parameters are four complex numbers, changing at different frequencies and bias conditions. The matrix representation is:

$$S = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix}$$

Where S_{11} is input reflection coefficient with the output of the network terminated by a matched load, S_{21} the forward transmission (from port 1 to port 2), S_{12} the reverse transmission (from port 2 to port 1), related with feedback effects, and S_{22} the output reflection coefficient. These parameters are defined for a determined characteristic impedance (Z_0) of the ports.

S-parameters are complex numbers with module and phase. The Smith chart is the most common tool for the interpretation of S-parameter measurements [81]. It uses a bilinear Moebius transformation, projecting the complex impedance plane onto the complex Γ plane

$$\Gamma = \frac{Z - Z_0}{Z + Z_0}, \tag{1.34}$$

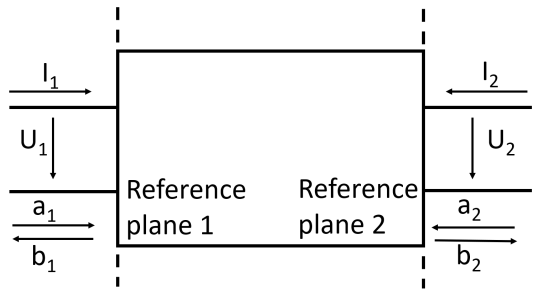

Figure 1.12: Scheme of the four-pole (or two-port) device.

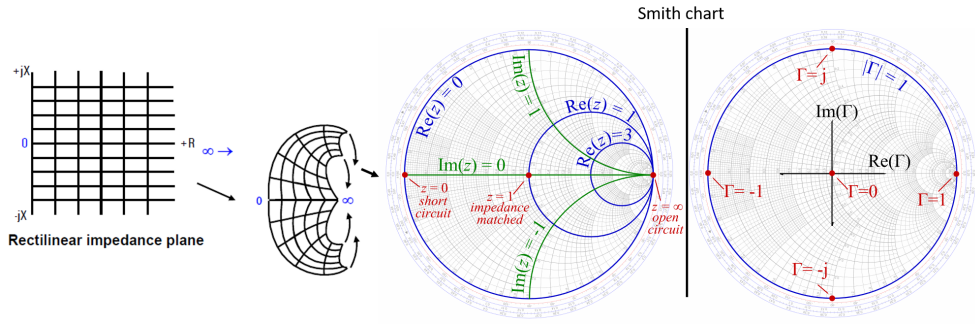

Figure 1.13: Conversion from the positive impedance plane to the Smith chart [82].

with Z the complex impedance of the device under test and Z_0 the characteristic impedance. Figure 1.13 shows how the half-plane with positive real part of the impedance Z is mapped onto the interior of the unit circle of the Γ plane normalized by the characteristic impedance. The upper (lower) part contains the positive (negative) imaginary part impedances.

In essence, impedances are represented by the associated reflection coefficient. The center of the Smith chart corresponds to the characteristic impedance, with a zero reflection coefficient, indicating a matched load ($Z = Z_0$). On the other hand, in the limit of the Smith chart the reflection coefficient is 1. The short circuit ($Z = 0$ and $\Gamma = 1$) is located at the left limit of the horizontal axis, while the open circuit ($Z = \infty$ and Γ =-1) is at the right limit.

In order to measure the S-parameters, we use the VNA N5244A PNA-X of Keysight Technologies presented in subsection 1.1.2. Before the measurements, it is necessary to calibrate the fixtures and cables, with the objective of changing the reference planes from the VNA to the RF probes. Allstron RF probes with a pitch of 100 μm are used. The calibration process requires a calibration, as shown in Figure 1.14(a), with 4 structures: short, open, load and thru (SOLT) [83]. In this work, we have used the guided calibration software including the model parameters of the AC-2 Allstron calibration substrate shown in Figure 1.14(b).

The S-parameters depend on frequency and bias conditions. The frequency dependence is measured with the VNA and the bias conditions are fixed with a SMU for each port. In a two-port device, 2 SMU are necessary. The setup required for the measurements of S-parameters is shown in Figure 1.15. The SMUs are connected to the bias ports of the VNA, which has an internal bias-tee to separate and mix the microwave and DC signals. For these measurements, we need 2 of the 4 ports available in the the VNA. Finally, the micropositioners of the Cascade M150 probe station are used to contact the device through the RF probes.

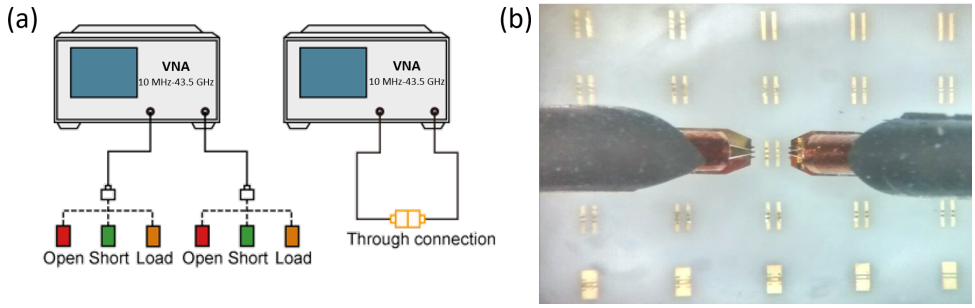

Figure 1.14: (a) SOLT calibration process and (b) Allstron AC-2 calibration substrate.

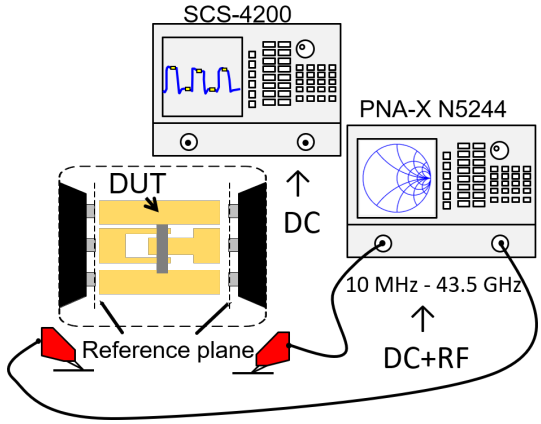

Figure 1.15: Setup used to measure the S-parameters.

These measurements include the effect of the accesses, which must be characterized. The steps followed to extract the equivalent circuit from the S-parameters measurements will be detailed in section 4.1. First, we measure the S-parameters, which are converted to Y-parameters according to the equations of [84]. Finally, the discrete elements of the equivalent circuit are calculated from the Y-parameters. The relations between Y-parameters and elements of the equivalent circuit are provided in section 4.1.

1.3.2. Monte Carlo simulations

By means of MC simulations we can also determine the small-signal equivalent circuit of a given device. In contrast to the experimental characterization, which measures the S-parameters, in the simulations we start from the Y-parameters [85]. To evaluate the Y-parameters of a device, we apply a step change in the bias voltages at the gate and

drain electrodes. A step function contains all frequency components, so that we can evaluate the whole frequency response of the device by taking the Fourier transform of the output signal, which is a transient of current.

The Y-parameters relate the variations of gate and drain current, $i_G(f)$ and $i_D(f)$, with variations in gate and drain voltages, $v_G(f)$ and $v_D(f)$ [58], at each frequency and bias point. Since, we are working with two-port devices, the Y-parameters are 2×2 matrices,

$$\begin{pmatrix} i_G(f) \\ i_D(f) \end{pmatrix} = \begin{pmatrix} Y_{11}(f) & Y_{12}(f) \\ Y_{21}(f) & Y_{22}(f) \end{pmatrix} \begin{pmatrix} v_G(f) \\ v_D(f) \end{pmatrix} \tag{1.35}$$

According the the previous matrix, the parameter Y_{ij} is calculated as

$$Y_{ij}(f) = \left(\frac{i_i(f)}{v_j(f)} \right)_{v_{i,i\neq j}=0}. \tag{1.36}$$

As explained before, the frequency components of $Y_{ij}(f)$ are obtained applying the Fourier transform to the transients of current obtained from voltage steps in MC simulations,

$$Y_{ij} = \frac{\int_0^\infty [I_i(t) - I_i(0)] e^{-j2\pi ftdt}}{\int_0^\infty \Delta V_j e^{-j2\pi ftdt}} = \frac{\int_0^\infty [I_i(t) - I_i(0)] e^{-j2\pi ftdt}}{\frac{j\Delta V_j}{\omega}}, \tag{1.37}$$

where $I_i(0)$ is the stationary current in electrode i before the voltage step, $I_i(t)$ the current response at time t after applying the step and ΔV_j the amplitude of the voltage step in terminal j. From the separation of real and imaginary parts of Equation 1.37 one obtains [86]

$$\Re[Y_{ij}] = \frac{I_i(\infty) - I_i(0)}{\Delta V_j} + \frac{\omega}{\Delta V_j} \int_0^\infty [I_i(t) - I_i(0)] sin(2\pi ft) dt, \tag{1.38}$$

$$\Im[Y_{ij}] = \frac{\omega}{\Delta V_j} \int_0^\infty [I_i(t) - I_i(0)] cos(2\pi ft) dt. \tag{1.39}$$

Since the transient response of the device is limited in time, the integrals of Equations 1.38 and 1.39 are evaluated along a reasonably long time after which it is possible to consider the current as constant and equal to that of the final bias conditions, I_i (∞). Since we study a two-port device, we require two simulations, one applying the step in the gate electrode and other in the drain electrode (noted by index 1 and 2, respectively), to obtain the four parameters of the Y-matrix. We will explain the relations between Y-parameters and elements of the equivalent circuit in subsection 4.1.2.2, where some current transients will be shown.

Chapter 2

Self-Switching Diodes

Self-switching diodes (SSDs) are electronic devices based on the fabrication of two insulating L-shaped trenches on a semiconductor heterolayer, which can be realized with different techniques, like etching or ion implantation. In Figure 2.1(a), the grooves are observed in a front-view of the device. Those trenches break the symmetry of the device and restrict the current flow through the channel. Figure 2.1(b) shows a top view of the device at equilibrium. The effective channel width (W_{eff}) is smaller than the physical width of the channel (W) because of the depletion region around the trenches originated by electrons trapped at surface states present at their sidewalls. When a negative bias is applied to the right terminal with respect to the left one, Figure 2.1(c), the depletion region is increased due to the lateral electric field effect, since the negative voltage reaches the sides of the channel. In contrast, as shown in Figure 2.1(d), a positive bias will reduce the depletion region, because the electrostatic lateral effect counteracts the depletion created by the surface states and, thus, widens the effective channel [17].

SSDs are planar devices which need just one lithographic step for their fabrication. Unlike other technologies like three terminal ballistic junctions, which cannot be easily connected in parallel, SSDs can be located in parallel in the form of arrays with the purpose of reducing the total impedance and lower as much as possible the parasitic effects caused by external connections [11]. On the other hand, the study of the influence of design parameters on the behavior of the devices, like geometry or number of channels in parallel, is a way to improve their performance. Based on the theory described in section 1.1 and the physical model of the device of [87], the main goal of this chapter is to provide global design strategies to enhance the RF responsivity and decrease the NEP of GaN-based SSDs. We will show that the detection capabilities of SSDs are improved by reducing the channel width. However, as a counterpart,

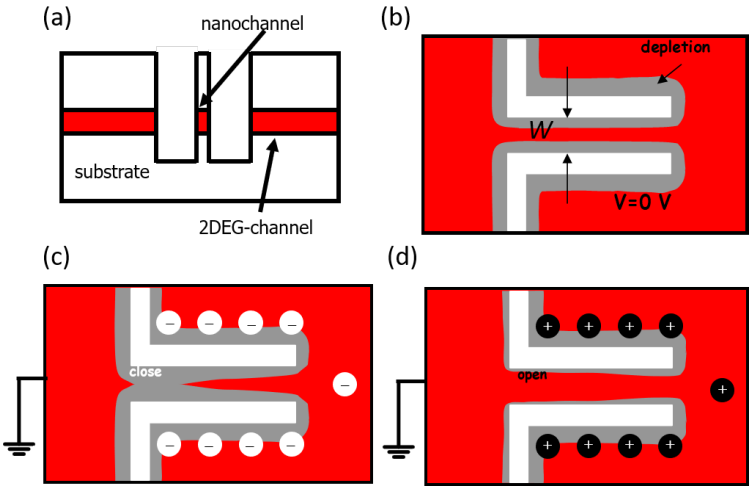

Figure 2.1: (a) Front-view scheme showing the depth of the trenches in a 2DEG heterostructure, allowing the formation of the nanochannel, (b) depletion region originated by the charges located at the walls of the trenches at equilibrium, (c) and (d) redistribution of charges and electrostatic effects for negative and positive bias applied to the right terminal, respectively.

the increase of the surface-to-volume ratio makes more relevant the surface trapping effects, which are analyzed in this chapter.

We will focus on SSDs based on AlGaN/GaN heterostructures operating as detectors in the sub-THz range. In the literature, SSDs have been fabricated with other materials like GaAs [88], InGaAs [89], ZnO [90], organic compounds [91] or graphene [92], some of them devoted to very high-frequency applications thanks to their superior mobility. Although GaN is not the optimal material for very high-frequency applications, detection has been experimentally demonstrated up to 690 GHz in free-space measurements [12]. Additionally, the high-power handling capability of GaN makes it suitable for high-power detection.

The detection capabilities of SSDs can be further improved with the inclusion of a third terminal, a gate, to control carrier concentration in the channel, leading to the so called gated self-switching diodes (G-SSDs) [93], that we will also analyze in this chapter. It is well known that the performance of some detectors in the sub-THz range is improved when they operate at lower temperatures. This enhancement of the detection figures of merit at lower temperatures has already been demonstrated in the literature, *e.g.*, in materials like InGaAs [11]. We will study the behavior in temperature of our GaN SSDs operating as detectors.

Let us note that the use of GaN in SSDs was initially proposed for emission purposes, to operate as free-running Gunn oscillators, based on the predictions of MC simulations [10]. Thus, combined with the detectors analyzed in this chapter, a compact system with a sub-THz source and a detector could be fabricated in the same wafer with the same technology.

2.1. The device

As mentioned before, the devices under test are SSDs based on heterostructures of AlGaN/GaN fabricated on two different substrates, silicon (Si) and silicon carbide (SiC). SiC has a higher thermal conductivity than Si, which makes it a more suitable candidate to be used for higher voltage applications, for example, when looking for Gunn oscillations (which require a very high bias), topic on which the group is working in the last years.

2.1.1. Fabrication

The SSDs were fabricated in the Institut d'Électronique de Microélectronique et de Nanotechnologie (IEMN), University of Lille by the group of Prof. C. Gaquière, based on an AlGaN/GaN heterojunction grown by EpiGaN by means of metal oxide chemical vapor deposition (MOCVD) on a high resistivity silicon (111) or silicon carbide substrate. The Al content changes in the successive fabrication runs from 30 to 35 %. The two dimensional electron gas (2DEG) created in the heterojunction is 25 nm below the surface. The epitaxial layer consists of 5 nm of SiN, around 25 nm of AlGaN, 1.5 μm of GaN and the thickness of the substrate is around 300 μm. Typical values of sheet carrier density n_s measured in these epilayers are in the range 8-12 $\cdot$ 10^{12} cm^{-2}, with a Hall mobility around 1200 cm^2/Vs. The ohmic contacts are formed by fast annealing of Ti/Al/Ni/Au layers at 900 °C, and then devices are isolated either by ion implantation (He^+) or dry etching. Using 240 nm of positive poly (PMMA) e-beam resist thickness and inductive coupled plasma (ICP) chlorine based technology for the etching, we have been able to achieve devices with channels as narrow as 50 nm. Thus, we will compare the performance of devices fabricated on two different substrates and using two different technologies for the definition of the trenches. The last step is the deposition of the top metal layer (Ti/Pt/Au) for the access lines. In Figure 2.2 the schematic of the steps used in the fabrication is shown.

In the case of G-SSDs, for the growth of the gates, an additional fabrication step is necessary. This additional process consists of an initial e-beam writing of the PMMA

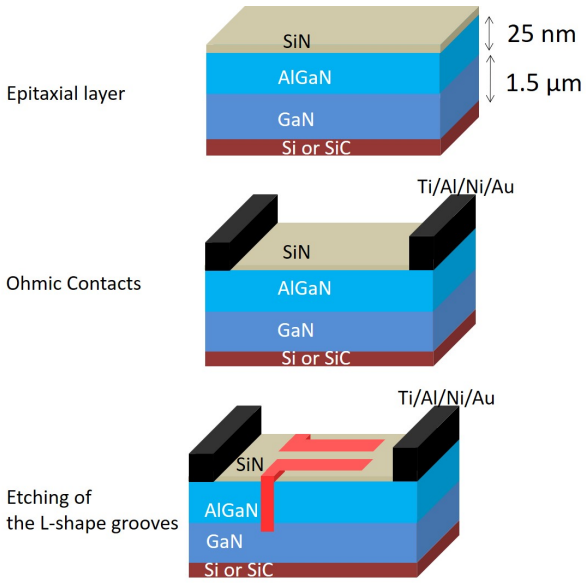

Figure 2.2: Fabrication process flow of an SSD.

and Argon etching, followed by a Ni/Au evaporation (around 40 nm and 300 nm respectively).

2.1.2. Designs and geometries

Three runs of devices have been fabricated with different designs. Two geometries were studied for two kind of applications based on the widths of the channels: (i) for RF detection, rectangular or T-shape SSDs with a narrow channel of width (W) and length (L) [see Figure 2.3(a)], and (ii) for generation of Gunn oscillations, rectangular SSDs with wider channels [see Figure 2.3(b)] and what we call V-shape geometries, where the width is increased along the channel from an opening of W_i at the entrance to W_o at the output [see Figure 2.3(c)]. Additionally, in Run 3, symmetrical channels with both sides fully etched were processed [see Figure 2.3(d)]. In the first run (Run 1) only Si substrates were used, like the one shown in Figure 2.4(a), following the technical process explained in the previous subsection. The devices of Run 1 show a slight fall in the DC current at increasing applied voltages, which in principle could be attributed to Gunn oscillations. However, after a deep analysis, reported in section 2.2, it is shown to be due to a combination of thermal and trapping effects.

In the second run (Run 2), devices on SiC substrate, shown in Figure 2.4(b), were also fabricated. Thanks to the higher thermal conductivity of SiC compared with Si, the use of higher voltages in the search of Gunn oscillations was possible. In the wafer

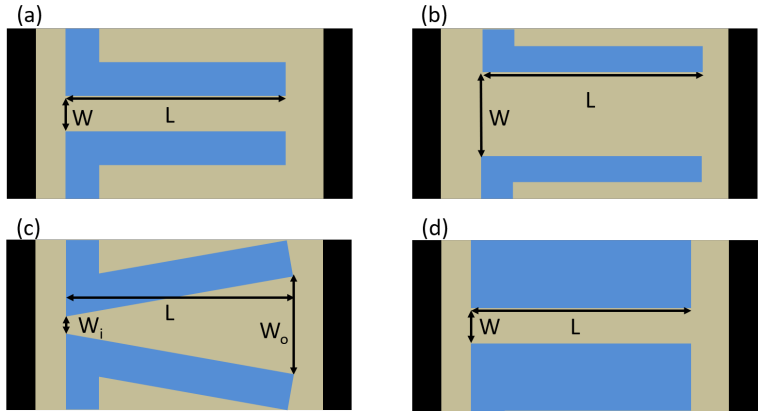

Figure 2.3: (a) T-shape or rectangular narrow SSD with a channel of width W and length L, (b) rectangular wide channel, (c) V-shape SSD with a channel of length L and opening W_i at the entrance and W_o at the output and (d) symmetrical channel with both sides fully etched.

of Run 2 a more advanced device was proposed. A top gate just on top of the channel was fabricated as shown in Figure 2.4(c), defining the so-called Gated-SSDs (G-SSDs). Unfortunately, the G-SSDs of Run 2 were designed without RF accesses, so that on-wafer measurements with RF probes were not possible. Nevertheless, G-SSDs with antennas were fabricated for free-space RF measurements. The main task developed in this Run 2 was, by exploiting devices with DC pads, a measurement campaign at DC level to identify the best candidates for detection.

The third run (Run 3) included devices fabricated on both substrates (Si and SiC). The main novelty was the improvement of the isolation in the gate of G-SSDs and the inclusion of an aluminum nitride (AlN) spacer in one of the SiC wafers in order to improve the confinement of the carriers at the AlGaN/GaN interface, now AlN/GaN [see Figure 2.4(d)]. In Run 3, both SSDs and G-SSDs with dedicated RF accesses and bow-tie antennas were fabricated to allow their characterization both under on-wafer RF probes and in free-space configuration.

According to the topology and optimizations of the devices in the different runs previously explained, their dimensions and the observed effects, different kind of electrical characterizations from DC to RF, and also free-space measurements, were done. A small summary of the geometries, dimensions and number of channels in parallel of the SSDs studied in this thesis corresponding to each Run is presented in Table 2.1.

Finally, two type of accesses in the characterization of the SSDs and G-SSDs are used (see Figure 2.5). CPW accesses are fabricated with a 30 μm signal line and a 20 μm spacing in order to provide a 50 Ω characteristic impedance [46]. The

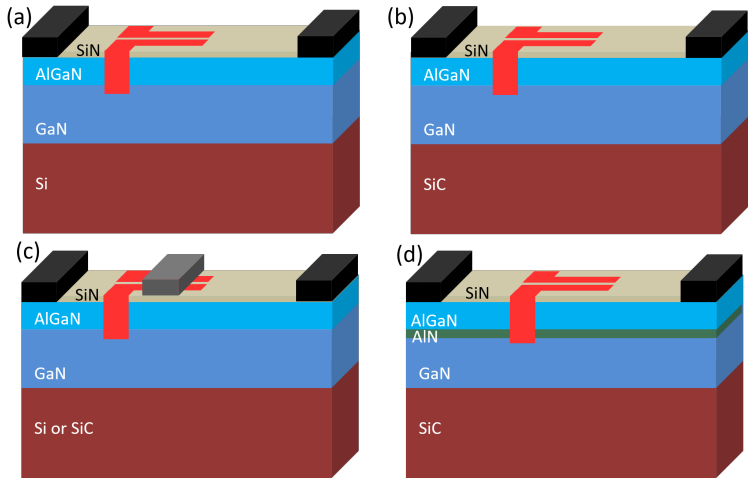

Figure 2.4: Topology and heterostructure of the SSDs with (a) Si substrate, (b) SiC substrate, (c) gate and (d) AlN spacer between the AlGaN and GaN layers.

# Run	Geometries	W (nm)	L (nm)	N	G-SSD
1	Narrow T-shape	50, 74	1000	1	no
	Wide T-shape	500	2000	1	
	V-shape	W_i = 250 - W_o = 550	1000	1	
2	Narrow T-shape	74, 100, 200	1000	1, 4, 8, 16	(bow-tie antenna)
	Wide T-shape	-	-	-	
	V-shape	W_i = 300 - W_o = 400	1000	-	
3	Narrow T-shape	100, 200	1000, 2000	1, 4, 8, 16	(bow-tie antenna & CPW accesses)
	Wide T-shape	-	-	-	
	V-shape	-	-	-	

Table 2.1: Summary of the devices of each run that have been characterized in this thesis attending to the geometries, dimensions and number (N) of diodes in parallel.

setup shown in Figure 1.5 is the adequate to perform the measurements with CPW accesses. Devices with bow-tie antennas with a frequency range of application between 83 and 700 GHz [94] (length 720 μm and width in the center 4 μm) are characterized with the setup of Figure 1.7. For both type of devices, we carry out DC and pulsed characterization with the setup of Figure 1.1.

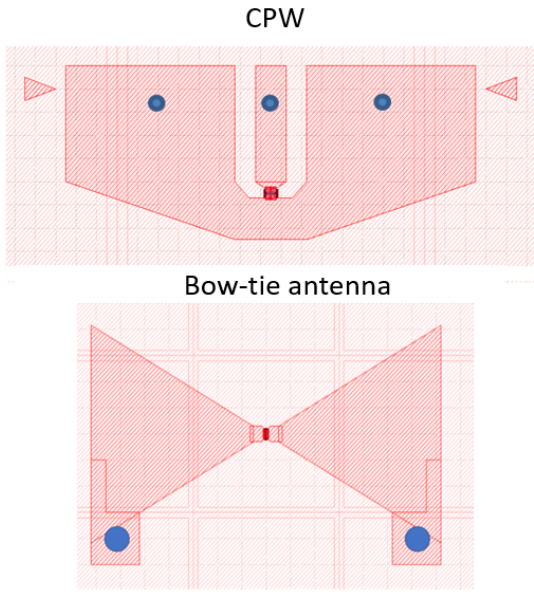

Figure 2.5: Schematic picture of the accesses used in the characterization of the devices. CPW and broadband bow-tie antennas are used in the RF characterization.

2.2. Run 1: Trapping effects in SSDs

When the SSDs fabricated in the first run were tested, relatively poor responsivity values along with unexpectedly low cutoff frequencies were obtained, presumably due to the presence of traps. Since trapping effects are limiting the performance of these devices, we decided to analyze such phenomena instead of focusing on RF detection.

First of all, just remind that only a Si-substrate wafer was available. We start the DC characterization of the devices with the current-voltage (I-V) curves. We analyze two narrow rectangular SSDs (W = 50 nm) with different channel length (L = 1000 nm and 2000 nm). A first inspection of the DC curves reveals a drop in the current for high-enough applied voltages (see Figure 2.6). This effect, called negative differential resistance, is usually associated with Gunn oscillations [95]. However, when a deeper study is done, the origin of the phenomenon is not so evident. It is well known that thermal and trapping effects can also induce a decrease in the current, similar to that observed in Figure 2.6 [6, 10]. Indeed, when a dual sweep of the I-V curve is measured, hysteresis curves are found, typically associated to trapping effects. We attribute the hysteresis to charges that are trapped and de-trapped in surface states at the sidewalls of the trenches or in the bulk of the GaN layer, as we will explain in the following.

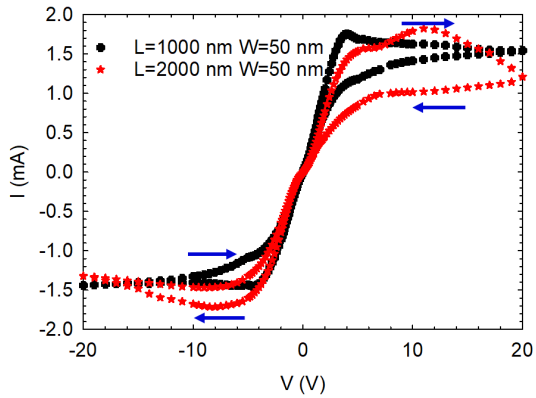

Figure 2.6: DC current-voltage characteristics of two narrow diodes (W = 50 nm) with different length (L = 1000 nm and 2000 nm). Measurements are performed in dual-sweep, arrows indicate the direction of the measurement.

The presence of surface and bulk traps in GaN devices leads to a limited reliability of the devices. Bulk traps induce well known effects like current collapse or drain and gate lags in FETs [21]. In our case, the channel of the SSDs was designed to be very narrow to obtain high responsivities [87], what means that the surface-to-volume ratio increases significantly. As a result, trapping effects at the lateral surfaces of the channel are expected to be quite relevant. In particular, carriers near the etched walls, will interact with the surface traps, thus afecting the performance of the SSD as detector. The influence of these trapped charges could also be the explanation of why up to now we could not observe Gunn oscillations in our GaN SSDs. To mitigate the effects of the sidewalls and solve this issue, V-shape structures have been proposed as an alternative to the rectangular ones (T-shape) [96].

2.2.1. Pulsed I-V measurements

To distinguish the influence of traps in competition with thermal effects, the I-V curves of several arrays of SSDs with different channel width were measured under pulsed conditions. This type of measurement allows to reduce thermal effects and helps identifying the characteristic times of the traps. The employed duty cycle is 1 %, with a minimum pulse width of 1 μs and a maximum pulse width of 10 s, limited by the equipment specifications for the voltage and current ranges used in these measurements. In Figure 2.7 we show an schematic picture of the pulsed measurement setup, where we have indicated the definition of the pulse width, the period and the duty cycle. Together with pulsed measurements, AC impedance measurements were done, in order to study the changes in conductivity induced by these mechanisms.

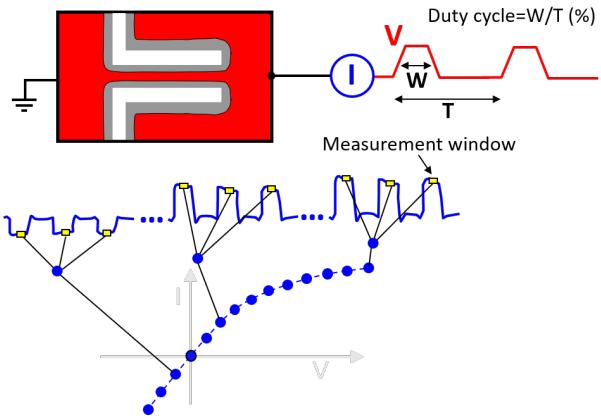

Figure 2.7: Schematic picture of the pulsed measurement setup for the SSD.

A relatively narrow SSD ($L = 1000$ nm and $W = 75$ nm) was selected for intensive study. Figure 2.8 shows the measured I-V curve for different pulse widths (1 μs and 10 s). As observed, for a long pulse width (10 s) a significant increase in the measured current takes place for high-enough applied voltages. For short pulses (1 μs) the current saturates due to the fast trapping of electrons in states at the sidewalls of the channel. Such electrons are partially released at longer times in the case of long pulses of high-enough amplitude, thus increasing the width of the effective conducting channel and allowing a higher current to flow. The threshold voltage for the described effect to take place is smaller in reverse (V <-3 V) than in forward bias (V > 5 V), reflecting the asymmetry of the diodes. Note that self-heating effects would provide the opposite behaviour, i.e., higher current for the shortest pulse width.

To estimate the time constant of the traps, the pulsed current-voltage characteristics were recorded for several values of pulse widths (from 1 μ s to 10 s). Then, the value of current at different applied voltages is analyzed it as a function of the pulse width (in a similar way to a transient study). Figure 2.9(a) shows the reconstructed "transients of current", revealing that for a voltage higher than 5 V (or smaller than -3 V in reverse voltage) a transition from a lower state of current (in shorter pulses) to a higher state of current (in longer pulses) is induced.

In order to study the characteristic times of the phenomenon, the transients of current are fitted to the following model

$$I(t) = I_0 + (I_\infty - I_0)e^{(-\frac{t}{\tau})}, \tag{2.1}$$

where I_0 is the low state of current, I_∞ is the higher state of current and τ the time of detrapping, which is the degree of freedom of the model [22]. In Figure 2.9(b), τ is plotted versus the bias voltage. As observed, the characteristic times are smaller

for higher voltages. Interestingly, for low voltages, the detrapping time is shorter in forward bias, however, the decrease with the voltage is more pronounced in reverse than in forward bias, so that for the highest applied voltages ($|V|$ >13 V), τ is shorter in reverse bias. Regarding the decrease of τ with the increase of voltage (in absolute value), it is to be noted that the potential barrier is narrower as the bias increases, and therefore trapped-charge release through tunneling is easier, thus explaining the decrease of the characteristic time. Note that τ is always at least two orders of magnitude higher than the typical times of self-heating mechanisms [75], which means that,

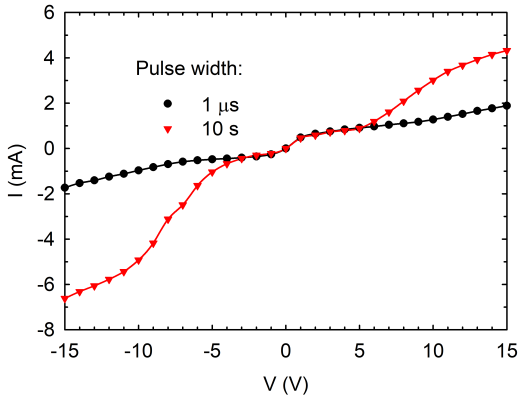

Figure 2.8: Pulsed current-voltage characteristic of an array of 16 SSDs in parallel, with L = 1000 nm and W = 75 nm, measured with two different pulse widths, 1 μs (in black) and 10 s (in red). The duty cycle is 1 %.

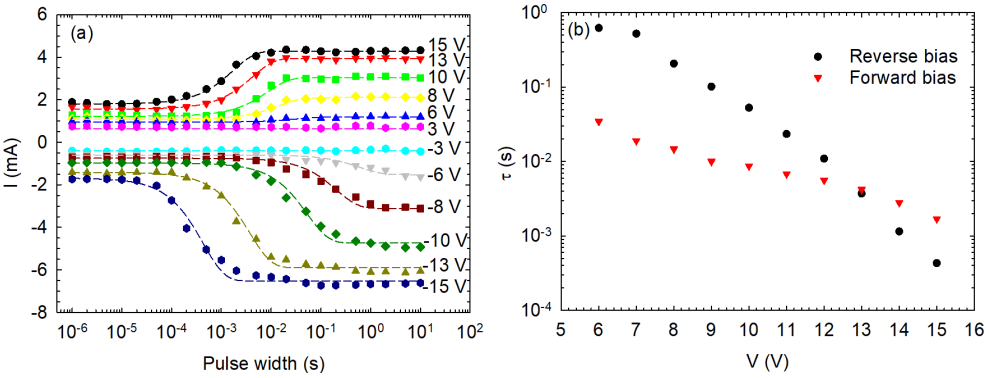

Figure 2.9: (a) Symbols: measured current *vs.* pulse width for different bias conditions. Dotted lines: fitting of the measurements to Equation 2.1. (b) Detrapping time constant extracted from the fittings in (a) *vs.* applied voltage.

even if thermal effects can be present in the SSDs within the range of times covered by τ, the observed time dependence is not associated to heating effects.

The observed effects are attributed to trapping/detrapping of electrons at the states present at the sidewalls of the trenches that define the channel, originated by the etching process. As it was explained in the introduction, surface charges at the walls deplete the channel. At equilibrium, the surface charges produce a depletion region near the interfaces of about 30 nm at each side of the channel, value determined by the method that will be explained in subsection 2.3.3, based on resistance measurements of SSDs with different widths [97]. Since the channel width in this channel is $W = 75$ nm, it is near to be completely depleted, its current level is low and the influence of the occupancy of surface states is very strong, since they modify quite noticeably the width of the conducting channel. If the width of the channel is increased, it is expected that such an influence is reduced. In order to verify this fact, it is necessary to compare this narrow channel diode with wider ones, where the influence of surface states is expected to be weaker because of the smaller surface-to-volume ratio. As wide-channel diodes we have selected a rectangular one ($L = 2000$ nm and $W = 500$ nm) and a V-shape one ($L = 1000$ nm, $W_i = 250$ nm and $W_o = 550$ nm). The current-voltage characteristics of the rectangular diode are shown in Figure 2.10(a) and those of the V-shape diode in Figure 2.10(b). As expected, in the I-V curves of both diodes, the effects observed in Figure 2.8 for the narrow channel are absent. Here, the current level obtained with the longer pulses is smaller than that reached with the shorter ones. In these wider channels, surface effects are much less important and we attribute the observed behavior to the influence of both bulk traps and heating effects.

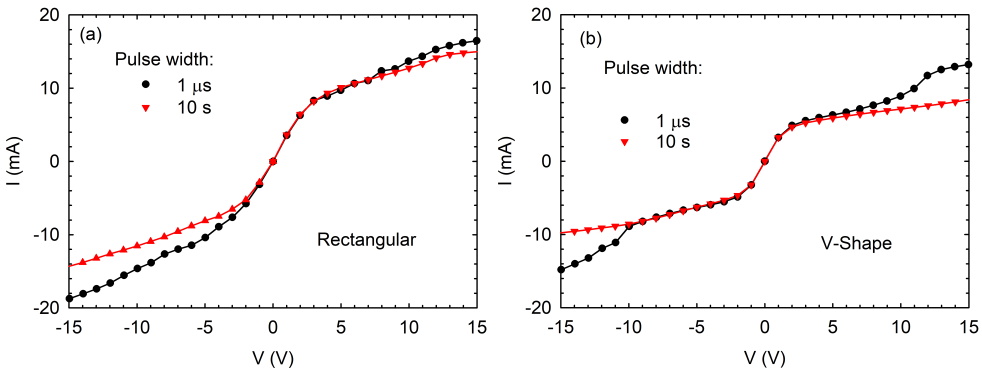

Figure 2.10: Pulsed current-voltage characteristics of an array of (a) 16 wide rectangular SSDs in parallel with $L = 2000$ nm and $W = 500$ nm, and (b) 16 V-shape SSDs in parallel with $L = 1000$ nm, $W_i = 250$ nm and $W_o = 550$ nm. Two pulse widths are considered: 1 μs (in black) and 10 s (in red).

2.2.2. AC impedance measurements

The transient behavior of the zero-bias AC impedance of the diodes measured after applying a voltage pulse can provide useful information about the trapping/detrapping processes taking place in the devices and their characteristic times. We have measured the zero-bias AC impedance (at 100 kHz with 30 mV_{rms}) just after applying pre-pulses of different widths (T_0) and amplitudes (V_0) to the narrow-channel SSDs of Figure 2.8. Figure 2.11 shows the schematic sketch of this setup, where we highlight the width and amplitude of the pre-pulse and the subsequent measurement window once the pulsed has finished.

In Figure 2.12(a) the AC impedance transients after the application of pre-pulses of constant width ($T_0 = 10$ ms) and varying amplitude are shown, while in Figure 2.12(b) it is the amplitude which is kept constant ($V_0 = 10$ V) and the width changes. The (steady-state) AC impedance without a pre-pulse (at equilibrium) is also shown for comparison. Surface states are known to be charged when the current flows through the diodes, thus decreasing the current and producing a hysteretic behavior in the *I-V*, which shows long-lasting memory effects (even of some minutes duration) due to the large release time of such traps [98, 99]. The measurements of the AC impedance shown in Figure 2.12 are coherent with this behavior.

The initial high values of the impedance (as compared with that at steady state) obtained in all cases for the shortest times are attributed electrons trapped in surface and bulk states due to the application of the pulse. For a given applied voltage, such increase is more pronounced in forward than in reverse bias because in the forward the lateral field effect pushes the electrons towards the sidewalls. Once the pulse finishes, in case the amplitude was not high enough to release electrons from the surface states during the application of the pulse, a slow decrease of the impedance due to the detrapping of electrons is observed. In contrast, for pulse amplitudes high-enough to release electrons from surface states when the pulse width is 10 ms (see Figure 2.9), an increase of the impedance at short times (some tenths of second) takes place, during which electrons are trapped again in those states, for then decreasing at a much longer time scale as in the previous case (detrapping of electrons). This interpretation is corroborated by the fact that when the measurement is done under

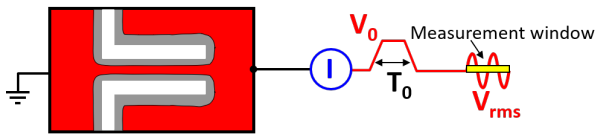

Figure 2.11: Schematic sketch of the C-V impedance measurement setup for the SSD.

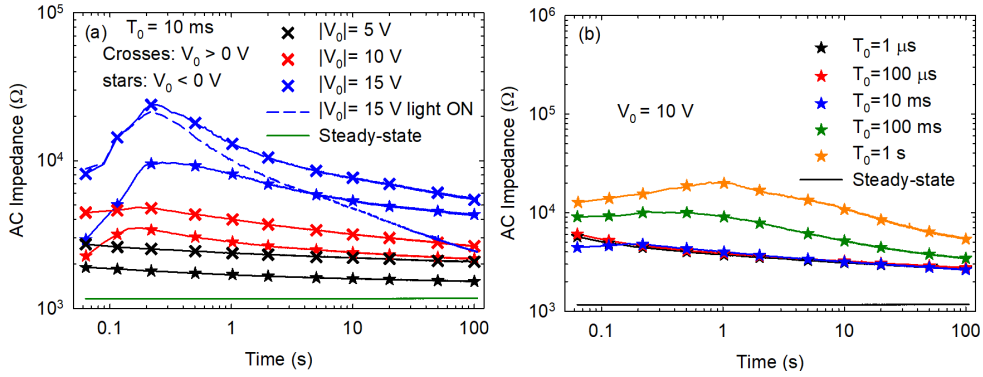

Figure 2.12: Zero-bias AC impedance transients measured just after the application of pre-pulses of (a) width $T_0 = 10$ ms and different amplitudes V_0 in forward and reverse bias and (b) amplitude $V_0 = 10$ V and different widths T_0 to the narrow-channel SSDs of Figure 2.8. The steady-state value (at equilibrium) is also shown for comparison.

illumination, the behavior at short times, attributed to trapping of electrons, does not change, while the detrapping taking place at longer times becomes accelerated by the presence of the light. It is interesting to highlight that the initial increase of the AC impedance becomes noticeable for smaller pulse amplitudes in reverse that in forward bias.

When the amplitude of the pulse is fixed to 10 V while its width is modified, Figure 2.12(b), for the shorter pulses ($T_0 < 10$ ms) the behavior of the AC impedance is essentially the same since no previous release of surface electrons takes place. However, for longer pulses, the initial trapping of electrons at the surface states becomes visible. As the width of the pulse is enlarged, for more electrons were previously released, the increase in the AC impedance is more pronounced and persists for longer times.

In order to check the importance of trapping effects in wider devices, where the surface-to-volume ratio is smaller, measurements of the zero-bias AC impedance, changing the width (T_0) and amplitude (V_0) of the pre-pulse, were also done in the wide rectangular SSDs and V-shape SSDs of Figure 2.10. Figure 2.13(a) shows the AC impedance transients measured in the V-shape diode with a pre-pulse of fixed width ($T_0 = 10$ ms) and different amplitudes ($|V_0| = 10$ V and 15 V). As observed, the increase in the impedance is smaller than in the narrow diodes. Indeed, the initial value of the impedance is around 300 Ω, while in the narrow ones was around 1 kΩ. A similar result is obtained in Figure 2.13(b), where the amplitude is fixed ($V_0 = 10$ V) and the pre-pulse width decreased down to 1 ms in the same V-shaped diode. For $T_0 = 10$ ms, it is to be noted a tiny increase of the impedance at the beginning of the transient, associated to the trapping of electrons previously released, as also found

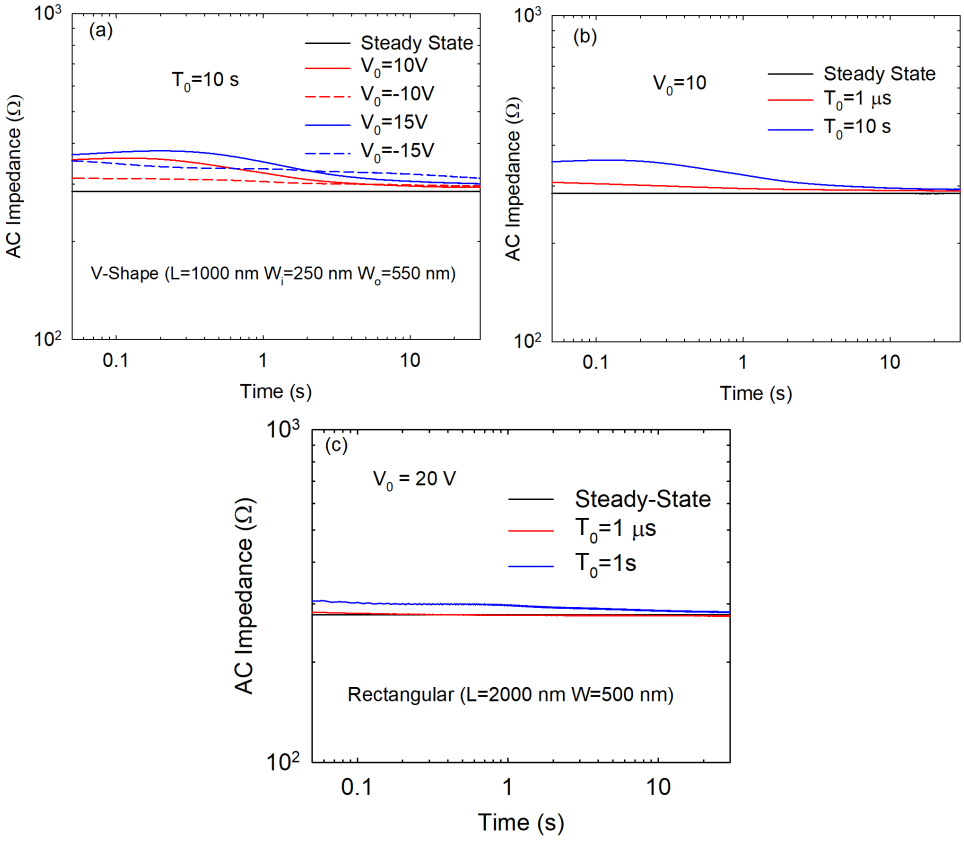

Figure 2.13: Zero-bias AC impedance transients measured just after the application, to the wide-channel diodes of Figure 2.10, of pre-pulses with: (a) and (c) constant T_0 and different V_0 and (b) constant V_0 and different T_0. (a) and (c) correspond to the V-shape diode and (b) to the wide rectangular one. The steady-state value measured without the pre-pulse is also shown for comparison.

in the narrow-channel diode. On the other hand, in the wide rectangular diode, Figure 2.13(c), the increase of the impedance is similar to that found in the V-shape diode; however, no increase of the impedance was observed at the beginning of the transient, confirming the scarce influence of trapping/detrapping mechanisms at the surface states in wide-channel diodes. We conclude that only in very narrow channels the surface states play an important role in the conduction and lead to the hysteretic behavior observed in the I-V curves.

2.3. Run 2: Detection in SSDs

In this section we will focus on one of the main objectives of this chapter, the use of the SSDs as zero-bias RF detectors.

2.3.1. State of the art

First of all, we summarize the state-of-the-art of RF detectors based on different devices and materials, paying special attention to SSDs and GaN. In 1997 a HFET was the first GaN device proposed for microwave detection [100], with responsivities in the order of tens of V/W and a maximum measured frequency of 20 GHz. To have a better overview of the current work in mm and sub-mm wave detectors, Table 2.2 shows the figures of merit, technologies and authors of various FETs, barrier diodes (including Schottky Barrier Diodes (SBDs)) and devices based on nanowires operating as detectors.

In [13], the authors study the detection with GaN HEMTs, which have maximum currents of 70 A/m. For the characterization, they used an Impact Avalanche Transit Time (IMPATT) diode emitting at 0.14 THz in a free-space setup. In [101], the device used as detector is an InGaAs FET with maximum current of 3 mA ($V_{GS} = 0$ V). The characterization is also done with a free-space setup and a backward wave oscillator at 615 GHz as a source. Currently, SBDs are the detectors showing higher responsivities like the InGaAs SBD of [102], where a responsivity around 16 kV/W is measured. The heterojunction backward diode of [103] exhibits bowing coefficients around 40-50 V^{-1}, higher than the theoretical maximum bowing coefficient of a Schottky Barrier Diode. The authors used an Agilent N5250C Vector Network Analyzer (10 MHz-110 GHz) as source and they characterized the detection with a RF on-wafer probes setup similar to that described in subsection 1.1.2. In [104], the authors show that their Fermi Level Managed Barrier Diode (FMB diode) was developed for achieving broadband and low-noise THz detection by controlling the barrier. A pre-amplification module designed by the authors improves the detection of the integrated FMB diode.

Devices based on more novel materials exhibit smaller reponsivities compared with the very high values of the previous ones. Between these devices, there are graphene FETs (G-FETs) and InN nanowires with responsivities in the order of units of V/W. In [105], the authors find that the non-linearity of G-FETs provides a lower responsivity than the previous technologies. Again, an on-wafer setup similar to that explained in subsection 1.1.2, with an Agilent 8275D signal generator in the 1-67 GHz band and a Keithley 2000 multi-meter, is used. In [106], the studied InN nanowires conduct a very small current (around tens of μA) and their bowing coefficient is also small, revealing low values of the responsivity. For the THz detection characterization, the

Technology	Responsivity	Frequency	NEP	Author
GaN HEMT	15 kV/W	140 GHz	1 pW/Hz$^{1/2}$	H.W. Hou [13]
G-FET	100 V/W	67 GHz	40 pW/Hz$^{1/2}$	M.A. Andersson [105]
InGaAs FET	1.1 kV/W	615 GHz	9 pW/Hz$^{1/2}$	V.V. Popov [101]
InGaAs SBD	16 kV/W	88 GHz	0.39 pW/Hz$^{1/2}$	M. Hoefle [102]
Fermi Level Managed Barrier Diode	1.1 kV/W	300 GHz	3 pW/Hz$^{1/2}$	H. Ito [104]
Heterojunction Backward Diode	4.6 kV/W	94 GHz	0.18 pW/Hz$^{1/2}$	Z. Zhang [103]
InN nanowires	1.1 V/W	290 GHz	-	X. Chen [106]

Table 2.2: Summary of figures of merit for detection with different technologies and materials.

authors used a 30 GHz AV1450C signal generator and frequency multipliers, resulting in a 290 GHz output wave. The used free-space setup is similar to that explained in subsection 1.1.2.

GaN HEMTs are among the devices providing higher reponsivities, in the order of units or tens of kV/W. A good review of the capabilities of GaN for THz technologies is provided in [107], including applications like generation, detection, mixing and multiplication of THz or sub-THz waves, by using devices like quantum cascade lasers, NDR diodes, SBDs, IMPATTs or HEMTs.

Focusing on the devices analyzed in this work, Table 2.3 reviews the milestones achieved in the main figures of merit measured in SSDs fabricated with different materials. As shown, SSDs have been able to detect signals of frequencies up to 2.5 THz (at 10 K) and to exhibit responsivities as high as 300 V/W (biased at 0.1 μA).

Material	$\beta_{50\Omega}$	Frequency	$NEP_{50\Omega}$	T	Author
GaAs	150 V/W; 300 V/W (zero bias; $I = 0.1$ μA)	1.5 THz	330 pW/Hz$^{1/2}$; -	300 K	C. Balocco [88]
ZnO	0.9 V (4 V_{rms})	30 MHz	-	300 K	M. Y. Irshaid [90]
InGaAs	8 V/W	2.5 THz	-	10 K	C. Balocco [108]
	160 V/W	110 GHz	63.5 pW/Hz$^{1/2}$	300 K	C. Balocco [89]
InAs	17 V/W	50 GHz	150 pW/Hz$^{1/2}$	295 K	A. Westlund [87]
Graphene	3.9 V/W	67 GHz	2.2 nW/Hz$^{1/2}$	300 K	A. Westlund [92]
GaN	30 V/W	325 GHz	280 pW/Hz$^{1/2}$	300 K	P. Sangaré [109]

Table 2.3: Summary of figures of merit for detection in SSDs fabricated with different materials.

In this dissertation, we characterize GaN-based SSDs. In previous works, both on-wafer measurements and free-space measurements have been performed. In [109], detection capabilities of GaN SSDs were evaluated by means of on-wafer measurements. A VNA with frequency extenders for G and J bands, 140-220 GHz and 220-325 GHz respectively, was used as signal source. Responsivities around 30 V/W were measured in these bands. In [12], the authors performed free-space measurements in 0.28-0.38 THz and 0.64-0.69 THz bands. This work demonstrated that the SSD still detects signals of frequencies as high as 690 GHz.

2.3.2. Topology of the SSDs under analisys

In the second run (Run 2), wafers with two kind of substrates, Si and SiC, were available. The diodes fabricated on the Si substrate had extremely narrow channels and were almost closed, so we have barely measured them. Fortunately, in the other wafer with a substrate of SiC, the initial results showed a much better behavior and a good agreement between RF and the quasi-static (QS) model, which was explained in subsection 1.1.1. Remember that this model, based on the prediction of the figures of merit extracted from I-V measurements, allows us to search and select the best candidates for RF detection. Afterwards, an intense campaign of measurements in devices with different characteristics, like number of channels in parallel N, channel length L and width W, was done to find the best SSDs for detection applications. In Table 2.4 a summary of the measured geometries is given.

As an example to illustrate the performance of these devices as detectors, we present experimental measurements of a SSD consisting in one single channel of $L = 2$ μm and $W = 100$ nm. The set-up presented in Figure 1.5 with the CPW accesses shown in Figure 2.5 has been used for the on-wafer characterization of the RF detection capability of the device. Measurements in the frequency ranges 0.01-43.5 GHz and 140-220 GHz (G-band) were carried out, in the upper band at the IEMN. Figure 2.14 reports the results for $\beta_{50\Omega}$. The input power is 1 mW in the 0.01-43.5 GHz band, while for the 140-220 GHz band it is between 1 and 10 μW. In the lower band, $\beta_{50\Omega}$

# Run	Geometry	W (nm)	L (nm)	N
1	Narrow T-shape	74	1000	1
2	Narrow T-shape	74, 100, 200	1000	1, 4, 8, 16
	V-shape	W_i = 300 - W_o = 400	1000	1, 4, 16, 64

Table 2.4: Geometry, channel width W and length L, and number of channels in parallel N of the SSDs fabricated on SiC substrate that were measured.

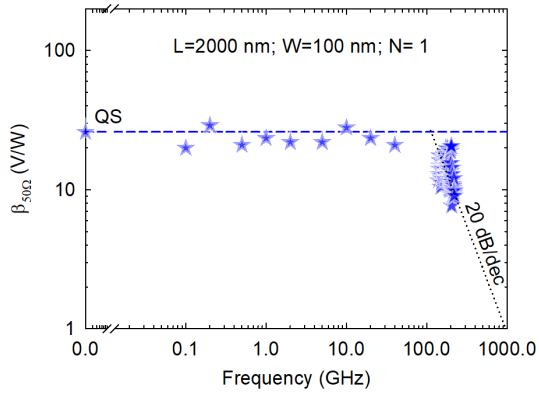

Figure 2.14: Log-log plot of $\beta_{50\Omega}$ *vs.* frequency measured in a SSD with just one channel of length $L = 2$ μm and width $W = 100$ nm. The horizontal dash line and the star at the lowest frequency represents the QS value of $\beta_{50\Omega}$.

remains practically constant at a value of 30 V/W. For higher frequencies in the upper band, $\beta_{50\Omega}$ drops from the initial value but it is still significant. As observed, a very good agreement with the prediction of the QS model is achieved in the low-frequency range, which will be exploited to analyze the performance of SSDs with different topologies in next subsections.

2.3.3. Number of diodes, width and length

In the following, we compare the results of the QS model with experimental measurements. The QS model is able to satisfactory predict the detection capability of SSDs, like it has been demonstrated in subsection 2.3.2. To obtain the detection figures of merit we just have to measure the DC *I-V* curves, like those shown in Figure 2.15. They correspond to SSDs coming from Run 2, with $W = 100$ nm, $L = 1$ μm and different number of channels in parallel N. Figure 2.15(a) evidences the decrease in the resistance of the SSDs when N increases. If we normalize by N, Figure 2.15(b), we can check the very good scaling of the current level, revealing the mature technology of our process within this Run 2. Note the asymmetry found in the different values of the current between direct and reverse bias.

By means of the model previously described in subsection 1.1.1, firstly the resistance of a single channel, $R_0^{SC} = dV/dI$, is obtained for every width of the channel. R_0^{SC} increases when reducing W. If the channel is narrow enough, it will be totally closed because of the lateral depletion, this is, $I = 0$ A, infinite R_0^{SC}, and $1/R_0^{SC}$ equal to 0. This allows us to estimate the lateral depletion width, W_d, induced by the charges in the sidewalls of the channel at equilibrium by extrapolating to zero the

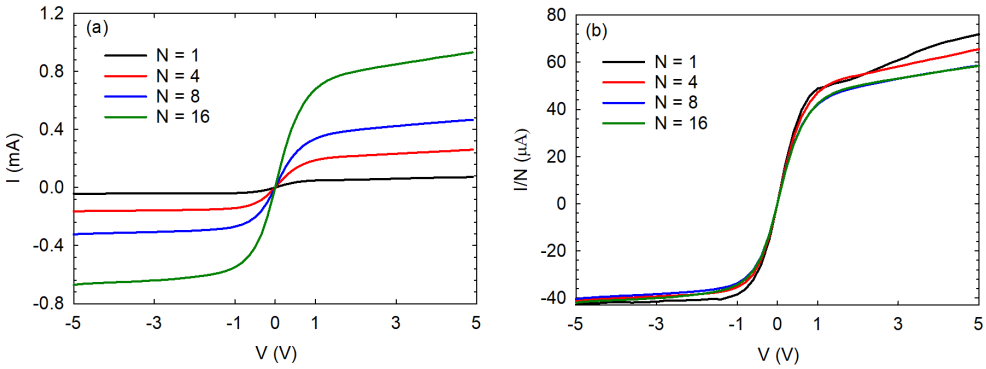

Figure 2.15: (a) Current-voltage characteristics of SSDs with $L = 1$ μm, $W = 100$ nm and $N = 1$, 4, 8 and 16 (b) Current normalized by the number of channels in parallel N.

representation of $1/R_0^{SC}$ as a function of W (see Figure 2.16). Note that these trap effects were deeply studied in Section 2.2. The effective width of the channel is defined as W_{eff} =W-2·W_d. The value extracted for W_d in the devices of Run 2 is around 25 nm, what means that the narrowest devices within this Run, with $W = 50$ nm, were completely closed and are not operative at all. On the other hand, the bowing coefficient, γ, is computed from the second derivative of the I-V curve (see Equation 1.7). This parameter is related with the curvature of the I-V characteristic or, in other words, the non-linearity. Considering as a fair approximation that the SSD behaves as an ideal MOSFET, as proposed in [92], γ should be proportional to $1/W_{eff}$, while $1/R_0^{SC}$ has to scale proportionally with W_{eff}. In Figure 2.16, the expected dependencies are confirmed for both the resistance and the bowing coefficient.

The figures of merit depend not only on the width but also on the number of channels in parallel N, which has to be optimized. Basically, because a higher N means a smaller $R_0 = R_0^{SC}/N$ and a higher current, leading to a constant γ. This result is clearly observed in Figure 2.17, where R_0 and γ are plotted as a function of N. Increasing N, R_0 decreases from 30 kΩ ($W = 74$ nm and $N = 1$) to 20 kΩ ($W = 74$ nm and $N = 16$), and from 4 kΩ ($W = 200$ nm and $N = 1$) down to 200 Ω ($W = 200$ nm and $N = 16$). On the other hand, for each channel width, γ is constant with N and, interestingly, the narrower the channel, the higher γ. Values change from 0.5 V^{-1} (W = 74 nm) to 0.1 V^{-1} (W = 200 nm).

The optimal responsivity, defined in a single channel by substituting R_0^{SC} in Equation 1.8, depends as well on the topology of the device. Concerning the width, according to the trend followed by R_0^{SC} and γ, we have that $\beta \approx 1/W_{eff}^2$. However, the impedances of SSDs are some orders of magnitude higher than the most common transmission line standard $Z_s = 50$ Ω, so that in a real RF measurement the respon-

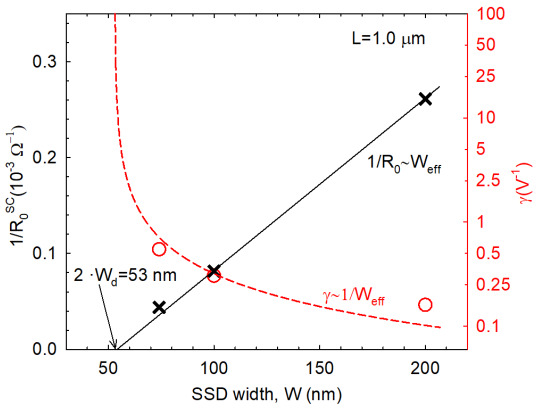

Figure 2.16: $1/R_0^{SC}$ (left axis) and γ (right axis) extracted from the QS model as a function of the channel width. The black and red lines correspond to the trends W_{eff} and $1/W_{eff}$, respectively. SC stands for single channel.

sivity defined by Equation 1.8 has to be modified by the influence of the mismatch, which is calculated according to Equation 1.9 with $\Gamma = (R_0^{SC} - Z_s)/(R_0^{SC} + Z_s)$, the reflection coefficient, which accounts for the reflected power due to the mismatch between the line and the device. As in our case $R_0^{SC} \gg Z_s$, the previous expressions can be approximated by $\Gamma \approx 4Z_s/R_0^{SC}$ and $\beta_{50\Omega} \approx 2Z_s\gamma$. Note that in this case $\beta_{50\Omega}$ depends only (proportionally) on γ, and thus it will follow then same trend, $1/W_{eff}$. Figure 2.18(a) shows β_{opt} and $\beta_{50\Omega}$ extracted with the QS model as compared with experimental measurements of $\beta_{50\Omega}$ at 1 GHz. β_{opt} exhibits a $1/W_{eff}^2$ trend as expec-

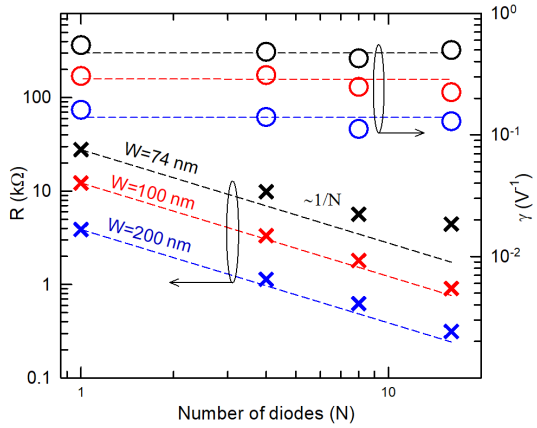

Figure 2.17: R_0 (left axis) and γ (right axis) *vs.* the number of channels in parallel for three channel widths, $W = 74$, 100 and 200 nm. $L = 1$ μm.

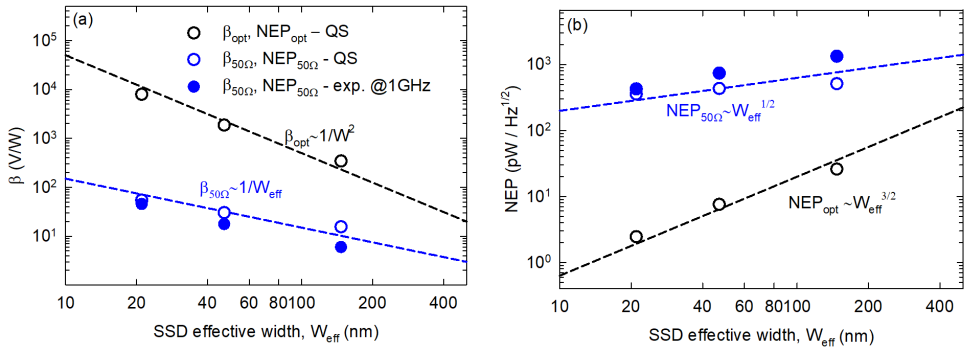

Figure 2.18: Log-log plots of (a) responsivity and (b) NEP *vs.* effective channel width extracted with the QS model from DC measurements (void symbols) and measured experimentally at 1 GHz (solid symbols) in SSDs with $N = 1$ and $L = 1$ μm. β_{opt} and $\beta_{50\Omega}$ were computed using Equations 1.8 and 1.9, respectively, and NEP using Equations 1.12 and 1.13. Dashed lines indicate the trends predicted by the model.

ted from the model, while for $\beta_{50\Omega}$ the dependence is as $1/W_{eff}$. A good agreement is found if we compare with the experimental results at 1 GHz ("low frequency"). A small discrepancy in the widest channel is observed. It could be associated with the uncertainties in the the extraction of the first and second derivatives of the I-V curve.

The other figure of merit of interest in this characterization is the Noise Equivalent Power or NEP (see subsection 1.1.1). Once again, assuming the SSD behaving as an ideal MOSFET, considering the previous trends for the key parameters and using β_{opt} in Equation 1.12, the calculated NEP, called NEP_{opt}, follows a trend $W_{eff}^{\frac{3}{2}}$. For $NEP_{50\Omega}$, calculated using $\beta_{50\Omega}$ in Equation 1.13, the dependence will be as $W_{eff}^{\frac{1}{2}}$. As in the case of the responsivity, these model predictions are supported by experimental results. NEP_{opt} and $NEP_{50\Omega}$ are shown in Figure 2.18(b), with the experimental values of $NEP_{50\Omega}$ obtained using $\beta_{50\Omega}$ at 1 GHz in Equation 1.13. As expected, a good agreement is found between the results of the QS model and the experimental values for $NEP_{50\Omega}$.

This good agreement confirms the validity of the QS model, which is useful not only to make predictions, but also to select from a group of SSDs with different geometries the ones with the best performance in order to perform a full RF characterization. The philosophy behind is that it is necessary just a very fast and easy DC current-voltage measurement to select the best candidate. RF measurements, which require of more complex setups, can be done afterwards only for the best devices.

2.3.4. Matching

From the previous results, design rules for performance optimization can be developed in terms of number of diodes in parallel, channel length and width. Placing N diodes in an array allows for the reduction of the resistance in a factor of $1/N$, with the advantage that γ remains constant with the number of channels, as demonstrated in Figure 2.17. Exploiting this fact, the optimal responsivity, defined by Equation 1.8, takes the value $\beta_{opt} = \frac{R_0\gamma}{2N}$ for an array of N diodes in parallel, each of them of resistance R_0. The $1/N$ trend comes from the fact that the resistance of the array is $R_0 = R_0^{SC}/N$. In the case of $\beta_{50\Omega}$, the dependence on N is not so simple, since the impact of the number of diodes in parallel depends on the ratio between the characteristic impedance of the line ($Z_s = 50\ \Omega$) and the actual resistance of the device R_0. Thus, we have three different regions depending on the value of N:

- In the first region, when $R_0 >> Z_s$, $\beta_{50\Omega}$ =2 γZ_s, independent of N.
- In the second region, where $R_0 \approx Z_s$, $\beta_{50\Omega}$ will follow the trend $1/N$.
- Finally, in the third region, where $R_0 << Z_s$, $\beta_{50\Omega}$ will decay as $1/N^2$.

Even for the case of $N = 16$, which is the maximum number of channels in parallel of Run 2, the resistance of the SSD ($R_0 \approx 10\,\text{k}\Omega$) is much higher than the characteristic impedance of the line. Therefore, we are always in the first region, with constant $\beta_{50\Omega}$. In order to observe the second region, we have studied the V-shape diodes, shown in Figure 2.3(c), where the resistance is expected to be lower because of their wider channel and the fact that arrays with a much higher number of channels in parallel, up to 64, were fabricated. The main drawback is the smaller bowing coefficient (wider channel means smaller non-linearity) and therefore low values for $\beta_{50\Omega}$ and β_{opt}. In Figure 2.19, we show, as a function of N, the experimental ($\beta_{50\Omega}$) and predicted responsivities ($\beta_{50\Omega}$ and β_{opt}) in (a) a T-shape narrow channel SSD, with $L = 1\ \mu$m and $W = 100$ nm, and in (b) a V-shape SSD, with $L = 1\ \mu$m, $W_{in} = 300$ nm and $W_{out} = 400$ nm. As expected, the predicted β_{opt} is inversely proportional to N, and the narrow T-Shape SSD has a higher β_{opt} than the V-shape SSD. On the other hand, the values of $\beta_{50\Omega}$ for the four available values of N in the the narrow T-Shape SSD lie in the first region, where $\beta_{50\Omega}$ is independent of N due to the extremely high mismatch. In contrast, for the case of the array of 64 V-shape SSDs, the value of $\beta_{50\Omega}$ already falls with N, according to the behavior in the second region, while for $N = 1$, 4 and 16 the values are still in the first region.

Another way to improve the impedance matching of SSDs is by connecting them to a high-impedance coplanar waveguide. For example, by reducing the signal line to 1 μm and increasing the ground plane spacing to 100 μm, the characteristic impedance of the CPW can be increased to $Z_s = 150\ \Omega$. In that case, an adequately tapered

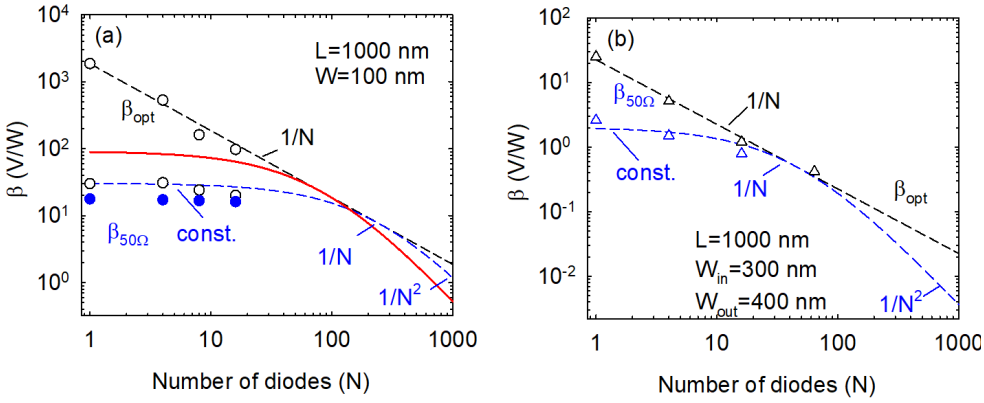

Figure 2.19: Log-log plot of responsivity *vs.* N extracted with the QS model (void symbols) and measured experimentally at 1 GHz (solid symbols) in (a) T-shape ($L = 1$ μm and $W = 100$ nm) and (b) V-shape ($L = 1$ μm, $W_{in} = 300$ nm and $W_{out} = 400$ nm) SSDs. The dotted lines indicate the trends of β_{opt} and $\beta_{50\Omega}$ following Equations 1.8 and 1.9 for $Z_s = 50$ Ω. The solid red line shows reponsivity calculated using $Z_s = 150$ Ω.

transition to the present 50 Ω accesses (with a 30 μm line and 20 μm spacing) has to be implemented in order to keep the reflection coefficient as low as possible. The values of $\beta_{50\Omega}$ calculated using $Z_s = 150$ Ω, plotted also in Figure 2.19, are much improved with respect to the case of $Z_s = 50$ Ω. Indeed, a 3× factor with respect to $\beta_{50\Omega}$ could be obtained. In that case the problem would be that the small size of the signal line would force the use of improved access designs to accommodate such number of devices, that needs around a 30 μm contour.

Regarding the NEP, the dependence on N has also three regions for the unmatched conditions and just one region for the matched conditions. In the matched results, according to Equation 1.12, the optimal NEP increases as $NEP_{opt} \propto \sqrt{N}$. Concerning the unmatched $NEP_{50\Omega}$, if we use the expression for $\beta_{50\Omega}$ in Equation 1.13 we have:

- A first region, when $R_0 >> Z_s$, where $NEP_{50\Omega}$ has a decay as $1/N^{1/2}$.
- A second region, when $R_0 \approx Z_s$, where $NEP_{50\Omega}$ increases as $N^{1/2}$.
- And a third regime, when $R_0 << Z_s$, where the increase is as as $N^{3/2}$.

The most interesting observation is that the minimum of $NEP_{50\Omega}$ is not reached when a perfect impedance matching is obtained ($R_0 = Z_s$), but when the condition $R_0 = 3Z_s$ is fulfilled. In this condition, corresponding to an optimum signal to noise ratio, the measured responsivity falls to 9/16 (56 %) of its maximum, $\beta_{50\Omega} = (9/8)\gamma Z_s$. For example, the SSD with $L = 1$ μm and $W = 100$ nm (with $R_0 = 12$ kΩ) would provide the best performance in a 50 Ω system by integrating approximately 80

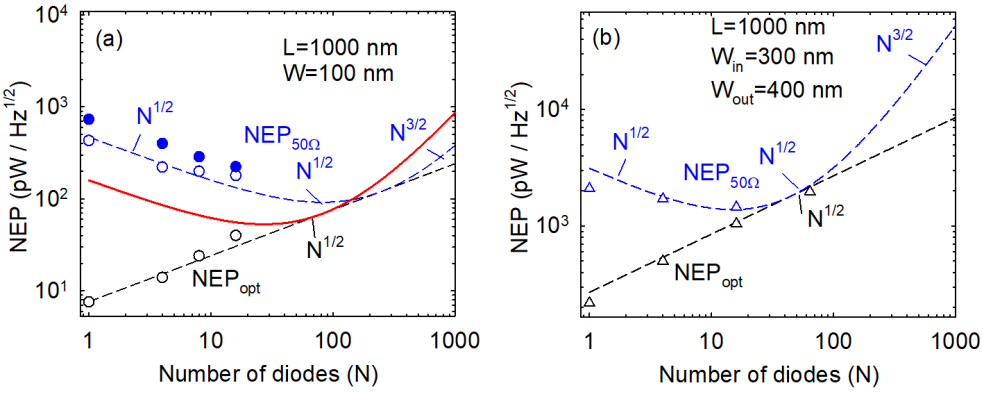

Figure 2.20: Log-log plot of NEP *vs.* N extracted with the QS model (void symbols) and measured at 1 GHz (solid symbols) in (a) T-shape (L = 1 μm and W = 100 nm) and (b) V-shape (L = 1 μm, W_{in} = 300 nm and W_{out} = 400 nm) SSDs. The dotted lines indicate the trends of NEP_{opt} and $NEP_{50\Omega}$ following Equations 1.12 and1.13 for Z_s = 50 Ω, while the red solid line shows the same analytical calculations using Z_s = 150 Ω.

channels in parallel. With this configuration, the results are $\beta_{50\Omega}$ = 17 V/W and NEP = 92 pW/Hz$^{1/2}$, as compared with 30 V/W and 425 pW/Hz$^{1/2}$, respectively, if N = 1. As we can see, these optimum matching conditions, attained by correctly choosing the value of N at the time of fabricating the devices, allow for an important decrease of the NEP (a 4.6 factor) with just a slight degradation of the responsivity (1.8 factor) with respect to a single-channel SSD. This behavior is analogous to that of transistors, in which the optimum bias for high gain does not coincide with that for low-noise operation. Finally, if devices are connected to a waveguide with Z_s = 150 Ω [also plotted in Figure 2.20(a)] the NEP would decrease by a factor of $\sqrt{3}\times$, reaching a value of 53 pW/Hz$^{1/2}$ (and $\beta_{50\Omega}$ = 50 V/W) with 3$\times$ less (around 27) number of parallel channels.

2.3.5. Influence of bias conditions

In previous sections we have focused on zero-bias RF detection by SSDs. It has the great advantage of no power consumption along with low noise. However, typically, a higher non-linearity is found when biasing the diode. In order to find the bias conditions where the non linear behaviour is maximum, the I-V curve has been measured in absence and presence of an RF signal of a given frequency. The direct comparison of both curves allows to very easily identify the best bias operation point. When an AC signal is injected into the device, the shape of the I-V curve changes, and, for example, at V=0 V the current is different to 0 A. The difference or shift in the

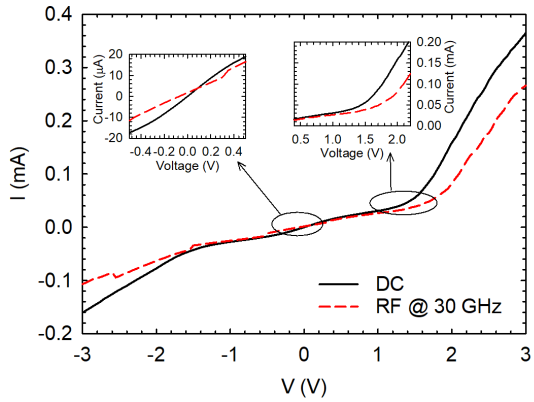

Figure 2.21: Current-voltage curves in absence and presence of a 0 dBm power RF signal at 30 GHz applied to an SSD (L = 1000 nm, W = 74 nm) of Run 1. Insets: zooms around 0 bias (left) and 1.3 V (right).

voltage (ΔV) between these two curves at a given current is the detected voltage, which straightforwardly gives $\beta_{50\Omega}$ for each bias. The bias where the detected voltage is maximum matches with the higher I-V non linearity, which is consistent with the equation $\beta_{opt} = 1/2\ R_0\gamma$, because γ is the highest at this point. Figure 2.21 presents the results for a diode of Run 1 (L = 1000 nm, W =74 nm) with no RF excitation and for a 0 dBm RF signal at 30 GHz. In the left inset a zoom around 0 V is shown, where the shift between measurements around 0 A is evidenced, resulting in a responsivity of 55 V/W. Instead, in the zoom around 1.3 V shown in the right inset, it can be observed that the maximum detection is reached for 45 μA, providing a responsivity around 230 V/W, about 4 times higher.

Once the increase in responsivity is understood, the experiment has been systematically repeated to cover the available frequency range of our VNA. Figure 2.22 shows the values of $\beta_{50\Omega}$ measured for RF excitations from 100 MHz to 43.5 GHz at 0 and 45 μA. The $\beta_{50\Omega}$ predicted by the QS model is also shown, exhibiting a good agreement.

The improved responsivity at 45 μA extends over the whole frequency range, with a small dependence on frequency. It is to be noted that this configuration has the drawback of power consumption and a significant increase of the noise with respect to a zero-bias detector. Since $1/f$ noise is excited, so that an adequate chopping of the input signal should be applied in order to decrease the NEP.

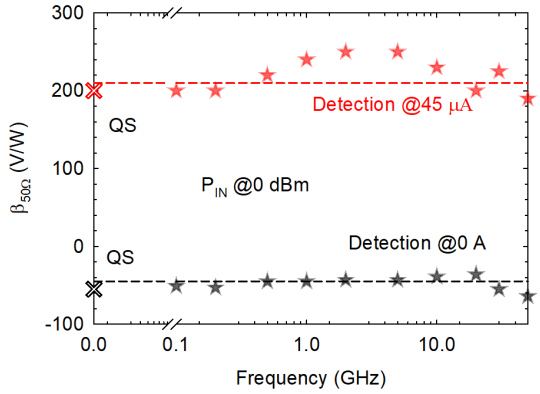

Figure 2.22: Impact of biasing the SSD on the value of $\beta_{50\Omega}$ as a function of frequency. The horizontal dashed line and the cross at zero frequency represent the QS value. Incident power of 0 dBm and 0 and 45 μA bias points.

2.3.6. Influence of temperature

In section 2.2, we have discussed the possible impact of self-heating effects to explain the differences between DC and pulsed measurements of the current-voltage characteristics depending on the device length. Unfortunately, in that moment we could not perform any real experiment to study the influence of T on the performance of SSDs. As mentioned in the introduction, at the end of my PhD our research group succeeded to acquire a new cryogenic probe station (LakeShore CRX-VF), presented in Chapter 1, which allows an operation temperature in the range between 10 K and 500 K. That is why in this subsection we present measurements to analyze the influence of temperature on the RF detection of SSDs fabricated on an AlGaN/GaN heterostructure grown on a Si substrate, which belong to Run 3. A device with one single channel of $L = 1$ μm and $W = 80$ nm has been analyzed.

As usual, first the I-V curve has been measured in a voltage range from -2 V to 2 V to subsequently apply the QS model. The results shown in Figure 2.23(a) reveal a surprising decrease of the current at low bias for the smaller values of T, while an increase was expected due to the higher mobility. This effect is most likely related to the presence of traps similar to those studied in section 2.2.

Following the QS model, it is straightforward to calculate the low-frequency responsivity according to Equation 1.9. Figure 2.23(b) shows how the value of R exhibits a monotonous increase when decreasing T, while the behavior of γ is more complex, first increasing abruptly, taking a maximum at $T \approx 200$ K, then changing sign at $T \approx 150$ K and showing a minimum at $T \approx 100$ K. The inset shows the dependence of

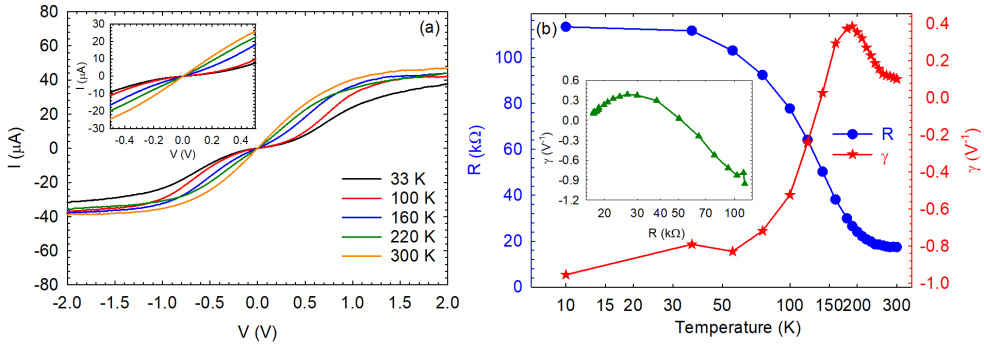

Figure 2.23: (a) *I-V* curves of a SSD with $L = 1$ μm and $W = 80$ nm measured at different temperatures. The inset shows a zoom around zero bias. (b) Resistance R and bowing coefficient γ obtained with the QS model as a function of temperature. The inset shows γ *vs.* R

γ with R. As mentioned, this behavior can be attributed to the presence of different kinds of traps [110].

To corroborate the predictions forecasted by the QS model, we have performed the RF characterization of the device in the frequency band between 100 MHz and 20 GHz with a -5 dBm input level. To this end we use the setup explained in subsection 1.1.2. The VNA operates as RF power generator, and, by means of a bias-tee, the SSD is biased with zero current and the output voltage ΔV is recorded. The results obtained for $\beta_{50\Omega}$ are shown in Figure 2.24, in (a) as a function of frequency for different temperatures and in (b) as a function of temperature for different frequencies and with the QS model. A fairly good agreement is found between the measured $\beta_{50\Omega}$ at low frequency (0.1 GHz) and the responsivity predicted by the QS model for each temperature. Moreover, by changing the input power, we have checked that the device behaves as square-law detector, as it can be observed in the inset. Similar results are obtained with multiple-channel SSDs and different channel widths and lengths. Interestingly, apart from the change of sign at about 140 K, for temperatures below 300 K and frequencies higher than about 1 GHz, the responsivity exhibits a drop-off. We attribute these effects to the presence of traps.

Currently, we are trying to identify the origin of these traps, which most likely correspond both to surface states located at the walls of the trenches, originated by the etching process, and defects of the bulk. The activation energy of the first ones is around 10-15 meV, corresponding to an equivalent temperature $T \approx 150$ K, around which the responsivity changes of sign [110]. The one attributed to the bulk appears around 60 meV and it has been observed in other works [111, 112, 113].

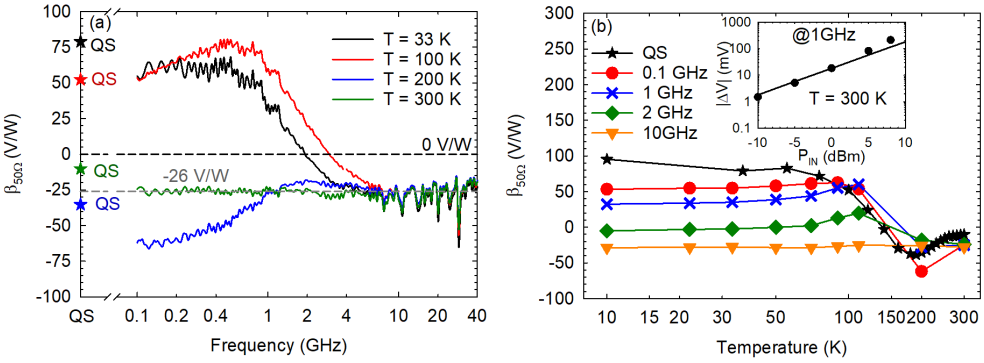

Figure 2.24: (a) $\beta_{50\Omega}$ as a function of the RF frequency measured at different temperatures. The stars represent the $\beta_{50\Omega}$ extracted with the QS model. (b) QS value compared with $\beta_{50\Omega}$ measured at 0.1, 1 and 10 GHz as a function of temperature. Inset: detected voltage as a function of the input power, the line confirms the square-law detection.

2.4. Gated Self-Switching Diodes

According to the previous results, the SSDs with the narrower channels provide the higher values of $\beta_{50\Omega}$. In these diodes, the depletion due to the charges trapped at the walls of the trenches has a very significant impact on the channel conductance. It can be concluded that the smaller the number of carriers contributing to the current, the better the detection capabilities [114]. However, the fabrication of those narrow channels is a very difficult task, which, in addition, has a main drawback: the variability in the widths of the channels. Then, the control of carrier concentration in the channel (n_s) is not evident just with the reduction of the widths. In order to control n_s in wider channels, which are easier to fabricate, the inclusion of a top gate on the channel was proposed. The impact of the top gate on the channel concentration is similar to the effect of reducing the channel width, the decreasing of n_s in the 2DEG, which improves the detection in the device [114]. We will call these devices Gated Self-Switching Diodes or G-SSDs.

2.4.1. G-SSDs with antennas (Run 2)

The G-SSDs were fabricated in the wafer of Run 2 at the IEMN. In particular, bow-tie antennas were fabricated for free-space measurements. Figure 2.25 shows a SEM image of an array of diodes ($N = 4$) with the gate fabricated on the center of the channel. The dimensions of the channels are $L = 1$ μm and $W = 100$ nm. In addition, some of the fabricated G-SSDs have the gate on the entrance of the channels. The characterized G-SSDs are based in an AlGaN/GaN heterojunction on a Si substrate grown by

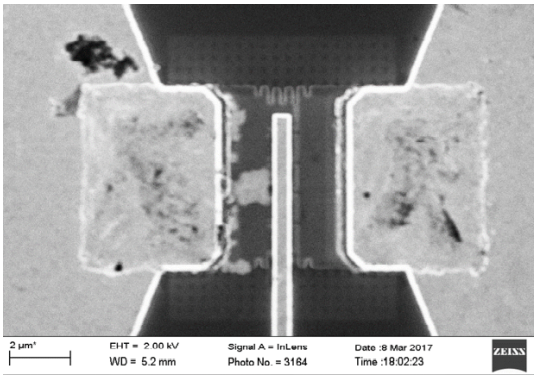

Figure 2.25: SEM image of the G-SSD with the top gate fabricated in the center of the channel. The dimensions of the channels are $L = 1$ μm and $W = 100$ nm. $N = 4$.

EpiGaN, consisting of a 25 nm thick AlGaN barrier (with 35 % Al content) on top of a 1.5 μm thick GaN buffer. The fabrication process, based on recess technology, is similar to the one presented in [109], in which, after the dry etching of the trenches, a final step associated with the top gate fabrication is added. The device under test has 4 channels in parallel, approximately 100 nm wide and 1.0 μm long. The 500 nm gate electrode is located at the center of the channel and will operate as a Schottky contact.

First, using the semiconductor analyzer (Keithley 4200-SCS), G-SSDs have been characterized in the DC regime at room temperature. Figure 2.26(a) shows the output curves of the devices, demonstrating a good transistor operation, in spite of the appearance of a non-negligible gate leakage current, most probably associated with electrons injected from the gate through the lateral walls of the trenches. On the transfer characteristics (I_D *vs.* gate-to-source voltage, V_{GS}), shown in Figure 2.26(b), it is observed that the threshold voltage V_{TH} is more negative as V_{DS} increases. This corresponds to a well-known short-channel effect, drain-induced barrier lowering [115]. Since the G-SSDs have not been designed for transistor operation, poor transconductance values are achieved, Figure 2.26(b). They have been designed to operate as zero-bias detectors, so their bias point is not in saturation as usual in transistors, but with V_{DS} around zero. Therefore, as a reference for calculating the gate voltage overdrive, we have used the threshold voltage, V_{TH} =-1.6 V, determined from the lowest values of V_{DS} in the transfer characteristics.

For the sake of comparison, in the inset of Figure 2.26(a), the current measured in a G-SSD with a floating gate (open gate operation) and that of a usual SSD (without gate electrode), with a similar channel geometry (width of 74 nm), are compared to that of the G-SSD with $V_{GS} = 0.0$ V. In view of the comparison, it is clear that just the

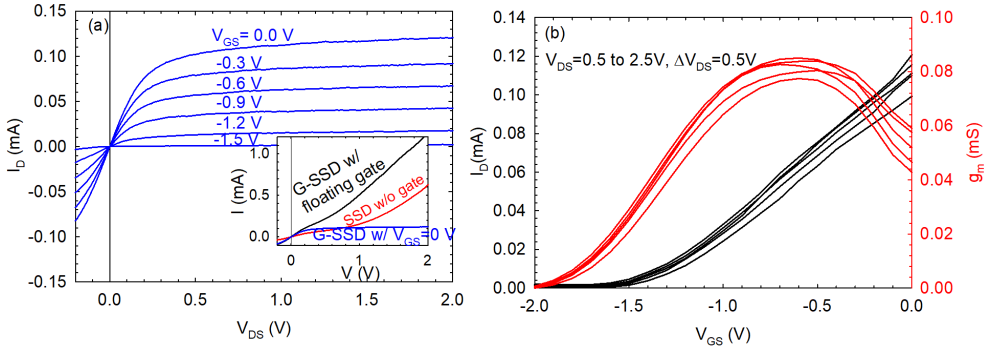

Figure 2.26: (a) Output characteristics and (b) transfer characteristics (left axis) and transconductance g_m (right axis) of the G-SSD under test. The inset shows the *I-V* curves of the G-SSD in open gate operation (floating gate) and a SSD without gate with a similar geometry (74 nm width and 1.0 μm length).

inclusion of the gate has a significant impact, reducing the depletion region imposed by the surface charges at the sidewalls of the channel, thus opening the channel and increasing the current.

From these DC measurements, it is possible to predict the responsivity and NEP, following as the method described in subsection 1.1.1. By means of a polynomial fitting of order three [using 20 points within the (+0.1 V, -0.1 V) range], the values of the resistance R and the bowing coefficient γ are calculated, thus allowing to determine the optimum responsivity $\beta_{opt} = \frac{1}{2}R\gamma$. Note that γ is a normalized parameter (given in units of V^{-1}) allowing to compare different types of device architectures and whose value does not depend on the device size, i.e., the area of SBDs, the gate width of FETs, or the number of parallel channels of SSDs or G-SSDs.

As expected, R and γ, shown in Figure 2.27(a) as a function of $V_{GS} - V_{TH}$, increase monotonically when decreasing V_{GS}, taking values in the range of 2.0 - 200 kΩ and 0.2 - 10 V^{-1}, respectively. However, we can identify two regions depending on the gate bias. For $V_{GS} - V_{TH}$ above 0.5 - 0.6 V, the G-SSD behaves as a standard FET, and R increases when decreasing V_{GS}, following the ideal $R \sim (V_{GS} - V_{TH})^{-1}$ dependence. But when the G-SSDs approach pinch-off conditions ($V_{GS} - V_{TH} < 0.5$ V), R increases faster than expected, as $(V_{GS} - V_{TH})^{-2}$. This indicates that the current control mechanism in the G-SSDs is modified from the pure field-effect gating appearing at higher V_{GS} to a more complex behavior when V_{GS} comes close to V_{TH}. Under those conditions, the depletion imposed by the surface charges at the drain side of the channel may become more important due to a stronger electron heating (due to

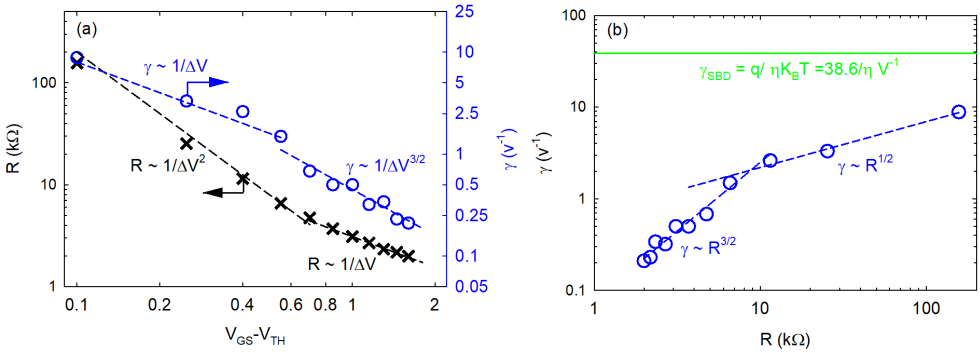

Figure 2.27: (a) R and γ extracted from the DC measurements of the $I_D - V_{DS}$ curves as a function of V_{GS} - V_{TH} at $I_D = 0$ A. Dashed lines show different dependencies on (V_{GS} - V_{TH}) for eye guiding. (b) γ *vs.* R, with the eye guiding lines showing the $\gamma \sim R^{3/2}$ and $\gamma \sim R^{1/2}$ dependencies, appearing at high and low V_{GS}, respectively. The green line corresponds to the value of γ in a SBD with $\eta = 1$.

the strong electric field caused by the large gate-drain voltage difference, V_{DG}) and thus further increasing R.

Those two regions of gate bias can also be observed in the values of γ. In open channel conditions, $(V_{GS} - V_{TH}) > 0.5\ V$, when R is below 10 kΩ, γ goes as $R^{3/2}$, as shown in Figure 2.27(b), so that $\gamma \sim (V_{GS} - V_{TH})^{-3/2}$. However, this dependence cannot be inferred from the ideal FET theory, since it predicts a null value (as expected from a linear dependence of I_D on V_{DS}), and it is the asymmetry of the channel (the SSD geometry) which produces this nonlinearity. In the low V_{GS} region, in spite of the steeper increase in R, γ increases more slowly with decreasing gate bias as a result of a weaker dependence on R [$\gamma \sim R^{1/2}$, in Figure 2.27(b)] so that γ goes as $(V_{GS} - V_{TH})^{-1}$. As it can be extrapolated from these γ *vs.* R dependencies, the value of $\left(\frac{d^2I}{dV^2}\right)$ increases with R for low R (when $\gamma \sim R^{3/2}$) and then decreases (when $\gamma \sim R^{1/2}$), peaking at about $(V_{GS} - V_{TH}) \approx 0.5\ V$. Even if the change of the slope in the V_{GS} dependencies of R and γ is not extremely obvious, the separation between the open-channel and near-pinch-off regions is quite evident in the γ *vs.* R representation of Figure 2.27(b) a clear switch from a rapid increase in γ as $R^{3/2}$ for low V_{GS} to a slower increase as $R^{1/2}$ for the higher V_{GS} values appears at $R \sim 10\ k\Omega$ (corresponding to $(V_{GS} - V_{TH})$ = 0.5 - 0.6 V). Figure 2.27(b) also shows the value of γ for devices with an exponential I-V curve, like SBDs, typically used as detectors. $\gamma = q/\eta k_B T$, with η being the non-ideality factor, which for $T = 300$ K and $\eta = 1$ leads to $\gamma = 38.6\ \mathrm{V}^{-1}$ (an invariant value regardless of the resistance of the SBD). This value of γ, which could be considered as the target for the G-SSDs (their non-

linearity would be comparable to that of an exponential I-V), is approached when lowering V_{GS}, providing values not far from 10 V^{-1}.

In order to demonstrate their potentiality as sub-THz detectors, the devices were integrated with broadband bow-tie antennas, as shown in the SEM image in the inset of Figure 2.28 (see also Figure 2.5). The solid-state frequency multiplied source on the setup of Figure 1.7, with an output power of $\sim$ 6 mW at 300 GHz was used to excite the G-SSD. The induced V_{DS} was measured at room temperature using a lock-in technique with a mechanical chopper between 0.233 and 1.29 kHz [116]. This setup is explained in detail in subsection 1.1.2. In this kind of configuration, optical losses (focusing, wave propagation, normalization due to beam spot and device size) are very difficult to estimate, so that in Figure 2.28 just the output voltage measured at the drain, $\Delta V_{DS} = V_{DS}^{ON} - V_{DS}^{OFF}$, is presented. The figure shows that the photoresponse increases sharply when V_{GS} approaches the threshold voltage and then saturates within the sub-threshold region, probably due to leakage current through the gate. This behavior has also been found in GaN-FETs [13].

With the aim of having a better quantitative estimation of the responsivity of the devices, we have also characterized the G-SSD as a RF detector under probes, again at room temperature. In this case, the average ΔV_{DS} was measured while simultaneously biasing the device with $I_D = 0$ (through a bias tee) and the corresponding V_{GS}. Since coplanar waveguide accesses were not available for the G-SSD, the RF measurements were performed using DC needles at relatively low frequency, 900 MHz (setup also explained in subsection 1.1.2). In order to calibrate the electrical losses associated with this setup, a power compensation is required. For that purpose, a previous measurement comparing both RF probes and DC needles was done on SSDs without gate (with integrated RF accesses), providing a value of input losses IL = 10 dB. There-

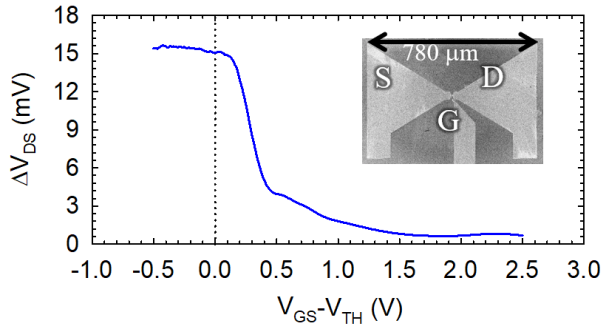

Figure 2.28: Output voltage when illuminating the sample with a 300 GHz beam as a function of V_{GS} - V_{TH} at $I_D = 0$ A. The inset shows the geometry of the bow-tie integrated antenna.

fore, the voltage responsivity of the G-SSD is calculated with Equation 1.14, which is constant in the whole range of the available input power, meaning that the device behaves as a square-law detector. On the other hand, the noise equivalent power is obtained as $NEP_{50\Omega} = (4k_BTR)^{1/2}/\beta_{50\Omega}$, using the ideal value of the noise power of the G-SSD given by the Nyquist theorem. In the case of the free-space measurements, $\beta_{50\Omega}$ and $NEP_{50\Omega}$ are calculated in the same way but the coupling and mismatch losses have been estimated by fitting the free-space results to the RF measurements at $\Delta V_{DS} = 0.1$ V, thus giving an approximate value of 27 dB losses.

Figure 2.29 compares the values of $\beta_{50\Omega}$ and $NEP_{50\Omega}$ as a function of ΔV_{DS} measured in free space (at 300 GHz) and under probes (at 900 MHz), with the calculations using the QS model. DC, RF, and free-space results show a reasonable agreement, the slight disagreement probably due not only to the power losses but also to the difficult extraction of the values of γ from very small values of current in the case of the QS model and the frequency dependence of the impedance of the devices, which could affect the value of the mismatch factor for the different frequency ranges. The increase in $\beta_{50\Omega}$ when lowering the gate bias shows the same trends as those of γ [Figures 2.27 and 2.29(a)], $\beta_{50\Omega} \sim (V_{GS} - V_{TH})^{-3/2}$, and $\beta_{50\Omega} \sim (V_{GS} - V_{TH})^{-1}$ in the $(V_{GS} - V_{TH})$ regions above and below 0.5 - 0.6 V, respectively. This happens because when R is very high, as occurs in the G-SSD, the value of the responsivity approaches $\beta_{50\Omega} \approx 2\gamma Z_s = 100\ \gamma$. Therefore, β is just proportional to γ, i.e., depends only on the non-linearity of the $I_D - V_{DS}$ curves. Figure 2.29(a) also shows the values of $\beta_{50\Omega}$ obtained in un-gated SSDs. Interestingly, the value of the responsivity of the G-SSD overcomes that of ungated SSDs when entering the near pinch-off gate bias region [$(V_{GS} - V_{TH}) < 0.5$ V]. This is also an evidence that, under those conditions, an additional current control mechanism is in action. Remarkably, this leads to values of responsivity as high as 600 V/W, never obtained previously in ungated SSDs, even with the optimum geometry (the highest responsivity, 100 V/W, was obtained with an extremely narrow channel defined by ion implantation [12]).

Regarding the NEP [see Figure 2.29(b)], in open channel conditions, it decreases when lowering V_{GS} as $(V_{GS} - V_{TH})$. This behavior follows from the $(V_{GS} - V_{TH})^{-3/2}$ and $(V_{GS} - V_{TH})^{-1}$ dependencies of β and R, respectively. For $(V_{GS} - V_{TH}) < 0.5$ V, a nearly constant value is reached, since the $(V_{GS} - V_{TH})^{-1}$ and $(V_{GS} - V_{TH})^{-2}$ trends of $\beta_{50\Omega}$ and R, respectively, cancel each other. As a consequence, the value of $NEP_{50\Omega}$ decreases below 50 pW/Hz$^{1/2}$.

Overall, the agreement achieved among the estimations of $\beta_{50\Omega}$ and $NEP_{50\Omega}$ obtained by the different approaches is remarkable, and indicates that the the G-SSDs exhibits a competitive performance as RF detector from low frequency up to at least 300 GHz.

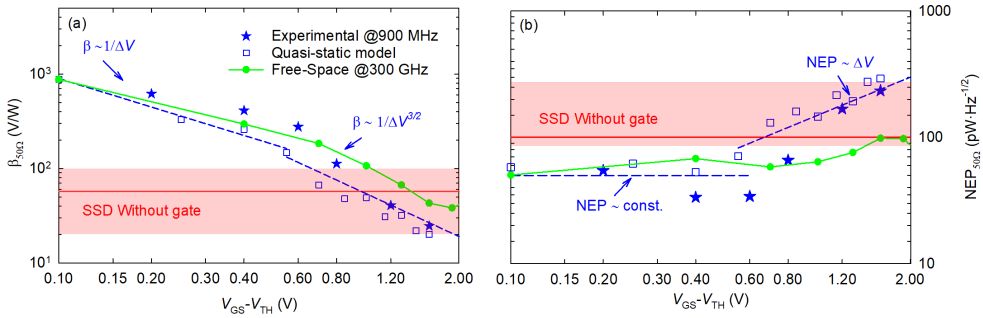

Figure 2.29: Comparison of the values of (a) $\beta_{50\Omega}$ and (b) $NEP_{50\Omega}$ *vs.* $V_{GS} - V_{TH}$ (at I_D = 0.0 A) calculated from the DC measurements (QS model) with those obtained in the experimental free-space setup at 300 GHz and the RF measurements at 900 MHz. The values for the SSD without gate and the same geometry are shown by the horizontal solid line, while the results of GaN based SSDs with other geometries (fabricated in the same run and published in the literature [12, 109]) are indicated by the shaded regions.

2.4.2. Number of diodes, width and length (Run 3)

A new set of devices was fabricated in Run 3 with the appropriate accesses for RF probes (see Figure 2.5). Two substrates, Si and SiC, with different thermal conductivities have been used. Three different layouts were designed, two of them with SiC substrate and the other one with Si substrate. In the G-SSD of Run 3, the gates were isolated to avoid the leakage found in Run 2. In particular, a thin layer of SiN was deposited on the top of the AlGaN before the gate fabrication step in order to correctly isolate the gate contact. In Figure 2.30(a), the output characteristics of a G-SSD of this Run 3 are shown; in particular, a device of the wafer of AlGaN/GaN on SiC substrate, with L = 1000 nm, W = 100 nm and N = 16 channels in parallel). A typical FET behavior is observed in these devices. In Figure 2.30(b), left axis, the transfer characteristics are shown. Using the same criterion previously explained in subsection 2.4.1, a value of V_{TH} =-5.5 V is extracted. The transconductance g_m is shown in the right axis. Again, the levels of g_m are quite low due to the low levels of current caused by the small width of the channels. A small width improves the non-linearity, limiting the current, but also reduces the capacitance induced by a higher width in a usual FET, what is positive for high-frequency applications. The width of the channel in the G-SSD is the equivalent parameter to the width in a usual FET. Therefore, these devices are optimized to improve RF detection (responsivity and maximum operation frequency), but is not optimum for amplification.

The QS model is used to study the geometrical dependencies in the performance of these devices. Figure 2.31(a) shows $\beta_{50\Omega}$ extracted from the *I-V* curves of the

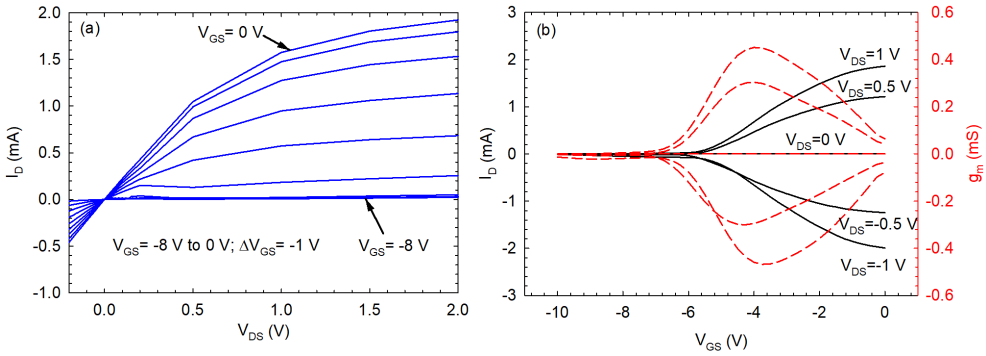

Figure 2.30: (a) Output characteristics, and (b) transfer characteristics (left-axis) and g_m (right axis) of a G-SSD with $L = 1000$ nm, $W = 100$ nm and $N = 16$.

G-SSDs ($L = 1000$ nm and $W = 100$ nm) with $N = 1$, 8 and 16 channels in parallel. Similar results are obtained for the three values of N. On the other hand, $NEP_{50\Omega}$, shown in Figure 2.31(b), as expected decreases with the increase of N. This decrease of $NEP_{50\Omega}$ can be understood by means of Equation 1.13. This behavior is similar to that of the results found for SSDs without gate in subsection 2.3.4, where it was explained. The argument was based on the fact that γ remains constant with N, but R decreases. For the widths studied, between 100 nm and 200 nm, $\beta_{50\Omega}$ is in the first region described in subsection 2.3.4, $R >> 50\ \Omega$, where the responsivity is just proportional to the bowing coefficient, which remains constant with N, thus leading to a nearly constant $\beta_{50\Omega}$.

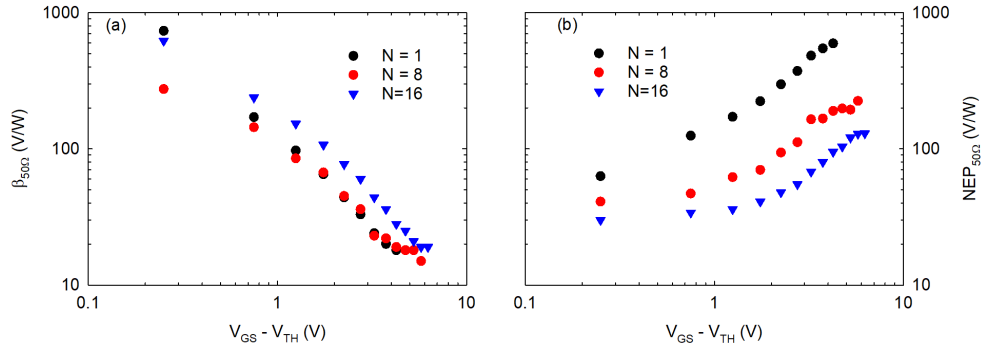

Figure 2.31: (a) $\beta_{50\Omega}$ and (b) $NEP_{50\Omega}$ extracted from the QS model as a function of V_{GS} - V_{TH} at $I_D = 0$ A in G-SSDs with RF accesses, with $L = 1000$ nm, $W = 100$ nm and different number of channels in parallel.

The length does not seem to be a critical element to be optimized. In contrast, the width is a key factor for the optimization, due to its close link with the bowing coefficient. R extracted from the QS model *vs.* $V_{GS}-V_{TH}$ is plotted in left axis of Figure 2.32(a). For an array of 16 G-SSDs in parallel, the narrower channel (100 nm and V_{TH} =-6.9 V) shows a higher R than the wider channel (200 nm and V_{TH} =-7.1 V). Concerning the bowing coefficient, rigth axis of Figure 2.32(a), the extracted γ is higher for W = 100 nm as compared with W = 200 nm. Therefore, according to Equation 1.8, smaller W will provide better responsivities.

In Figure 2.32(b), γ is plotted *vs.* R for all measured biasings. Both widths show a behavior quite similar to the one previously analyzed in subsection 2.4.1 for SSDs without gate. As novelty, it is remarkable the change in the trend of γ in the region close threshold: the wider G-SSD has a smaller slope ($\gamma \sim R^{3/4}$) than the narrower one ($\gamma \sim R$). γ in a SBD is around $38/\eta$ V^{-1}, while the G-SSDs of Run 3 have a maximum value of 6.24 V^{-1}, with room for optimization.

Finally, Figure 2.33(a) shows the values obtained for $\beta_{50\Omega}$ by means of the QS model. As mentioned before, W = 100 nm leads to higher $\beta_{50\Omega}$ because of the dependence of R and γ on the widths. In Figure 2.33(b), $NEP_{50\Omega}$ is plotted. The narrower G-SSD provides smaller values of $NEP_{50\Omega}$ due to the proportional relationship between $NEP_{50\Omega}$ and $R^{1/2}$ and inversely between $NEP_{50\Omega}$ and $\beta_{50\Omega}$. Interestingly, when V_{GS} is close to V_{TH}, $NEP_{50\Omega}$ becomes practically constant.

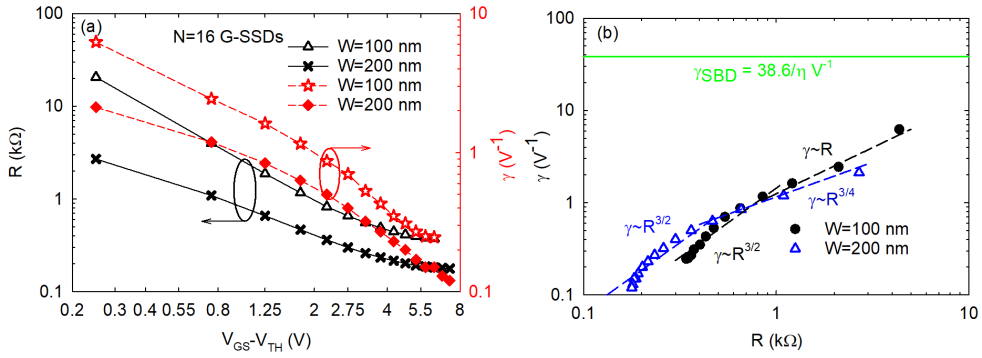

Figure 2.32: (a) R (left axis) and γ (rigth axis) extracted from the QS model at I_D = 0 A, and (b) γ *vs.* R for G-SSDs with RF accesses, with L = 1000 nm, N = 16 and two different widths, W = 100 nm and W = 200 nm. The green line corresponds to the value of γ in a SBD with η = 1.

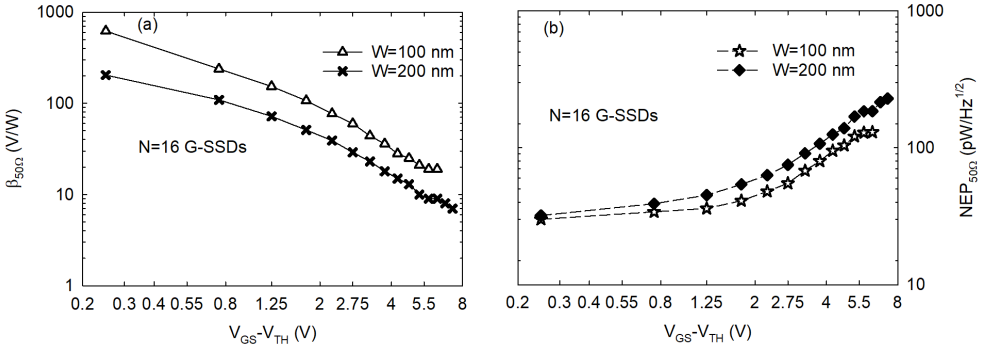

Figure 2.33: (a) $\beta_{50\Omega}$ and (b) $NEP_{50\Omega}$ *vs.* V_{GS} - V_{TH} at $I_D = 0$ A, extracted from the QS model for G-SSDs with RF accesses, with $L = 1000$ nm, $N = 16$ and two different widths, $W = 100$ nm and $W = 200$ nm.

RF measurements

In order to validate the results obtained with the QS model in the G-SSDs of Run 3, we have measured the responsivity of two G-SSDs with $L = 1$ μm, $N = 16$ and widths $W = 100$ nm and $W = 200$ nm. Figure 2.34 shows the comparative of the results of $\beta_{50\Omega}$ extracted with the QS model and the experimental results at 1 GHz with an input power of 0 dBm at the entrance of the G-SSD (after compensating losses). As expected, a higher reponsivity is measured in the narrower G-SSD. Specifically, for $W = 100$ nm, a maximum responsivity of 650 V/W is predicted by QS model and 200 V/W is measured at V_{GS} =-6.65 V.

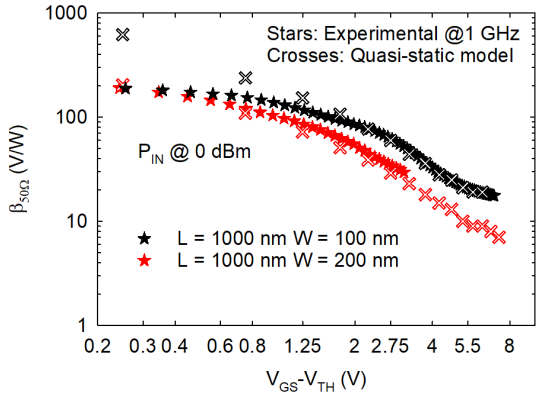

Figure 2.34: $\beta_{50\Omega}$ *vs.* $V_{GS} - V_{TH}$ at $I_D = 0$ A extracted from the QS model (crosses) and RF measurements (stars) for G-SSDs with RF accesses, with $L = 1$ μm, $N = 16$ and two different widths, $W = 100$ nm and $W = 200$ nm. $P_{IN} = 0$ dBm.

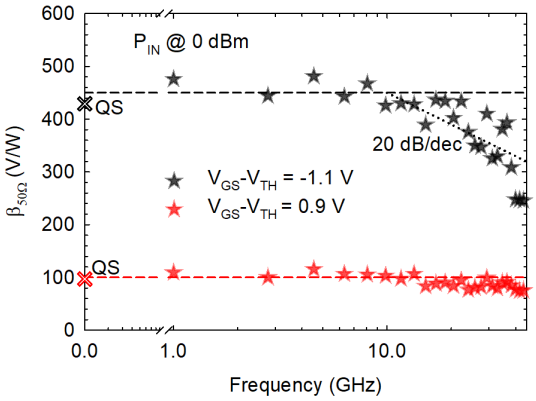

Figure 2.35: $\beta_{50\Omega}$ *vs.* frequency measured at $I_D = 0$ A in a G-SSD with $W = 200$ nm, $L = 1$ μm and $N = 16$, at V_{GS} - $V_{TH} = 0.9$ V and V_{GS} - V_{TH} =-1.1 V. $P_{IN} = 0$ dBm. The horizontal dashed line and the cross at zero frequency represent the QS value.

Notice that the results at the V_{GS} values in which the channel is open show a good agreement between the QS model and the measurements. However, for V_{GS} approaching the threshold voltage, a disagreement is evidenced, more pronounced in the narrower device. These discrepancies for V_{GS} close to pinch-off conditions suggest that the QS model may be not accurate enough in this range because of the difficulty in estimating the (very large) resistance of the channel by means of the derivative of very low values of current obtained with not enough precision.

In Figure 2.35, we plot $\beta_{50\Omega}$ *vs.* frequency measured at two bias conditions chosen in relation with the threshold voltage (V_{GS} =-6 V and V_{GS} =-8 V corresponding to V_{GS} - $V_{TH} = 0.9$ V and V_{GS} - V_{TH} =-1.1 V, respectively) in the G-SSD with $W = 200$ nm. At V_{GS} - $V_{TH} = 0.9$ V, the measured $\beta_{50\Omega}$, around 100 V/W, is practically constant with frequency and coincides with the value predicted by the QS model. At V_{GS} - V_{TH} =-1.1 V, $\beta_{50\Omega}$ is higher, around 450 V/W, as expected from a bias condition closer to pinch-off. However, a roll-off at frequencies higher than 20 GHz is observed. Again a good agreement with the QS model can be observed at low frequencies.

Influence of temperature

In subsection 2.3.6, we have studied the influence of temperature on the performance of SSDs. Since, as already mentioned, a cryogenic probe station (LakeShore CRV-X) was acquired by the laboratory at the end of my experimental activities, here we provide very preliminary results of the characterization of G-SSDs in temperature, just in DC conditions. In particular, we have characterized a G-SSD of Run 3 on a

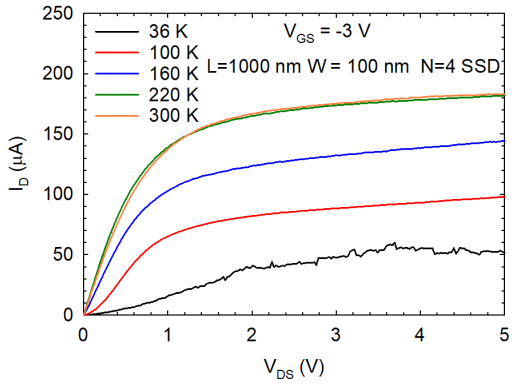

Figure 2.36: Output characteristics measured in a G-SSD with $W = 100$ nm, $L = 1$ μm and $N = 4$ at five temperatures, for V_{GS} =-3 V.

substrate of Si with $W = 100$ nm, $L = 1$ μm and $N = 4$. Figure 2.36 shows the output characteristics at V_{GS} =-3 V measured at different temperatures from 36 to 300 K. As in the case of the SSDs without gate (see Figure 2.23), an increase of the current with temperature takes place for $T < 220$ K and a change of sign in the zero-bias γ occurs around 150 K. These effects are again attributed to presence of traps at the sidewalls of the channel, which release the captured electrons as the temperature is increased.

To conclude we would like to remark that the results presented in this last subsection 2.4.2 (and the ones corresponding to 2.3.6) are preliminary. On-going measurements will allow us to investigate the behavior of $\beta_{50\Omega}$ when pushing our G-SSD more in the sub-threshold region in order to carry out a comparison with the measurements of the detection performance of the HEMTs, also depending on the temperature (last chapter of this thesis, section 4.2). Our two main objectives are: (i) analyze the physical mechanism of detection, in particular the dependence of $\beta_{50\Omega}$ on the temperature for voltages $V_{GS} - V_{TH} < 0$ (see Figure 2.28) and (ii) quantify the frequency corner of the RF detection (see Figure 2.35) as a function of V_{GS} in several scenarios.

Chapter 3

High-Electron-Mobility Transistor: DC behavior

The high-electron-mobility transistor (HEMT) has significantly contributed to the progress in the field of high-speed electronics. These devices demonstrate good performance with high gain and low noise at very high frequencies. In digital electronics, it has also reduced propagation delays and access times in SRAM memories. The concept of accumulation of charge at a heterojunction interface was introduced in the late 1960s and the develepoment of fabrication techniques like epitaxial-growth made a reality the fabrication of high-quality heterostructures in III-V compounds [117]. The initial activity on this type of devices was done with AlGaAs/GaAs n-channel heterostructures, the first transistor fabricated in 1978 [118]. Subsequently, other material systems have been used in the fabrication of HEMTs with advanced topologies, which have largely improve their high-frequency performance. These HEMTs are based on materials like InAlAs/InGaAs [119], AlSb/InAs [120] or AlGaN/GaN [121]. In the last decades, GaN-based HEMTs have emerged as robust devices with applications in different fields such as power amplifiers, radar systems or energy conversion, which require high output power and high efficiency [122]. This chapter will be devoted to the analysis of GaN HEMTs operating under DC conditions.

In section 3.1, we will study the basics of HEMTs, more specifically of GaN-based HEMTs, and the physics behind this kind of heterojunction devices. In section 3.2, we describe the wafer samples available for this study, fabricated at IEMN, including the details about the semiconductor layers and dimensions. In each reticle on the wafers there are several specific elements very useful to characterize the quality of the material system used in the fabrication of the devices. In section 3.3, we show the DC

results obtained at 300 K and describe the protocol to fit the experimental results with the Monte Carlo (MC) simulations. *I-V* curves evidence the importance of the effects caused by heating. GaN is a material with a wide bandgap and good thermal conductivity, thus suitable for high-power applications, where issues related with self-heating arise [123]. We have studied the impact of heating on the DC behavior of the transistor by means of the MC tool in subsection 3.4.1. Two approaches have been used, the thermal resistance model (TRM) and the electrothermal model (ETM), explained in subsection 1.2.2. Finally, the behavior of the transistor at temperatures higher than 300 K will be analyzed in subsection 3.4.2.

3.1. GaN HEMTs

HEMTs are field effect transistors (FETs) fabricated on a heterojunction formed of two materials with different gap. When two semiconductor materials with different gap are grown together in a heterojunction, discontinuities in the conduction band (E_C) edges are present at the heterointerface, what creates a quantum well in the material with narrower *gap*. In the majority of HEMTs, the wide-bandgap material is *n*-doped with donor impurities [for example the AlGaAs in an AlGaAs/GaAs heterojunction like the one shown in Figure 3.1(a)]. Electrons accumulate in the well and form a sheet of charge. The thickness of this channel is about 100 $\mathring{A}$, of the order of the de Broglie wavelength the electrons. Thus, the electrons are quantized in a two-dimensional system at the heterointerface, forming the 2DEG [124]. In this way, electrons are physically separated from the impurities, reducing the scattering and increasing the mobility [117]. An improvement added to these type of HEMTs is the use of a thin layer of donors, usually called δ-doping, like in the case of the InAlAs/InGaAs heterostructure shown in Figure 3.1(b). The InAlAs layer is still present, but the doping is positioned in a monolayer (of width comparable with the lattice constant) far from the 2DEG in order to reduce the influence of the dopants on the carriers and improve the control of the gate [125].

The heterojuntion of our HEMTs is AlGaN/GaN. GaN is a III-V nitride material with a wurzite crystalline structure [128]. The most important symmetries in the crystalline structure are in the nitrogen (N). However, GaN has not inversion symmetry along the [0001] axis, which leads to a large macroscopic polarization along that axis. This is a spontaneous polarization ($\vec{P}_s$) caused by the lack of symmetry in that direction. ($\vec{P}_s$) is also present in the AlGaN layer, like it has been represented in Figure 3.2. Additionally, a piezoelectric coupling ($\vec{P}_z$) appears in the the AlGaN layer due to a tensile strain. All these effects lead to the presence of a net surface charge at the interfaces between materials, with an associated discontinuity in the electric field.

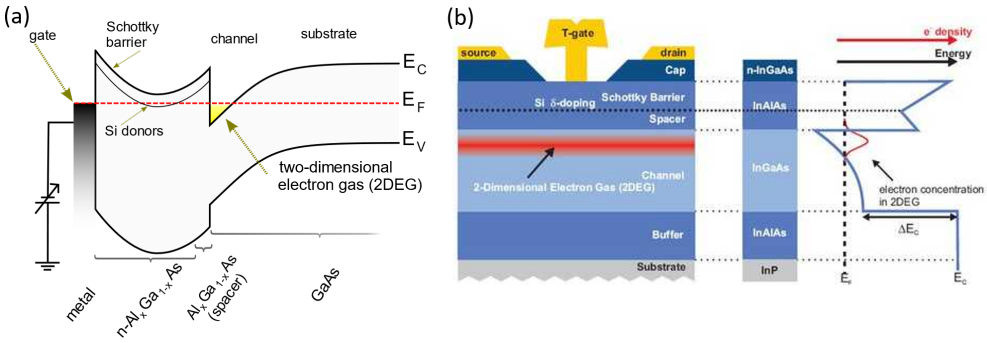

Figure 3.1: Heterostructure and band structure of (a) an AlGaAs/GaAs HEMT, which includes an n-doped AlGaAs barrier [126], and (b) an InAlAs/InGaAs HEMT, which includes a very narrow δ-doping layer [127].

These surface charges, by attracting electrons, are at the origin of their accumulation in the 2DEG channel of AlGaN/GaN HEMTs, where the layers are not intentionally doped.

In Figure 3.3(a), we show the geometry of a typical AlGaN/GaN HEMT and the position of the 2DEG channel in the heterostructure. AlGaN/GaN HEMTs do not have any intentionally doped layer, since the carriers of the 2DEG come from the presence of polarization, piezoelectric and top-surface charges, whose balance requires the existence of negative charge in the well [1]. Figure 3.3(b) shows the band structure of the AlGaN/GaN heterojunction, with the position of the potential well. As novelty with respect to this standard layer structure, our devices have a spacer

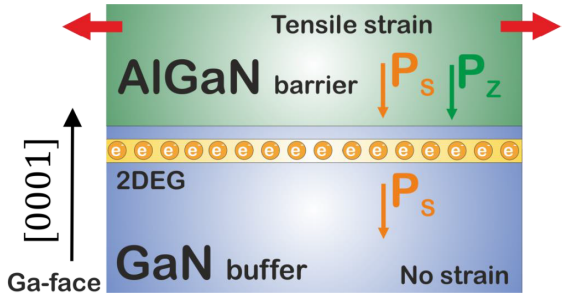

Figure 3.2: Spontaneous and piezelectric polarizations in the AlGaN/GaN heterostructure [129].

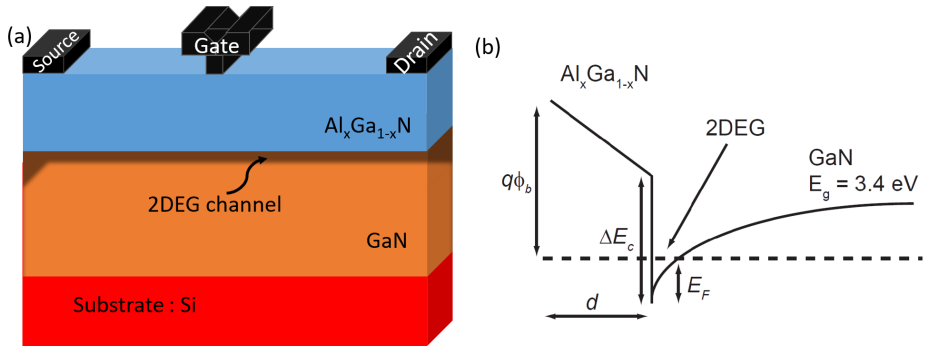

Figure 3.3: (a) Heterostructure and (b) band structure of a typical AlGaN/GaN HEMT.

(AlN) between the two materials of the heterojunction (not shown here), in order to improve the confinement in the 2DEG.

3.2. Devices under test

Our devices under test (DUT) are HEMTs with an AlGaN/GaN heterojunction grown on a high-resistivity silicon substrate by ammonia source molecular beam epitaxy. The heterostructure has a 14 nm thick AlGaN (29 % Al) layer, on a 1.73 μm thick GaN buffer, with an 1 nm spacer of AlN in the middle to improve carrier confinement in the 2DEG and reduce alloy scattering, and a cap of GaN of 0.5 nm thick on the top of the heterostructure. In addition, it has been passivated with N_2O pretreatment and 150 nm of SiN [130]. These devices have been fabricated at the Institut d'Électronique de Microélectronique et de Nanotechnologie (IEMN), University of Lille, France, by the group of Prof. V. Hoel.

In every wafer there are usually structures designed to analyze the quality of the technology, such as transfer length measurement (TLM) structures. TLMs are just a series of ohmic contacts with increasing separation distance L deposited on the heterostructure (without any gate). With the TLMs of the wafer, we can extract the contact resistance (R_C) and the sheet resistance ($R_\square$). The parameter $R_\square$, together with Hall effect measurements of van der Pauw structures [131, 132], which can also be found in the wafer, allows the estimation of the mobility (μ) and the electron sheet density (n_s). In Figure 3.4, a sector of the wafer divided in four quadrants is shown. This pattern is repeated several times along the wafer.

The previously mentioned TLM structures are placed in the down-left quadrant. In this quadrant, there are also Schottky contacts to characterize the gates and van der Pauw structures to obtain the carrier mobility. The dimensions (width and length)

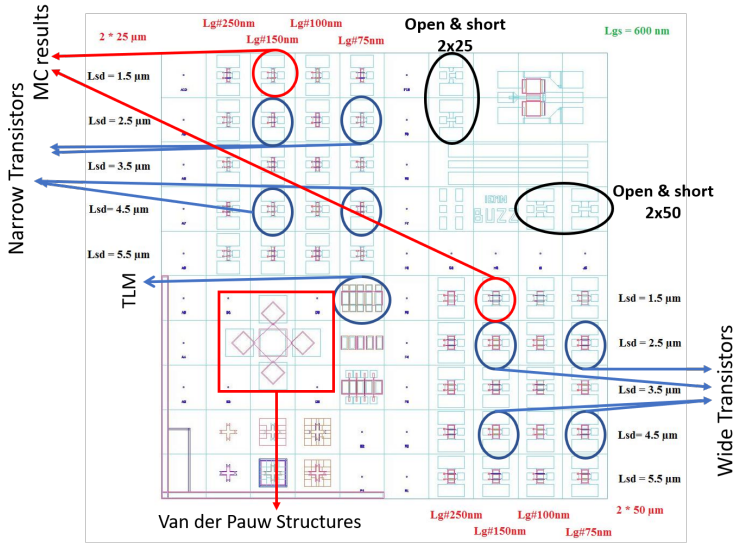

Figure 3.4: Layout of a section of the wafer. HEMTs are located in the up-left and down-right quadrants. The up-right quadrant contains *dummies* and the down-left one has TLMs, Shottky contacts and van der Pauw structures.

of the TLM structures are provided in Table 3.1. In addition, the table includes the lengths of the simulated TLMs. The structures of the up-right quadrant are called *dummies*. They are (empty) structures with pads but without devices, very useful to calibrate the effect of the pads in the RF measurements. HEMTs with different geometries are present in two of the quadrants: narrow transistors are in the up-left quadrant (W= 2 × 25 μm) and wide transistors in the down-right one (W= 2 × 50 μm). [6]

In the wafer there are transistors with several geometries (see Figure 3.4). In order to clarify the meaning of the characteristic dimensions, we have indicated them on the heterostructure in Figure 3.5, denoted as W, L_{GS}, L_{DS} and L_G. Moreover, in Table 3.2, a number is assigned to each transistor of the reticle to easily identify them according to their geometry. In particular, we have experimentally characterized in detail transistors 2, 4, 6, 14 and 16 narrow and wide. For simplicity, along the

Device	Width (W = 100 μm)				
TLM (L)	2 μm	5 μm	10 μm	20 μm	-
TLM^{MC} (L)	0.5 μm	0.75 μm	1 μm	2 μm	5 μm

Table 3.1: Dimensions of the TLMs shown in Figure 3.4.

[6] The 2 stands for the number of transistors in parallel, with a two-finger gate configuration [133].

L_{DS} \ L_G	250 nm	150 nm	100 nm	75 nm
1.5 μm	1	2	3	4
2.5 μm	5	6	7	8
3.5 μm	9	10	11	12
4.5 μm	13	14	15	16
5.5 μm	17	18	19	20

Table 3.2: Numbers assigned to identify the transistors shown in Figure 3.4. Along the manuscript a letter N (narrow, W= 2 × 25 μm) or W (wide, W= 2 × 50 μm) referred to the width will be added to the number of the transistor.

manuscript a letter N (narrow, W= 2 × 25 μm) or W (wide, W= 2 × 50 μm) referred to the width will be added to the number of the transistor and we will use transistor number 2N (L_G =150 nm, L_{DS} =1.5 μm and W= 2 × 25 μm) to be compared with MC simulations.

The HEMTs under study are designed for both high-power and high-frequency applications. These transistors were characterized at the IEMN and exhibit cutoff frequencies above 100 GHz [134], as it can be observed in Figure 3.6(a), calculated from parameters H_{21} and U plotted with the Maximum stable gain (MSG). More concretely, f_t = 116 GHz and f_{max} = 150 GHz. On the other hand, Figure 3.6(b) shows, for a transistor with L_G = 75 nm and W = 2 × 25 μm, at the operating point V_{DS} = 25 V and I_{DS} = 250 mAmm^{-1} with the optimal load ($\Gamma = 0.6\angle 50°$), a power gain G_p = 6.5 dB and a saturated output power density P_{out} = 2.7 Wmm^{-1} with a PAE = 12.5 %. This result is within the state of the art in large signal applications and confirms the interest of these devices.

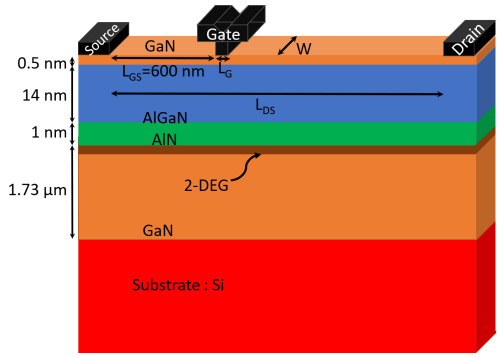

Figure 3.5: Geometry of a HEMT with its characteristic dimensions: gate length (L_G), drain-to-source length (L_{DS}), gate-to-source length (L_{GS}) and width (W).

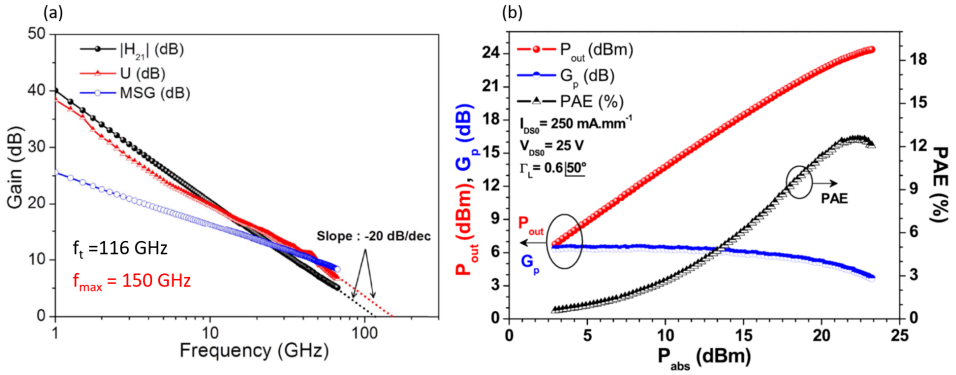

Figure 3.6: Figures of merit of HEMTs [134]: (a) H_{21} (f_t), U (f_{max}) and MSG (b) P_{out}, output power of the device. The 1 dB compression point is the input power P_{abs} at which P_{out} does not follow the linear behavior (it is 1 dB less than expected). The PAE measures the efficiency by which a device converts DC into added RF power.

3.3. DC characterization

In the wafer design, in addition of the HEMTs, other elements are usually included to characterize the fabrication process. Some of these elements are useful, for example, to calculate the carrier mobility, the carrier concentration in the channel, the contact resistance or the features of Schottky contacts, which conform the gate of the transistors. In order to study these elements, we will compare measurements and MC simulations. We will focus on TLMs, measuring the current-voltage curves for every geometry in Table 3.1. The details of the simulator were explained in subsection 1.2.1. With the aim of calibrating the MC tool, we will fix some parameters of the model in order to reproduce the mobility (μ) and concentration (n_s) measured in the samples. In view of of the differences found between the experimental and simulated results of the I-V curves, we have also included in the MC tool the thermal effects presented in subsection 1.2.2. Once the MC model has been properly calibrated with the experimental results of the TLMs, we will study the DC behavior of the transistors. The experimental DC measurements provide information about the current level achieved in the HEMTs and allow to determine the best biasing conditions for the subsequent RF characterization. In the same way as before with the TLMs, some discrepancies appear between the simulated transfer and output characteristics of the transistors and the experimental results. To deal with these discrepancies, we have included in the simulations the influence of the contact resistance and the Schottky barrier, and we have employed the two thermal models (TRM and ETM) to account for self-heating effects.

3.3.1. TLMs

In this subsection, the comparison between experimental results and MC simulations of the TLMs is presented. In order to reproduce the experimental results by means of our MC tool, in subsection 3.3.1.1 we first extract, from DC measurements, the experimental μ and n_s. Immediately after, in subsection 3.3.1.2 we detail the steps followed in the simulation of the heterojunction to adequately reproduce both parameters.

3.3.1.1. Experimental results

In order to determine μ and n_s in our sample, we measure the I-V characteristics of TLMs with different lengths. Figure 3.7(a) shows a scheme and the dimensions (L and W) of the TLMs included in the wafer, which were introduced in Table 3.1. On the other hand, the method to extract the contact (R_C) and sheet ($R_\square$) resistances is summarized in Figure 3.7(b). Analyzing the I-V curves, which follow a linear trend ($V < 1\ V$), and extracting R as the inverse of their slope, we can graph R *vs.* L for every length between contacts in TLMs. Since R *vs.* L also follows a linear trend, just making a linear regression, the y-intercept is $2R_C$ and the slope is $R_\square/W$.

Figure 3.8 confirms that the I-V curves of TLMs are linear for low voltages and that R increases proportionally to the length of the TLM. As expected, shorter TLMs exhibit higher current, and thus smaller R, than longer ones. It is to be noted that the values of R, with values in the order of tens of Ω, obtained initially with a 2-wire technique are similar to those of the wires used for the connections. As a consequence, the sheet density n_s extracted from the estimation of $R_\square$ does not reproduce the experimental one measured with the van der Pauw structures at IEMN. In order to

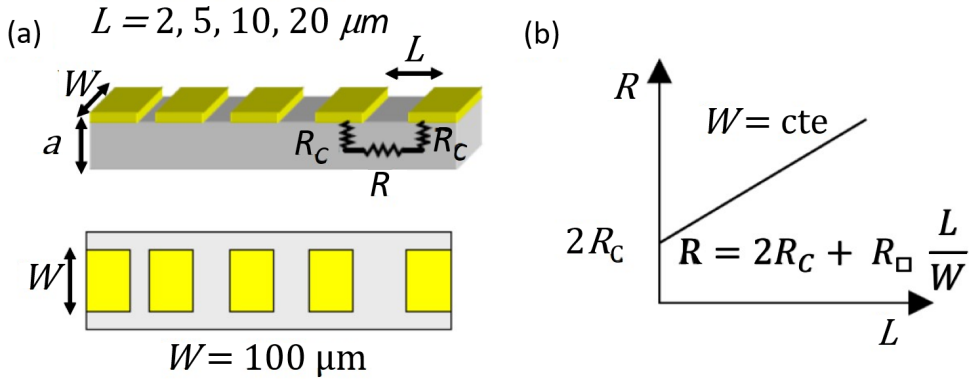

Figure 3.7: (a) Schematic picture of the TLM structure and dimensions ($W = 100\ \mu$m) and (b) diagram of the method used to calculate R_C and $R_\square$.

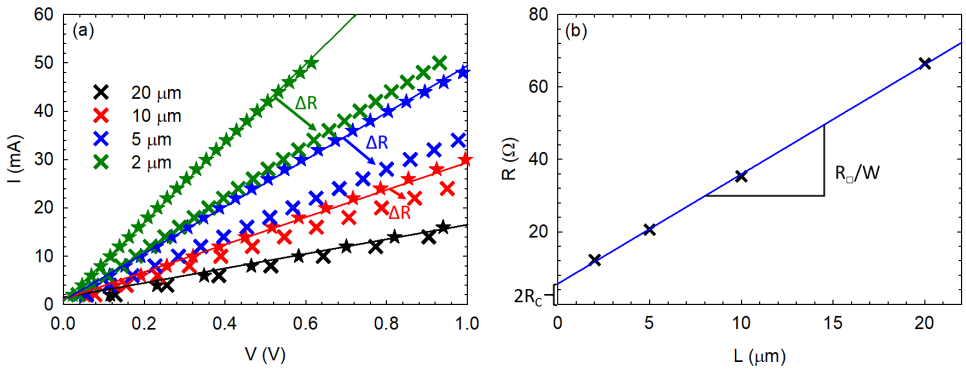

Figure 3.8: (a) Current-voltage curves for the TLMs of lengths 2 μm (green), 5 μm (blue), 10 μm (red) and 20 μm (black). Results obtained with the 2-wire method (crosses) and 4-wire method (stars) are shown. (b) R obtained from the 4-wire measurements as a function of the length of the TLMs.

obtain reliable values of R, we had to improve our measurement technique. The 4-wire (or Kelvin) method is employed. It involves both a ammeter to measure the current through the devices and a voltmeter to measure the voltage between the contacts of the TLM [135]. As observed in Figure 3.8(a), the slopes of the I-V curves are smaller (higher R) when using the 2-wire method as compared to the 4-wire one, since the resistance of the cables has been removed in the second case. In Figure 3.8(b), the values of R obtained with the 4-wire method are plotted for every length and a linear regression is performed, following the method introduced in Figure 3.7. The result of the regression is

$$R(L) = 3.03\ L + 5.66\ \Omega. \tag{3.1}$$

According to Equation 3.1, the y-intercept (5.66 Ω) corresponds to 2 R_C, and therefore $R_C = 0.28\ \Omega{\cdot}mm$. From the slope of the regression, the sheet resistance per μm is $R_\square/W = 3.03\ \Omega_\square/\mu$m. Knowing that $W = 100\ \mu$m, we extract for $R_\square = 302.52\ \Omega_\square$. Previous measurements of Hall effect, done in a van der Pauw structure at the IEMN, and also at the facilities of the USAL (see subsection 3.4.2), provided a mobility for the heterostructure $\mu_n = 2022\ \mathrm{cm}^2/\mathrm{Vs}$. The relationship between the carrier concentration, sheet resistance and mobility is

$$n_s = \frac{1}{\mu_n R_\square e}. \tag{3.2}$$

Substituting in Equation 3.2, the obtained experimental electron density in the channel is $n_s = 1.02 \cdot 10^{13}\ \mathrm{cm}^{-2}$, which agrees well with the value obtained from van der Paw measurements.

3.3.1.2. Monte Carlo simulations

The same heterostructure of section 3.2 has been used in the MC simulator to study TLMs. In order to compare MC simulations with the experimental results, first it is necessary to calibrate the MC tool from the basic principles. In particular, the calculation of the concentration and potential profiles at equilibrium along the contacts is necessary for the study of the device under polarization.

In our tool the electrodes are typically located vertically, extending across the hetero-interface. The first step is the determination of the values of the potential and concentration assigned to these electrodes as boundary condition, assuming that they are always at equilibrium. For this purpose, we calculate the vertical profiles of both quantities under equilibrium conditions ($V = 0$ V) at the center (to be precise their average over some meshes) of a two-terminal sample where the electrodes are placed in the top of the heterojunction, like it was explained in subsection 1.2.1.4. An sketch of the procedure is shown in Figure 3.9(a). A long simulation of 10^6 time steps (1 fs) is performed for this calculation. The obtained vertical profiles at the center of the sample are recorded and used as boundary condition at the lateral electrodes in subsequent simulations, as shown in Figure 3.9(b). In order to improve the accuracy of these profiles, we evaluate them again in the center of the device (now with lateral electrodes) every 10^5 time steps to be used as updated injection profiles in the next iterations. After 10 of such refinements, they are considered as final values [64]. Previous works have proved that the possible error introduced by this way of calculating the equilibrium profiles at the electrodes does not affect more than five meshes inside the structure [136].

In section 3.1, the physical origin of the carriers in the channel of AlGaN/GaN HEMTs was explained. They come from the spontaneous and piezoelectric surface polarization charges. In order to perform the simulations, we have to include the polarization charges. Following the model explained in [128] we can write

$$P_{Al_xGa_{1-x}N/GaN}(x) = P^{sp}_{GaN} - P^{sp}_{Al_xGa_{1-x}N}(x) - P^{pz}_{Al_xGa_{1-x}N}(x), \tag{3.3}$$

where the index *sp* refers to spontaneous polarization due to the polarity of the GaN layer and the index *pz* means piezoelectric polarization due to the strain in the growth of AlGaN over GaN. In the simulation, the polarization charge $P_{Al_xGa_{1-x}N/GaN}$ causes a discontinuity in the normal displacement vector at the hetero-interface (Neumann boundary condition (BC))

$$\vec{n} \cdot (\vec{D_1} - \vec{D_2}) = P_{Al_xGa_{1-x}N/GaN}. \tag{3.4}$$

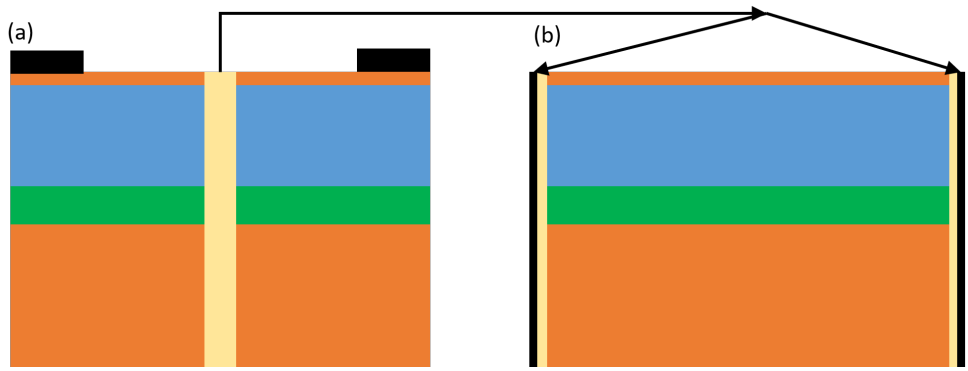

Figure 3.9: (a) Scheme to evaluate potential and concentration profiles in the center of a sample with top electrodes under equilibrium conditions. (b) Sample with vertical electrodes at the laterals, where the profiles previously calculated are used as boundary conditions for the potential and the injection of carriers.

In [128], the *ab initio* calculation of the parameters of Equation 3.3 in cm^{-2} is explained in detail, obtaining

$$P^{sp}_{GaN} = -0.034, \tag{3.5}$$

$$P^{sp}_{Al_xGa_{1-x}N}(x) = -0.090x - 0.034(1-x) + 0.019x(1-x), \tag{3.6}$$

$$P^{pz}_{Al_xGa_{1-x}N}(x) = xP^{pz}_{AlN}[\varepsilon(x)] + (1-x)P^{pz}_{GaN}[\varepsilon(x)], \tag{3.7}$$

where

$$P^{pz}_{AlN} = -1.808\varepsilon + 5.624\varepsilon^2 \; if \; \varepsilon \; < \; 0, \tag{3.8}$$

$$P^{pz}_{AlN} = -1.808\varepsilon - 7.888\varepsilon^2 \; if \; \varepsilon \; > \; 0, \tag{3.9}$$

$$P^{pz}_{GaN} = -0.918\varepsilon + 7.559\epsilon^2, \tag{3.10}$$

where ϵ is the basal strain rate

$$\varepsilon = \frac{a_{GaN} - a(x)}{a(x)}, \tag{3.11}$$

with a_{GaN} the lattice constant of GaN and $a(x)$ the lattice constant of the alloy $Al_xGa_{1-x}N$, which is usually estimated as $a(x) = 0.31986\text{-}0.00891\ x$ in nm. The alloy used in our HEMTs is $Al_{0.29}Ga_{0.71}N$, so that Equation 3.3, replacing $x = 0.29$ in Equations 3.5 to 3.11, provides a value of $P_{Al_{0.29}Ga_{0.71}N/GaN}$ around $1.4{\cdot}10^{13}$ cm^{-2}.

Let us note that the HEMT of this work has three heterojunctions: GaN/AlGaN, AlGaN/AlN and AlN/GaN. In Figure 3.10, the simulated heterostructure in the electrical domain is shown with the names of polarization charges in every heterojunction. From down to top, we have: the GaN/AlN interface, where the total contribution coming from strain and spontaneous polarization is called P_a, the AlN/AlGaN interface,

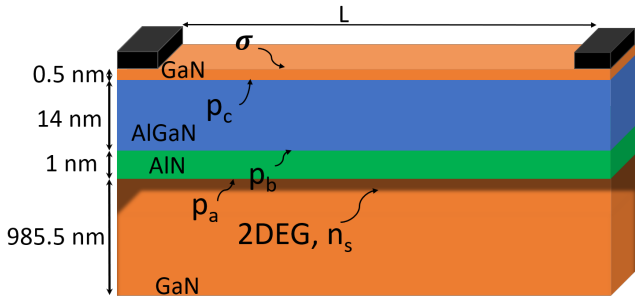

Figure 3.10: Electrical domain with surface and polarization charges included in the model and their position in the heterostructure.

where the total polarization is called P_b and the AlGaN/GaN inteface, whose total contribution is called P_c. It is important to note that these parameters are used as Neumann BCs at the hetero-interfaces (Equation 3.4) when solving Poisson's equation to calculate the potential [55], as we will show in the following.

Therefore, there is a contribution to the total polarization charge from these three heterojunctions. On the other hand, the condition of neutrality of charge must be satisfied

$$P_a + P_b + P_c + \sigma - n_s = 0, \tag{3.12}$$

where σ accounts for the charge present at the top surface of the heterojunction due to the discontinuity GaN/air. In order to reproduce the experimental n_s of the heterojunction calculated in subsection 3.3.1.1, simulations are performed with several combinations of P_a, P_b, P_c and σ satisfying the neutrality condition.

We have performed several simulations with different configurations of the polarization and surface charges, P and σ, respectively. A first one with $P_a = 12{\cdot}10^{12}$ cm^{-2}, P_b =-2·10^{12} cm^{-2}, P_c =-6·10^{12} cm^{-2} and $\sigma = 4{\cdot}10^{12}$ cm^{-2}, which does not satisfy the neutrality condition with the experimental sheet-carrier density n_s (it provides $n_s = 8 \cdot 10^{12}$ cm^{-2}). A second one with P_a= 15·10^{12} cm^{-2}, P_b =-2·10^{12} cm^{-2}, P_c =-3·10^{12} cm^{-2} and $\sigma = 0{\cdot}10^{12}$ cm^{-2}, which satisfies neutrality with the experimental n_s, but it has no surface charge in the GaN/air interface. And finally, $P_a = 15{\cdot}10^{12}$ cm^{-2}, P_b =-2·10^{12} cm^{-2}, P_c =-2·10^{12} cm^{-2} and σ =-1·10^{12} cm^{-2}, which satisfies the mentioned condition with a negative surface charge in the top. In Figure 3.11(a), we show the potential profile *vs.* the vertical length for the first meshes at the top of the device, where the differences in the slopes of the potential at the heterojunctions (discontinuities in the electric field) can be observed. The presence of the 2DEG and the heterojunction AlGaN/AlN/GaN is evidenced in the figure at around 15 nm. The region close to the top shown in the inset exhibits three different

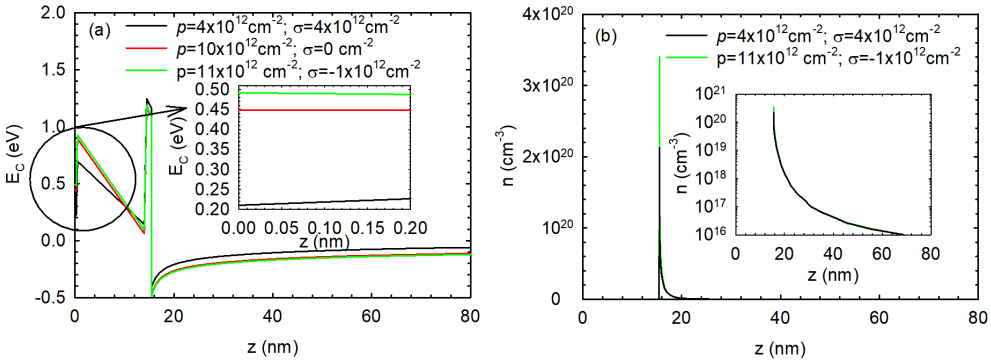

Figure 3.11: (a) Vertical potential profiles (conduction band edge) along the first layers of the device for three configurations of P and σ. Inset: zoom of the profiles near the GaN/air surface. (b) Concentration profile for the first and third configurations. Inset: concentration profiles in logarithmic scale.

behaviors related with the value of σ. The first configuration has a positive slope near the surface, the second is flat and the third configuration has a small negative slope. The second slope at around $z = 0.5$ nm becomes negative due to the presence of P_c. The influence of P_b at the third heterojunction (around $z = 14.5$ nm) leads to a stronger negative slope in the potential. And, finally, at the fourth junction (around $z = 15.5$ nm) the slope becomes positive due to the high value of P_a. Note that the first configuration satisfies the neutrality condition with a value of $n_s = 8 \cdot 10^{12}$ cm^{-2}, smaller than the experimental one ($n_s \approx 1.0 \cdot 10^{13}$ cm^{-2}), which reflects in higher values of the conduction band edge at the 2DEG region. We also note that the potential reference is assigned to the bottom of the device, as previously explained in subsection 1.2.1. The arbitrary election of the reference will be clarified in the next section with the inclusion of a third terminal.

In Figure 3.11(b), the profile of electron concentration *vs.* length in the vertical direction is plotted for the first and third case, where it can be observed that the carriers fundamentally accumulate in the potential well and the concentration is higher for the third configuration. This result is even more evident in the inset, where the concentration profiles are plotted in logarithmic scale. As expected, the total concentration in third scenario is $n_s \approx 1.0 \cdot \ 10^{13}$ cm^{-2}, satisfying the charge neutrality condition. In the following, we will consider in the simulations the polarization and surface charges corresponding to the third case. Finally, the differences in the individual values of P_a, P_b and P_c, does not influence the electrons at the 2DEG, only their global value $P = P_a + P_b + P_c$ is of interest since typically no carrier will be present at the top layers.

In order to reproduce the properties of electron transport in the channel, we have included roughness scattering at the heterointerface in the simulator by means of a simple model, which considers that a given fraction of the electron reflections is not specular but diffusive [137]. When an electron reaches the surface, it is a random number which decides the diffusive or specular behavior. The fraction of electron reflections considered as diffusive is the so called Percentage of Diffusive Reflections (PDR), given in the model as %.

We have simulated the I-V curves of TLMs with different lengths: 0.5, 0.75, 1, 2 and 5 μm. These values of L are shorter than those of the actual TLMs in the wafer due to the too long computation times that would require their simulation. In Figure 3.12(a), R is plotted *vs.* L for the three shorter TLMs (0.5, 0.75 and 1 μm) simulated with four values of PDR (0, 0.25, 0.50 and 0.75 %). As observed, the results of the simulations best fitting the experimental linear dependence of R on L (blue line, Equation 3.1) with $R_{\square} = 302\ \Omega_{\square}$ correspond to a $PDR = 0.25$ %.

As previously mentioned, the simulation of the actual TLMs (2 to 20 μm) would require longer times of computation and/or longer cells with a lower accuracy of the simulation. Therefore, we model shorter TLMs (L = 500 nm, 750 nm, 1, 2 and 5 μm), which require more reasonable computation times. The two longer simulated lengths coincide with actual lengths of TLMs in the wafer. In Figure 3.12(b), we plot R extracted from both simulated and experimental results, jointly with the line of Equation 3.1, adding R_C to the values obtained with the simulations. The comparison, with the simulated TLMs following the same trend that the TLMs of the wafer, indicates that the values chosen for the parameters of the model in the MC simulation

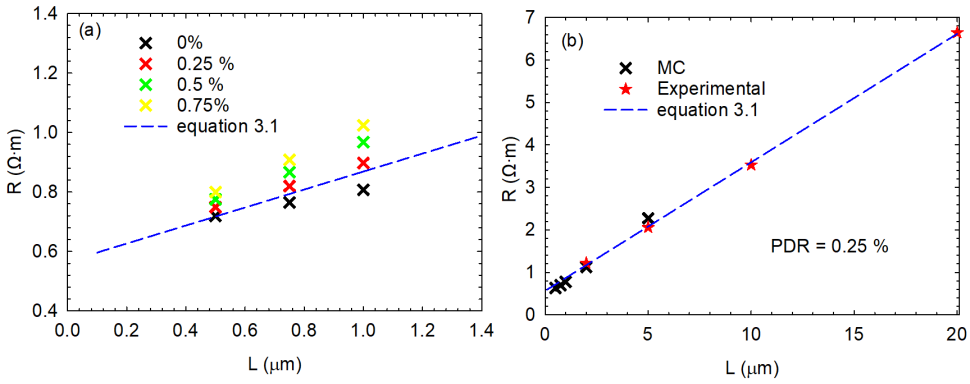

Figure 3.12: (a) R *vs.* length obtained from the simulated I-V characteristics of TLMs for PDR from 0 % to 0.75 %. The blue line corresponds to the linear fitting of experimental values. (b) R *vs.* length plot comparing experimental and MC results for $PDR = 0.25$ %.

reasonably reproduce the carrier mobility in the heterostructure. In the cases of $L = 2$ and 5 μm, we have experimental results and simulations, resulting in similar values of R.

Once the experimental carrier concentration and mobility (near equilibrium) have been reproduced, we compare the simulated I-V curve with the experimental one in a wider bias range, from 0 to 10 V. In Figure 3.13, the comparison is shown for two lengths, $L = 2$ and 5 μm. For $V < 1$ V, as expected, the MC I-V curves fit very well the experimental ones. However, when $V > 1$ V, the measured current is smaller than that obtained with the simulations. In addition, at high voltages the measurements show current saturation, while the simulations do not. These differences are attributed to the fact that the simulations are performed at a constant temperature $T = 300$ K, without considering any self-heating induced by power dissipation inside the device.

In order to analyze the influence of temperature on the current level, we have performed simulations at different constant temperatures (uniform inside the device), $T = 300$, 400 and 500 K, and compared them with the values measured at 300 K. In Figures 3.14(a) and (b) we plot the simulated I-V curves for $L = 2$ μm and $L = 5$ μm, respectively. Even if a good agreement is not obtained for any of the considered temperatures, the results of the simulations at high temperatures are able to better reproduce the trend of the experimental I-V curve (for high values of the applied voltage V), confirming that thermal effects are relevant for $V > 1$ V. Moreover, the results indicate that the shorter device reaches higher temperatures due to the higher I (smaller R).

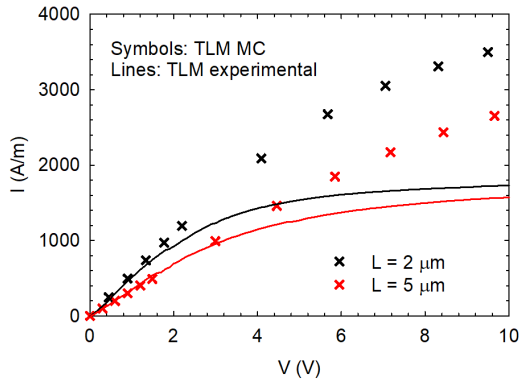

Figure 3.13: Measured and simulated current-voltage characteristics of TLMs with lengths $L = 2$ and 5 μm.

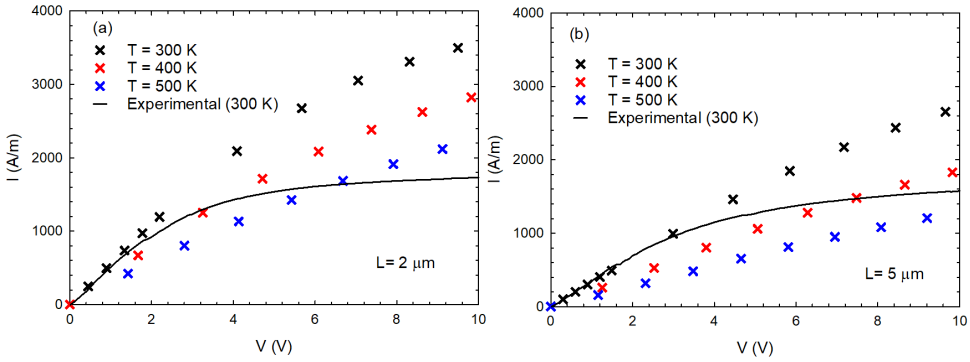

Figure 3.14: Current-voltage characteristics simulated at different constant temperatures as compared with the experimental one measured at 300 K for TLMs of length (a) $L = 2$ μm and (b) $L = 5$ μm.

Although we have been able to reduce the current level by increasing the temperature at which the simulation is performed, there are still significant discrepancies between the experiments and simulations, what indicates that a model considering the specific heating effects taking place at every bias point is necessary. In subsection 1.2.2, two of such models were introduced. The simpler one is the thermal resistance model (TRM), in which the (uniform) temperature at which each bias condition is simulated is given by the equation (see subsection 1.2.2)

$$T_{latt} = T_{heat-sink} + R_{TH} \times V_{MC} \times I_{MC}. \tag{3.13}$$

The second and more sophisticated method is based on the resolution of the heat conduction equation (HCE) self-consistently with the electrical MC simulation (ETM).

As first approximation, and in order to check the impact of thermal effects on the I-V curve, we compare the results of the TRM model and the experimental measurements. In Figures 3.15(a) and (b) we show I-V curves simulated using different values of R_{TH}. In the background, the value of T_{latt} calculated with $R_{TH} = 20$ mm·K/W is represented to have an idea of the temperatures reached inside the device at each bias point. As expected, the current obtained within the TRM is smaller than that calculated at a constant temperature of 300 K. Comparing the two lengths, the shorter TLM ($L = 2$ μm), shown in Figure 3.15(a), reaches higher temperatures ($T \sim 600$ K) than the longer one ($L = 5$ μm), shown in Figure 3.15(b), as expected from the higher I. While the agreement at low V, where dissipation is small, is still good, it is remarkable the improved current saturation obtained in simulations with the TRM

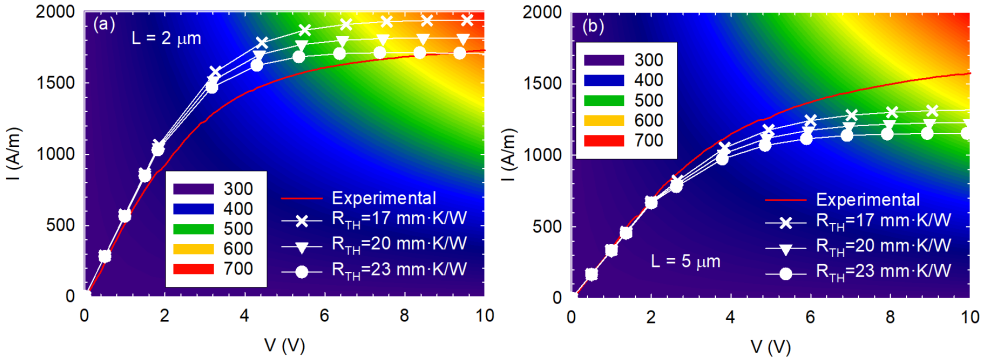

Figure 3.15: Simulated current-voltage characteristics considering the TRM with different values of R_{TH} for TLMs with (a) $L = 2$ μm and (b) $L = 5$ μm, as compared with the experimental I-V curve measured at 300 K. The background color represents T_{latt} obtained for $R_{TH} = 20$ mm·K/W.

at high voltages, which is now much more similar to that of experimental data. We can conclude that TRM modeling constitutes a significant advantage with respect to the iso-thermal study, where the current does not saturate. In principle, the agreement can be even improved by means of the ETM, as we will show in the study of transistors in next subsections.

3.3.2. Transistors

Once our MC tool has been calibrated in order to replicate the main experimental features of the TLMs, now we will employ it to study the 3-terminal HEMT. Although we have experimentally characterized all the transistors of the wafer (see Appendix A), we will focus our MC study in transistor number 2N ($L_G = 150$ nm, $L_{DS} = 1.5$ μm and $W = 2{\times}25$ μm). We start our study with measurements and simulations of the transistor at room temperature. In Figures 3.16(a) and (b), we plot the measured and simulated output and transfer characteristics, respectively. In the MC results we have not included any thermal effect nor the influence of the contact resistances. In the figures, it can be observed that the current obtained in the simulation is much higher than the experimental one. Attending to Figure 3.16(b), it is also remarkable the shift in the threshold voltage between both results. The measured HEMTs have two ohmic contacts in source and drain and a Schottky contact in the gate. For a correct comparison between simulations and measurements, it is necessary: (i) to take into account the experimental contact resistances (related to the metalization process), which change the V_{DS} and V_{GS} values corresponding to MC results, and (ii) to replicate properly the threshold or pinchoff voltage, the value of V_{GS} at which

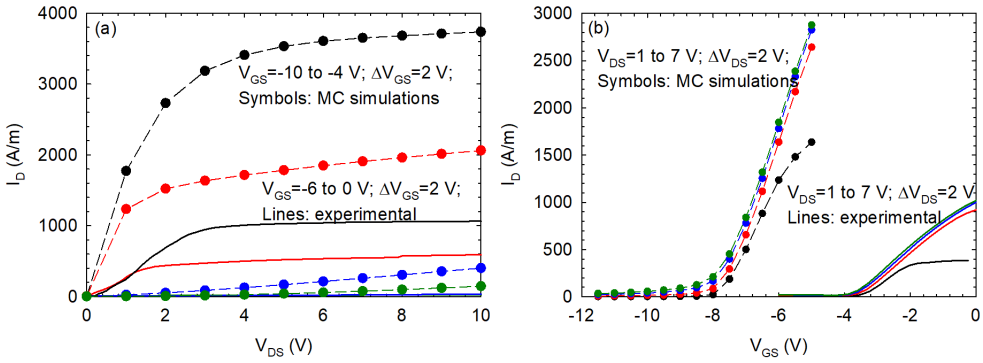

Figure 3.16: Measurements and MC simulations without post-processing of the (a) output and (b) transfer characteristics of transistor 2N.

the channel it is depleted. There are two main contributions to justify the shift in the pinchoff between experiments and MC simulations. In subsection 1.2.1.4, we have indicated that the reference of the potential was at the bottom of the device, which is an arbitrary choice having an influence in the values of V_{GS}. The second contribution is related to the Schottky barrier of the gate, which up to now is not included in the simulation.

In conclusion, Figures 3.16(a) and (b) suggest that a post-processing must be done to reproduce the experimental data. With this intention, we follow the method explained in [138], based on Figure 3.17. The transformations needed to include the contact resistances R_C are given by

$$V_{DS} = V_{DS}^{MC} + I_D \cdot (2R_C + R_\square \cdot l), \tag{3.14}$$

$$V_{GS} = V_{GS}^{MC} + V_{SCH} + I_D \cdot (R_C + R_\square \cdot l). \tag{3.15}$$

The voltages without superscript represent the external or experimental voltages, while the ones with superscript MC are the internal or MC voltages (those used in the simulations). Note that we include an additional term $R_\square \cdot l$, which comes from the ohmic behavior of a small portion of the source-to-gate region of length l that is not considered in the simulation to save computation time. l is 300 nm while the L_{GS} of the real HEMTs is 600 nm. This strategy reduces the time required by the simulations without losing accuracy in the results because of the ohmic nature of transport in such a region. The other parameter used in Equation 3.15 is V_{SCH}, which represents the Schottky barrier of the gate and the shift in the reference of the potential.

In order to find the parameters which best fit the experimental data, we implement the transformations of Equations 3.14 and 3.15 with different values of R_C and V_{SCH} and the experimental value of $R_\square = 300\ \Omega_\square$. First we perform calculations with

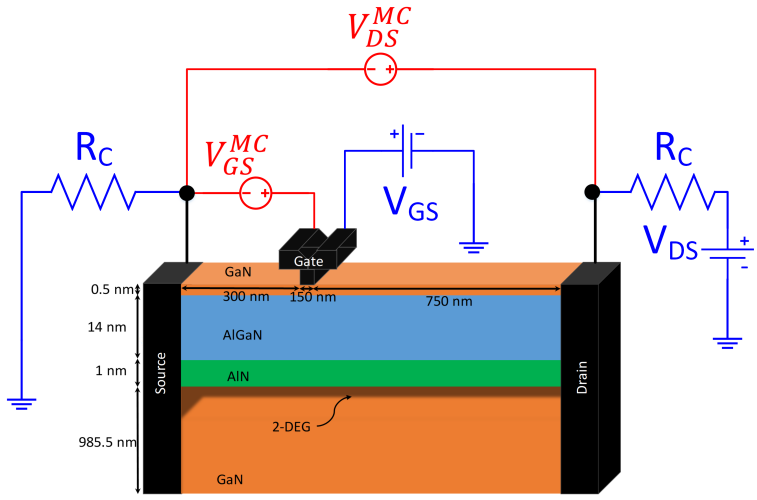

Figure 3.17: Scheme for the inclusion of contact resistances in the HEMT. Blue lines stand for external or experimental elements and the red ones for MC (intrinsic).

$R_C = 1\ \Omega \cdot \text{mm}$ and $R_C = 1.25\ \Omega \cdot \text{mm}$, and $V_{SCH} = 4.5$ V. We show the obtained output and transfer characteristics in Figures 3.18(a) and (b), respectively. It can be observed that the slope of the experimental current in the region $V_{DS} < 1$ V is reproduced for $R_C = 1\ \Omega \cdot \text{mm}$, while that obtained with $R_C = 1.25\ \Omega \cdot \text{mm}$ is smaller. However, the I_D^{max} of the MC simulations is still much higher than the experimental one for both values of R_C and the channel is not completely closed for high V_{DS}. A possible solution to reproduce the I-V curves with this technique is the use of a higher value for V_{SCH} to reduce I_D^{max} and to close properly the channel.

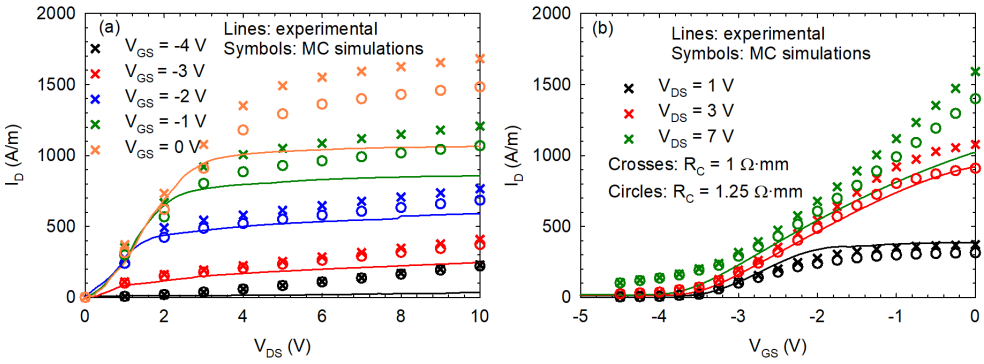

Figure 3.18: (a) Output and (b) transfer characteristics with a post-processing including $R_C = 1\ \Omega \cdot \text{mm}$ (crosses) and $R_C = 1.25\ \Omega \cdot \text{mm}$ (circles), and $V_{SCH} = 4.5$ V. (a) V_{GS} from -4 V to 0 V with $\Delta V_{GS} = 1$ V and (b) $V_{DS} = 1$ V, 3 V and 7 V.

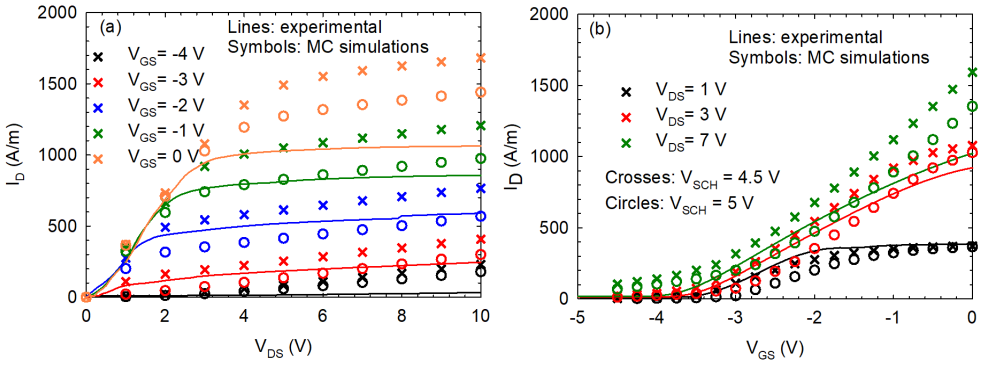

Figure 3.19: (a) Output and (b) transfer characteristics with a post-processing including $R_C = 1\ \Omega \cdot \text{mm}$, and $V_{SCH} = 4.5$ V (crosses) and $V_{SCH} = 5$ V (circles). (a) V_{GS} from -4 V to 0 V with $\Delta V_{GS} = 1$ V and (b) $V_{DS} = 1$ V, 3 V and 7 V.

Now, we keep $R_C = 1\ \Omega \cdot \text{mm}$ and we compare the results of Equations 3.14 and 3.15 for $V_{SCH} = 4.5$ V and $V_{SCH} = 5$ V. The results are plotted in Figures 3.19(a) and (b). In the output characteristics, the low-bias slope is fitted satisfactorily, since we use the appropriate R_C, but I_D^{max} is not well reproduced in any case. When $V_{SCH} = 5$ V, a more closed channel reduces the maximum current, but the obtained V_{TH} does not fit the experimental one, as it can be observed in Figure 3.19(b). We conclude that the more suitable values to replicate the low-bias regime are $V_{SCH} = 4.5$ V and $R_C = 1\ \Omega \cdot \text{mm}$, which we will use in next sections. It seems also clear that using a uniform simulation temperature of $T = 300$ K, as we have done so far, it is not possible to reproduce the experimental behavior under high current conditions, in particular I_D^{max}, and self-heating effects must be taken into account.

3.4. Thermal effects

Microwave devices able to operate at high temperature without external cooling could push the development of low-cost, high-power, high-frequency applications. GaN, thanks to its wide bandgap, is a good candidate to this end, since heating is not an issue until temperatures much higher than in other semiconductors, beyond 600 °C. Moreover, the gate-leakage current can also be lower. Therefore, GaN-based devices are expected to operate at higher temperatures than other technologies [139]. Anyway, thermal effects may have a strong influence on the behavior of the devices, mainly degrading their performance, and need to be investigated in detail.

3.4.1. Room temperature operation

In subsection 1.2.2, we described the techniques to include thermal effects. Two models were presented: the thermal resistance model (TRM) and the electrothermal model (ETM) [36]. In the TRM, all the meshes in the electrical domain have the same uniform temperature, given by Equation 3.13. In the ETM, the temperature is not uniform and it is calculated for every mesh by means of the resolution of the HCE consistently with the electrical MC simulation.

Within the TRM, we have done simulations with different values of R_{TH} in order to find the optimal one. Figure 3.20 shows the simulated output characteristics of transistor 2N (L_G = 150 nm, L_{DS} = 1.5 μm and W = 2×25 μm) considering two values of the thermal resistance[7]: R_{TH} = 18.5 mm·K/W and R_{TH} = 19.25 mm·K/W. It can be observed that the levels of current are reproduced much better than in Figure 3.18 thanks to the inclusion of thermal effects, which allow to replicate more closely the physical conditions inside the device. As expected, the current is smaller for larger R_{TH} because T_{latt} is higher for the same P_{Diss}, and scattering becomes more intense at higher temperatures.

Even though the current levels for the lower R_{TH} are still systematically higher than the experimental ones, for the higher R_{TH} and intermediate values of V_{GS} simulations and measurements are in a reasonably good agreement. Near pinchoff conditions, the MC values of I_D are higher than the experimental ones, since the channel cannot be completely closed due to strong drain-induced-barrier-lowering ef-

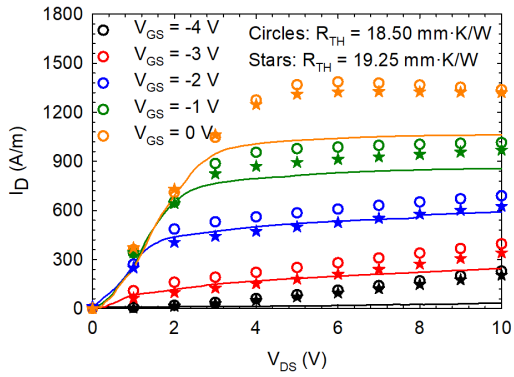

Figure 3.20: Output characteristics of transistor 2N considering thermal effects using the TRM with R_{TH} = 18.50 mm·K/W (circles) and R_{TH} = 19.25 mm·K/W (stars). Lines correspond to the experimental values.

[7] It is important to remark that we have performed a post processing using V_{SCH} = 4.5 V and R_C = 1 Ω · mm.

fects (DIBL) taking place in the simulations [115]. These short-channel effects could be mitigated with the inclusion of a p-type doping in the GaN layer of the heterostructure, as detailed in [140, 141]. The p-type doping has the effect of a better confinement of electrons near the heterojunction, originated by the depletion field of deep acceptors. This confinement can be achieved by increasing the donor density in the GaN, but it cannot be increased too far since it could result in reduced mobility and too low carrier concentration in the channel. Despite the explained potentiality of considering the p-type doping to improve the agreement between simulations and measurements, we decided to focus our work on the influence of thermal effects on the equivalent circuit of HEMTs for intermediate current levels, for which the agreement is already satisfactory. On the other hand, under open channel conditions the I_D of the simulation is also higher than the experimental one as a consequence of the DIBL and punch-through effects previously explained.

Figure 3.21(a) shows the experimental and simulated output characteristics obtained for a value of $R_{TH} = 19.25$ mm·K/W, with T_{latt} at each operating point represented by the background color. Temperatures above 500 K are reached for the higher currents (larger than experimental ones). On the other hand, the transfer characteristics for several V_{DS} are plotted in Figure 3.21(b).

It is again evidenced that the levels of current and V_{TH} are correctly reproduced, but the pinchoff of the channel is not well replicated for $V_{DS} > 1$ V. It is important to remind that in this model the temperature is uniform in the electrical domain, but infrared and thermoreflectance measurements have shown that the temperature in HEMTs is not uniform through the transistor [35]. Therefore, the next step is to use the ETM model.

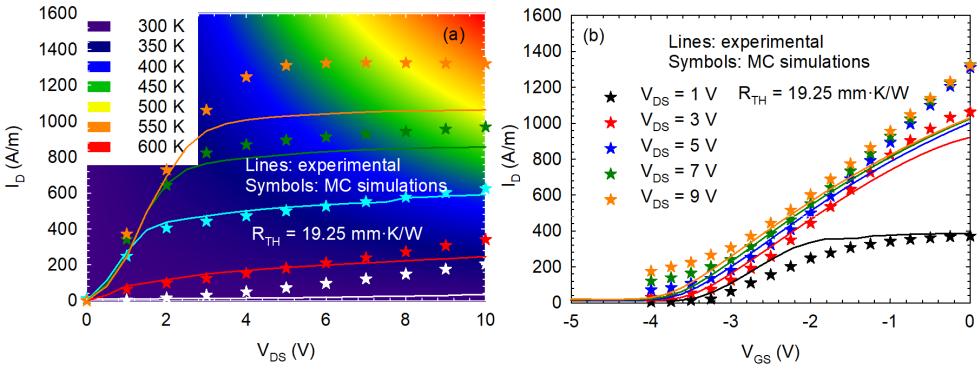

Figure 3.21: (a) Output characteristics obtained with $R_{TH} = 19.25$ mm·K/W. The background color represents T_{latt} at each operating point according Equation 3.13. V_{GS} from -4 V to 0 V, with $\Delta V_{GS} = 1$ V. (b) Transfer characteristics.

material	κ ($W \cdot K^{-1} \cdot m^{-1}$)
AlGaN	30
GaN	130
Si	156
Au	300
AlN	170

Table 3.3: Thermal conductivities used in the resolution of the HCE.

ETM simulation, thanks to the self-consistent solution of the HCE with the electrical MC simulation, provides a non-uniform distribution of temperatures inside the device with local values in every mesh, which is closer to the actual physical conditions. In order to solve the heat equation (see subsection 1.2.2.2), the thermal conductivities (κ) of the materials in the heterojunction are needed. We show the values used in the simulations in Table 3.3. We assume a κ independent of temperature as an approximation, taking the value at $T = 300$ K. As explained in subsection 1.2.2.2, within this model both a thermal and a electrical domain are considered, as sketched in Figure 3.22. The area of the electrical domain (inside the thermal domain) is delimited by the dashed yellow line. 200 μm of gold contacts, 730 nm of GaN and 300 μm of Si substrate are added to the electrical domain to compose the thermal domain.

We perform the simulations with the heat-sink[8] at a temperature $T = 300$ K and the thermal conductivities of Table 3.3. Figure 3.23(a) shows the output cha-

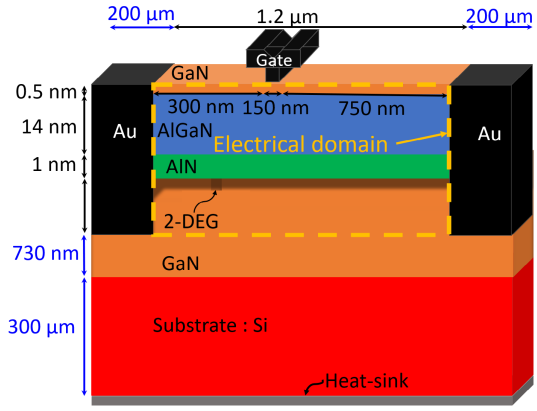

Figure 3.22: Thermal and electrical domains of the simulation for the ETM. Blue lines and numbers stand for added elements in the resolution of the HCE.

[8] Bottom of the device at constant temperature (see Figure 3.22).

racteristics obtained with the ETM.[9] It can be observed that the levels of current in Figures 3.23 and 3.20 are very similar, since the value of R_{TH} used in the TRM simulations is in agreement with the slope of the T *vs.* P_{Diss} curve obtained with the ETM simulation, as will be shown in Chapter 4. On the other hand, in the transfer characteristics, plotted in Figure 3.23(b), V_{TH} is also well reproduced, but DIBL effects are still the main reason of the disagreement with measurements.

In [36] it was argued that both models, TRM and ETM, are equivalent because the current is determined by the average temperature (T_{av}) inside the device, which is very similar with both models. Note that in the TRM the temperature is uniform, but in the ETM it changes from mesh to mesh. In this work, we confirm the argument, since both models exhibit practically the same levels of current, which compare favorably with the experimental current for intermediate values of V_{GS}, as observed in Figure 3.24, where the output characteristics obtained with both models are compared with measurements.

Finally, to achieve a more realistic level of maximum current in the simulation, the thermal barrier between the GaN layer and the Si substrate can also be taken into consideration [56]. The defects present at the GaN/Si interface originate the presence of a thermal barrier, which is modeled as a layer of a thickness Δ_{TBR} and low thermal conductivity κ_{TBR}. The value of the thermal barrier in terms of this two parameters is $TBR = \frac{\Delta_{TBR}}{\kappa_{TBR}}$. TBR models the opposition of an interface to the heat flow. It includes contributions from crystalline defects close to interfaces and low-thermal-conductivity interfacial layers. The combination of these elements contributes to the total device thermal resistance in any heteroepitaxial GaN device [142].

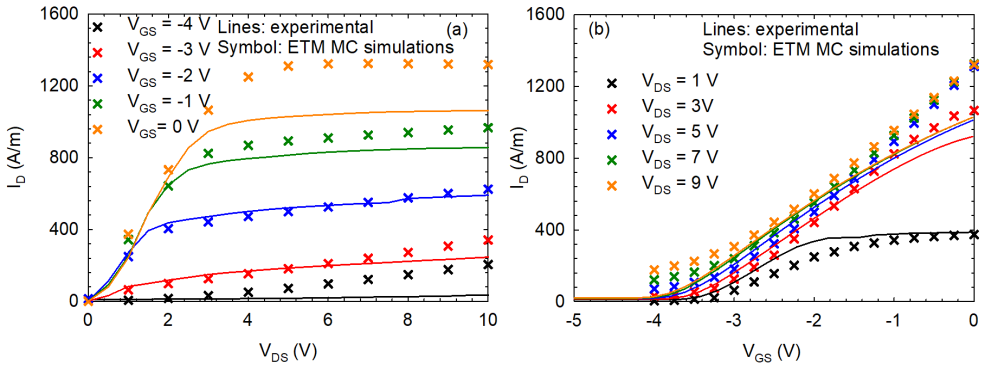

Figure 3.23: (a) Output and (b) transfer characteristics of transistor 2N simulated using thermal effects with the ETM as compared with measurements.

[9] Again we have used a value of $V_{SCH} = 4.5$ V and $R_C = 1\ \Omega \cdot$ mm.

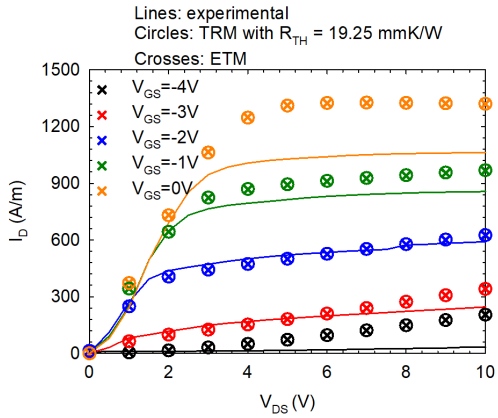

Figure 3.24: Output characteristics obtained both with the TRM ($R_{TH} = 19.25$ mm $\cdot$ K/W) and the ETM compared with measurements.

In Figure 3.25, the I_D *vs.* V_{DS} curve at $V_{GS} = 0$ V obtained with two values of TBR is plotted as compared with the experimental results. As observed, the I_D^{max} resulting from the higher TBR ($TBR = 15$ Km^2/W) is smaller as a consequence of the higher temperatures reached inside the device, which enhance the intensity of scattering. In contrast, the results obtained with $TBR = 1.2$ Km^2/W are practically the same as those achieved without TBR, since this low value of the TBR hardly modifies the temperature inside the device.

Figure 3.26 shows the (a) output and (b) transfer characteristics obtained considering a thermal barrier $TBR = 15$ Km^2/W. As already pointed out, I_D at intermediate V_{GS} is well reproduced. However, there is still an evident DIBL given by punch

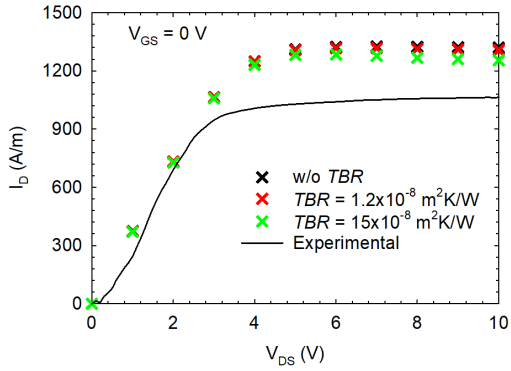

Figure 3.25: Output characteristics obtained with the ETM without TBR and including it with values of 1.2 Km^2/W and 15 Km^2/W, as compared with experimental results.

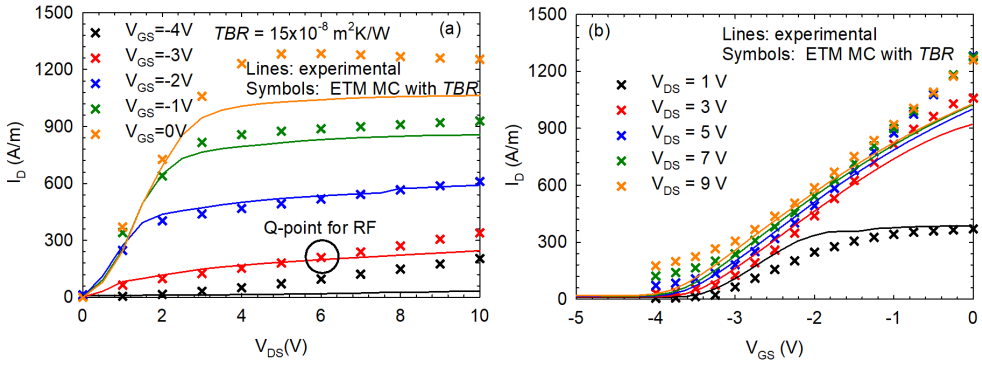

Figure 3.26: (a) Output and (b) transfer characteristics obtained with the ETM considering TBR = 15 Km^2/W as compared with experimental results. The circle at V_{DS} = 6 V, V_{GS} =-3 V, indicates the quiescent point (Q-point) for the subsequent RF MC characterization in subsection 4.1.2.2 of Chapter 4.

through in the simulations, where the pinchoff is not complete in the subthreshold region. In any case, the curves obtained in the simulations for V_{GS} between -3 V and -1 V are in a reasonable agreement with the measurements and its levels of current. In particular, we will choose the point V_{DS} = 6 V, V_{GS} =-3 V, at which the agreement is very good, as bias conditions to be used in the subsequent RF MC modeling of the small-signal equivalent circuit of the HEMT in subsection 4.1.2.2 of Chapter 4.

In order to understand the differences and similarities between the TRM and the ETM with TBR, the average temperature and the map of temperatures obtained with the ETM can be useful. Table 3.4 shows the average temperatures (T_{av}) of the ETM in the electrical domain and the values of T_{latt} resulting from Equation 3.13 in the TRM for several bias conditions. At intermediate V_{GS}, T_{av} is similar to T_{latt}, which is consistent with the similar values of I_D obtained with both models. However, in open channel conditions T_{latt} in the TRM is lower than T_{av} in the ETM. The origin of this difference will be studied in subsection 4.1.2.2.

In the ETM, T_{av} is obtained from a map of temperatures, which allows us to identify the hotspots and the regions where heat dissipation is more pronounced. The maps obtained in the electrical domain at the bias points (a) V_{DS}^{MC} = 3 V,

Bias point (V)	MC Bias point (V)	T_{av} (ETM)	T_{latt} (TRM)
V_{DS} = 6 V V_{GS} =-3 V	V_{DS}^{MC} = 6 V V_{GS}^{MC} =-8 V	324 K	324 K
V_{DS} = 6 V V_{GS} =-2 V	V_{DS}^{MC} = 8 V V_{GS}^{MC} =-7.5 V	375 K	379 K
V_{DS} = 10 V V_{GS} = 1 V	V_{DS}^{MC} = 10 V V_{GS}^{MC} =-4 V	664 K	650 K

Table 3.4: Average temperatures in each model at three bias point of interest.

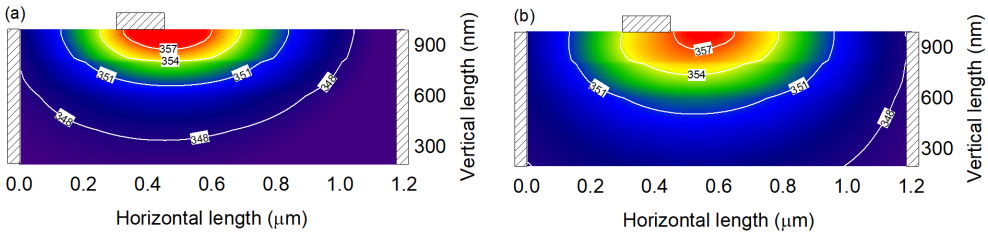

Figure 3.27: Map of temperatures obtained in the electrical domain for the bias points: (a) V_{DS}^{MC} = 3 V, V_{GS}^{MC} =-6.5 V (V_{DS} = 3 V, V_{GS} =-0.5 V) and (b) V_{DS}^{MC} = 10 V, V_{GS}^{MC} =-8.5 V (V_{DS} = 9 V, V_{GS} =-3 V). Shaded areas indicate the positions of the contacts.

V_{GS}^{MC} =-6.5 V (V_{DS} = 3 V, V_{GS} =-0.5 V) and (b) V_{DS}^{MC} = 10 V, V_{GS}^{MC} =-8.5 V (V_{DS} = 9 V, V_{GS} =-3 V) are plotted in Figure 3.27. These points have not been arbitrarily selected. The dissipated power (P_{Diss}) is the same in both bias conditions, P_{Diss} = 2.8 W/mm, although in the first one the channel is open, whereas the second point is under a quasi-pinchoff bias condition. Although the hotspot is different, 364 K in open bias condition and 358 K in quasi-pinchoff, T_{av} = 350 K is similar in both conditions. It is also interesting that the position of the hotspot, as observed in the figures, is in the gate-to-drain region. The most important difference between both conditions is in the temperature distribution, since the highest temperatures at the quasi-pichoff condition exhibit a highly focused distribution at the gate side of the gate-to-drain region, while in open channel conditions they are more homogeneously distributed and extend also under the drain side of the gate. This behavior is explained in [41] in terms of the more or less constricted region through which I_D flows in the device. In quasi-pinchoff, a high V_{GS} is applied to form a local depletion region within the channel that induces a zone of high electrical resistance and a high field, at the drain side of the gate where a strong heat generation takes place, originating a quite localized hotspot. However, in the open channel condition, even if the dissipated power is the same, V_{GS} is lower, allowing the current flow through a less constricted region, so that heat generation and the resulting temperature are more spread out and more symmetrical around the gate.

To confirm that the constriction of the current is at the origin of the differences between the temperature distributions in open and quasi-pinchoff conditions, it is better to compare operating points with similar V_{DS}. In this case, since the dissipated power is different, we divide the profile of temperature by the maximum value. Figures 3.28(a) and (b) show the maps of temperatures at the bias points V_{DS}^{MC} = 5 V, V_{GS}^{MC} =-4 V (V_{DS} = 4.5 V, V_{GS} = 1 V) and V_{DS}^{MC} = 5 V, V_{GS}^{MC} =-8 V (V_{DS} = 4.5 V, V_{GS} =-3 V), respectively. These maps confirm the previous findings. The open chan-

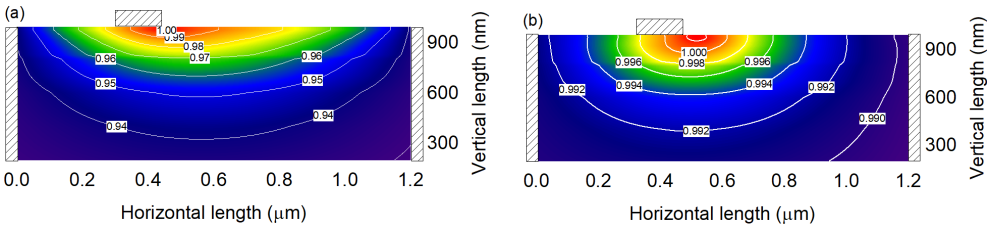

Figure 3.28: Map of temperatures in the electrical domain normalized to the maximum value for the bias points: (a) V_{DS}^{MC} = 5 V, V_{GS}^{MC} =-4 V (V_{DS} = 4.5 V, V_{GS} = 1 V) and (b) V_{DS}^{MC} = 5 V, V_{GS}^{MC} =-8 V (V_{DS} = 4.5 V, V_{GS} =-3 V). Shaded areas indicate the positions of the contacts.

nel condition shows a more homogeneous thermal distribution under the gate than the quasi-pinchoff condition, with a more focused distribution towards the drain. Although we have confirmed that both ETM and TRM lead to practically the same results, since T_{av} or T_{latt} determine the behavior of the device, we remark that the ETM gives more information about the physics of thermal effects inside the device, since it is able to capture the specific effects of the V_{GS} and V_{DS} voltages, providing the temperature distribution and allowing the location of the hotspots inside the HEMT. However, TRM require less effort to treat thermal effects, avoiding dealing with the steady-state HCE and the details of the layer structure of the thermal domain.

In this work, the experimental I-V characteristics have been obtained applying voltages at the terminals of the transistors and measuring the resulting current. So far, in all measurements the SMUs are biasing the HEMTs in a continuous fashion, i.e., during all time of the measurement the terminals are subjected to an excitation. We called this setup DC measurement. However, if the bias is applied during a small period of time and returns to a previously determined bias condition just after the measurement, we have pulsed measurements (see subsection 1.1.2 and Figures 1.1 and 2.7). In case the voltage pulse is short enough and the intermediate bias condition is zero, thermal effects can be considered negligible, since there is not enough time for the heating of the device. Therefore, a stronger similarity is expected between pulsed measurements and MC simulations without considering thermal effects. Likewise, DC measurements and MC simulations including the thermal algorithms should be similar. Figure 3.29 illustrates these conclusions. The current of the MC simulations without thermal effects is higher than that obtained considering the TRM with R_{TH} = 19.25 mm·K/W. Pulsed and DC measurements exhibit an equivalent behavior. In the pulsed experiments we have used a pulse width τ = 1 μs and period of 0.1 ms (duty cycle of 1 %). Since the reduction of current in the MC simulation has been

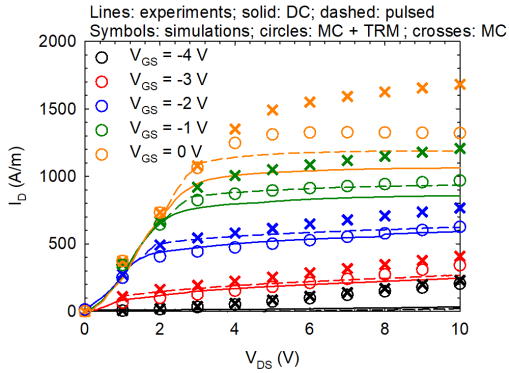

Figure 3.29: Comparison between experimental DC and pulsed ($\tau = 1$ μs, duty cycle 1 %) output characteristics, and MC output characteristics calculated considering thermal effects with the TRM ($R_{TH} = 19.25$ mm·K/W) and without considering thermal effects.

achieved by means of the concept of thermal resistance, following an inverse process we can estimate the value of the thermal resistance in our devices from the differences observed between DC and pulsed measurements, as done in next subsection 3.4.2.

3.4.2. High-temperature operation

Even though simulations of TLMs at high temperatures have been presented in subsection 3.3.1.2, as concerns electrical measurements, only 300 K results have been reported so far. The motivation of this subsection is to study experimentally the effect of increasing the operation temperature in TLMs and transistors. As mentioned in the introduction, the time frame in which this part of work was performed was towards the end of my PhD, when the cryogenic probe station (LakeShore CRX-VF) arrived to the laboratory. That is the reason why the results and their discussion are less detailed than other sections in this dissertation.

Hall measurements

As explained in subsection 3.3.1, initial Hall measurements in van der Pauw structures (see Figure 3.4) performed at IEMN allowed to obtain carrier mobility and concentration at 300 K in the wafer were TLMs and HEMTs were fabricated. Here we replicate the characterization by means of the software 8400 Series HMS of LakeShore in order to study the temperature dependence of the mentioned parameters. Figure 3.30(a) shows the obtained sheet resistivity. At low temperatures ($T < 200$ K), it is practically constant and takes a value around 150 $\Omega/\square$. At temperatures higher than 200 K, the sheet resistivity increases significantly. The opposite behavior is found in the mo-

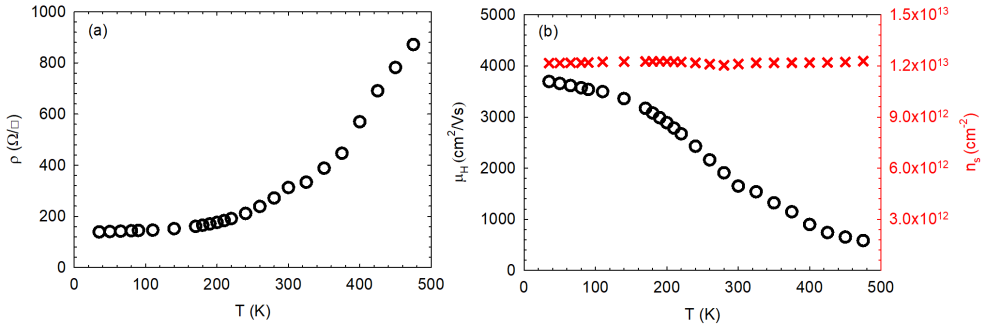

Figure 3.30: Hall measurements *vs.* temperature of (a) sheet resistivity, and (b) mobility (left axis) and sheet-carrier concentration (right axis).

bility μ_H, as illustrated in the left axis of Figure 3.30(b). At low temperatures μ_H is constant, but at higher temperatures decreases. In the right axis of Figure 3.30(b), we show the resulting sheet-carrier density n_s, which remains nearly constant and equal to $1.2{\cdot}10^{13}$ cm^{-2}, which is similar to that obtained in subsection 3.3.1.1. The small disagreement may come from the use of different reticles inside the wafer for the measurement. The constant value of n_s found in this range of temperatures indicates that the increase of resistivity with temperature is due to the decrease of mobility caused by the enhanced intensity of scattering.

TLMs

In Figure 3.14 we showed how the *I-V* characteristic of TLMs changes with the temperature considered in the simulation. Now, we can compare those results with measurements. Figures 3.31(a) and (b), for TLMs of lengths $L = 2$ μm and $L = 5$ μm, respectively, confirm the predictions of MC results. Again, the current decrease with temperature is attributed to the enhancement of scattering mechanisms, which are the main responsible of the increase of the ohmic resistance (inverse of the slope at low voltage) and the decrease of the saturation current. It is to be noted that the large discrepancy with experimental results at higher voltages (in the saturation region), is mainly due to the fact that self-heating effects are not considered in these simulations. Inclusion of the thermal models would enhance a lot the agreement (not done here due to the lack of time).

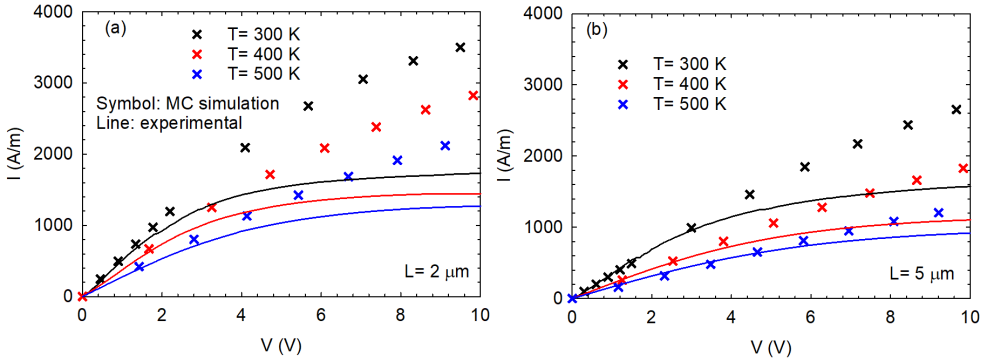

Figure 3.31: Current-voltage characteristics measured using the cryogenic probe station (LakeShore CRX-VF) and calculated from MC simulations at different ambient temperatures for TLMs of length (a) $L = 2$ μm and (b) $L = 5$ μm.

Transistors

The next step is the analysis of the performance of HEMTs measured in the temperature range 300-500 K. Figures 3.32(a) and (b) show the output characteristic for $V_{GS} = 0$ V, and the transfer characteristic and transconductance g_m for $V_{DS} = 5$ V, respectively, measured in transistor 2N ($L_G = 150$ nm, $L_{DS} = 1.5$ μm and $W = 2{\times}25$ μm) at different ambient temperatures. Again, a progressive decrease of the current can be observed for high temperatures due to the decrease of the mobility (influence of scattering mechanisms). The shift in the threshold voltage and the decrease of the transconductance at $T > 350$ K is also remarkable. We attribute this behavior to trapping effects, which could have an activation temperature slightly above 350 K.

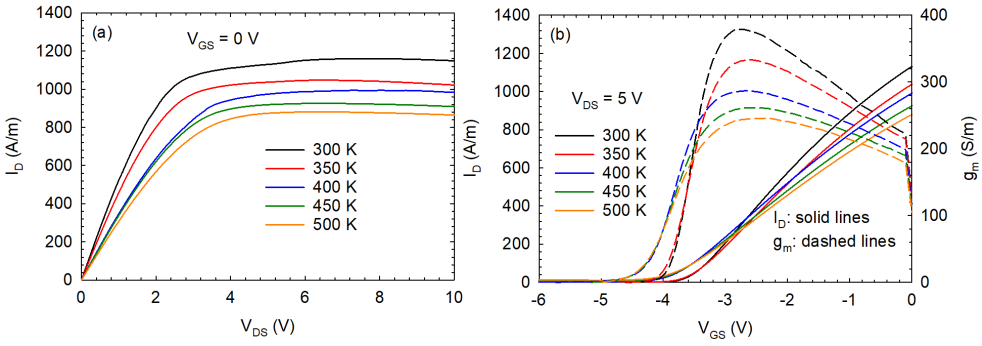

Figure 3.32: (a) Output characteristic for $V_{GS} = 0$ V, and (b) transfer characteristics (left axis) and transconductance (right axis) for $V_{DS} = 5$ V measured in transistor 2N at different ambient temperatures.

Based on the technique described in [143], it is possible to estimate the channel temperature ($T_{channel}$) by measuring DC and pulsed I-V curves as a function of temperature. According to this method, when the voltage pulse used in the measurement is narrow enough and the duty cycle is small, it can be assumed that $T_{channel} \approx T_{amb}$, the temperature of the holder in the cryogenic probe station. Therefore, when performing measurements at increasing temperatures, it is possible to correlate the decrease of I_D^{pulsed} just with the increase of the heat-sink temperature and not with any self-heating mechanism. The process consists of two steps: (i) the calibration step and (ii) the measurement step.

The calibration step is based in the study of I_D^{pulsed} *vs.* T_{amb} for a V_{DS} = 10 V corresponding to the saturation regime and V_{GS} = 0 V. We have used a pulse width of τ = 1 μs and period of 0.1 ms (duty cycle of 1 %). The slope (linear fitting) of I_D^{pulsed} *vs.* T_{amb} is called Θ, which provides information about the decrease of current per unit temperature ($\Delta T_{amb} = \Delta I_D^{pulsed}/\Theta$). Figure 3.33(a) shows the calibration curve for our transistors for T from 250 K to 500 K. A value of Θ =-1.12 A/m·K is obtained.

In the measurement step, we just compare the I-V curves measured under DC and pulsed conditions. The differences between both, observed in Figure 3.33(b), are therefore attributed only to the self-heating taking place in the DC measurements. Hence, taking into account the previous assumption for the pulsed measurements, $\Delta T_{channel} = \Delta T_{amb}$, we can attribute the decrease of the DC current respect pulsed conditions (I_D^{DC}- I_D^{pulsed}) to the difference between the heat-sink and the actual

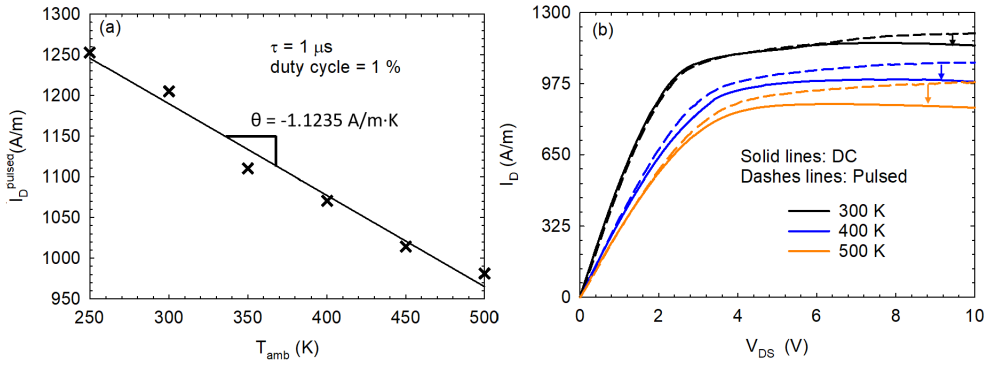

Figure 3.33: (a) I_D^{pulsed} (V_{GS} = 0 V, V_{DS} = 10 V) *vs.* T_{amb}, pulse of τ = 1 μs and duty cycle 1 % (calibration step) and (b) I_D^{DC} and I_D^{pulsed} *vs.* V_{DS} at V_{GS} = 0 V and different T_{amb} (measurement step).

channel temperature, $T_{channel} - T_{amb}$,

$$T_{channel} = T_{amb} + \frac{I_D^{DC} - I_D^{pulsed}}{\Theta}. \tag{3.16}$$

Finally, the thermal resistance R_{TH} can be estimated for each temperature just from the slope of the linear fitting $T_{channel}$ *vs.* P_{Diss} ($= I_D^{DC} \times V_{DS}$), plotted in Figure 3.34(a). Notice that the lines begin at different P_{Diss}, since the level of power at which I_D^{DC}- I_D^{pulsed} becomes significant changes with T_{amb} . Indeed, at higher T_{amb} self-heating due to the enhanced dissipation by scattering mechanisms reduces I_D^{DC} and starts having an influence at lower V_{DS}, and hence at lower P_{Diss}. Table 3.5 summarizes the values of R_{TH} so obtained at each temperature T_{amb}. At room temperature R_{TH} = 10 mm·K/W, a value lower but of the order of that used in the TRM-MC simulations (∼19 mm·K/W), coherent also with the results of the ETM-MC simulations. Table 3.5 also shows the estimated $T_{channel}$ at V_{DS} = 10 V with the associated P_{Diss}, evidencing the difference between the temperatures of the heat-sink and the hotspot in the channel, which, as expected, increases with T_{amb}.

We compare the R_{TH} obtained from $T_{channel}$ and P_{Diss} at V_{DS} = 10 V by means of Equation 1.30, with the results obtained from the explained method [see Figure 3.34(b)]. Although the R_{TH} obtained at V_{DS} = 10 V is smaller than that used in the simulations, it shows the expected behavior, increasing with the ambient temperature. On the other hand, the R_{TH} at T = 400 K obtained with the described method is clearly smaller than the expected value. The origin of the discrepancies between the obtained results and the expected increasing trend with T_{amb} could be related with two factors, the pulse width and the maximum voltage bias. Reducing the pulse width could also reduce more the impact of self-heating, that could be still

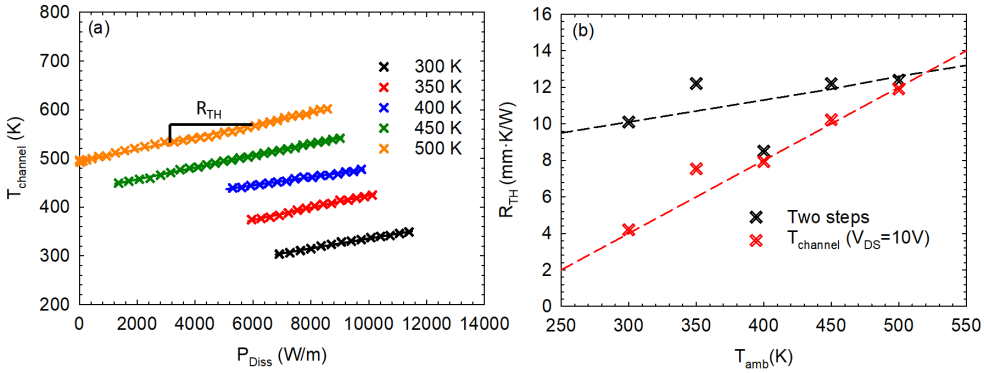

Figure 3.34: (a) $T_{channel}$ *vs.* P_{Diss} for each heat-sink temperature T_{amb}. (b) Comparison between R_{TH} calculated with the described method (black symbols) and calculated with $T_{channel}$ and P_{Diss} at V_{DS} = 10 V. Dashed lines are an eye-guide to observe the trends.

T_{amb} (K)	R_{TH} (mm·K/W)	$T_{channel}$ (K) - P_{Diss} (W/m) (V_{DS} = 10 V)
300	10.1	349 - 11496
350	12.2	427 - 10219
400	8.5	478 - 9833
450	12.2	543 - 9090
500	12.4	603 - 8649

Table 3.5: Experimental R_{TH} at different T_{amb}, and $T_{channel}$ estimated with P_{Diss} at V_{DS} = 10 V.

present in the measurement. Moreover the influence of the self-heating on the *I-V* curve is much more significant at higher temperatures. Therefore, we should increase V_{DS} to observe an enhanced effect of self-heating at every T_{amb}, which could allow a more accurate estimation of R_{TH}.

Chapter 4

Microwave Characterization of HEMTs

In the previous chapter, we have studied the DC performance of HEMTs and the influence of temperature on the current-voltage characteristics. However, HEMTs were developed in the search of faster devices for high-frequency applications, one of the main objectives of modern electronics, and, in the case of GaN, also for high-power applications. Therefore, the AC characterization of HEMTs is mandatory. Small-signal modeling is a common analysis technique that approximates the (nonlinear) behavior of electronic devices at each bias point by means of linear equations, making use of the so called Small-Signal Equivalent Circuit (SSEC), introduced in section 1.3. This type of analysis can be performed both from experimental and physical modeling points of view. Concerning experimental characterization at RF frequencies, a Vector Network Analyzer (VNA) is the most suitable equipment. On the other hand, in connection with modeling, MC simulations are a very appropriate tool to study the AC behavior of the devices by means of the procedure explained in subsection 1.3.2. The equivalent circuits have been used by researchers since the first models were proposed [144, 145], to understand the physics of the devices, compare the performance between different technologies and model the device behavior in electronic design programs. Apart from applications like amplification, based on the linear behavior of the devices modeled by means of the SSEC, other applications exploiting the nonlinearities present in their response are also quite relevant, like RF signal detection, as reported in section 2.3 of chapter 2 for the case of SSDs.

In this chapter, the SSEC of our GaN HEMTs will be experimentally extracted from the measured S-parameters in section 4.1. We analyze the anomalous behavior exhibited by the S-parameters when transistors are measured for the first time, which we attribute to trapping effects. Then, we study the influence of self-heating, whose relevance in the DC regime was already stressed in subsection 3.3.2. In particular, by means of MC simulations, we analyze the effect of temperature and self-heating on the parameters of the SSEC. Finally, in the last part of the Chapter (section 4.2), the capability of the HEMT for the detection of microwave signals will be studied. The differences between RF gate- and drain-coupling schemes will be analyzed, as well as their possible frequency limits.

4.1. Small-signal equivalent circuit

The different models of SSECs in HEMTs and the methods to obtain the elements of the circuit can be found in [144, 145]. In this section, the technique we use to extract the parameters of the equivalent circuit is described. To this end, we measure the S-parameters in the frequency range covered by our VNA (from 10 MHz to 43.5 GHz). The models of the equivalent circuit usually consider only the intrinsic parameters, which are bias dependent, but in the measurement the accesses of the device are also present. Therefore, they have also to be modeled in the equivalent circuit by means of the so-called extrinsic parameters, which do not depend on bias.

4.1.1. Extrinsic parameters

There are several methods to extract the extrinsic parameters, from impedance (Z) or admittance (Y) parameters, depending on the topology of the equivalent circuit [146], usually called Π or T. However, those methods, developed for MESFETs, need for biasing the device in extreme conditions, which can deteriorate the performance in the case of GaN HEMTs. An alternative to estimate a small-signal equivalent circuit for the extrinsic elements is to measure the S-parameters of the dummies available in the wafer [147], taking the effects of the series parasitics into account. A dummy is not a calibration standard, it is a dedicated structure fabricated in the wafer to measure the impact of the pads in the RF response. In this work we use two type of dummies, open circuit and short circuit. In Figure 4.1, both type of dummies are shown. In an open circuit there is no connection between source, drain and gate pads and therefore it presets an impedance close to the right limit of the Smith chart for both gate and drain ports, while a short circuit connects source, drain and gate pads and therefore it presents an impedance close to the left limit of the Smith chart for both drain and

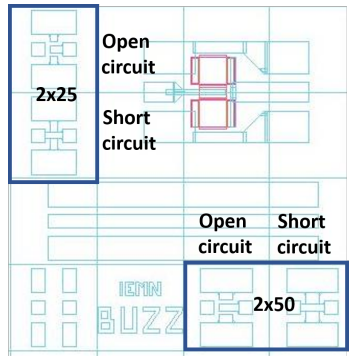

Figure 4.1: Open and short circuit dummies: widths 2×25 μm and 2×50 μm.

gate ports. The wafer has two device widths (2×25 μm and 2×50 μm) to make possible the determination of the parasitics in each geometry.

In Figures 4.2(a) and (b), the proposed equivalent circuits for the dummies are shown. In the open circuit, the coupling between the gate or drain and source pads is modeled with the capacitors C_{pg}, C_{pd} and C_{pd2} (for the narrowest part of the gate contact) and the resistances R_{pg} and R_{pd}, while the parameters with sub-index *acop*, R_{acop} and C_{acop}, model the crosstalk between the gate and drain of the device. On the other hand, the short circuit has the same coupling between gate or drain and source, thus represented by the same elements in the model (C_{pg}, C_{pd}, R_{pg} and R_{pd}), but the gate and drain pads are now connected, and also with the source pad. In order to model these lines we use inductances: L_1 and L_2 for the gate-to-drain line and L_p for the gate(drain)-to-source line.

Since the proposed equivalent circuit for the open-circuit dummy exhibits a Π topology, the adequate parameters to work with are the admittance parameters (Y).

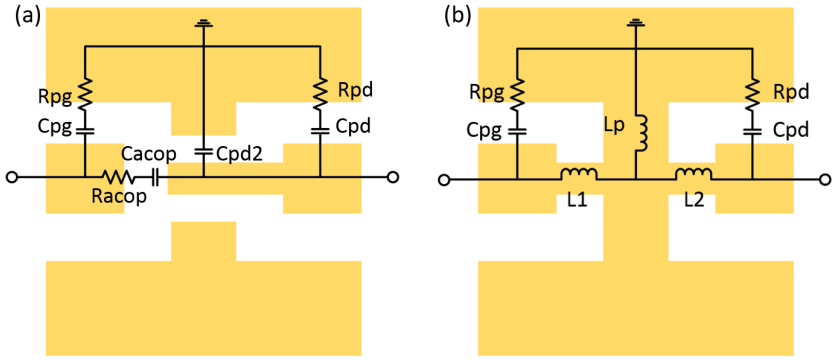

Figure 4.2: Equivalent circuit for the dummies: (a) open and (b) short circuit.

However, the VNA measures the S-parameters, which are converted to Y-parameters using the equations in [84] for a matched case,

$$Y_{11} = (1/50)\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}, \tag{4.1}$$

$$Y_{12} = (1/50)\frac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}, \tag{4.2}$$

$$Y_{21} = (1/50)\frac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}, \tag{4.3}$$

$$Y_{22} = (1/50)\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}}. \tag{4.4}$$

The numeric values of the Equations 4.1-4.4 are obtained with the software Quite Universal Circuit Simulator (Qucs) [148], an open source code used for the simulations of electrical circuits. This software also allows for the optimization of the elements of the circuit to reproduce the measured Y-parameters of the dummies. Therefore, by comparing the measurements of the dummies with the proposed model of equivalent circuit, we can extract the values of the extrinsic elements.

In Figure 4.3, the comparison between the experimental and modeled (a) Y_{11} and (b) Y_{22} parameters is shown for an open circuit. As observed, Y_{11} takes higher values, which can be explained in terms of the topology of the proposed equivalent circuit. In port 1 (gate) the circuit has just R_{pg} in series with C_{pg}, while in port 2 (drain) the series connection of R_{pd} and C_{pd} is in parallel with C_{pd2} to model the wider and narrower part of the drain pad, respectively. This asymmetry in the equivalent circuit (due to the asymmetry of the topology) is the reason for the differences between Y_{11} and Y_{22}.

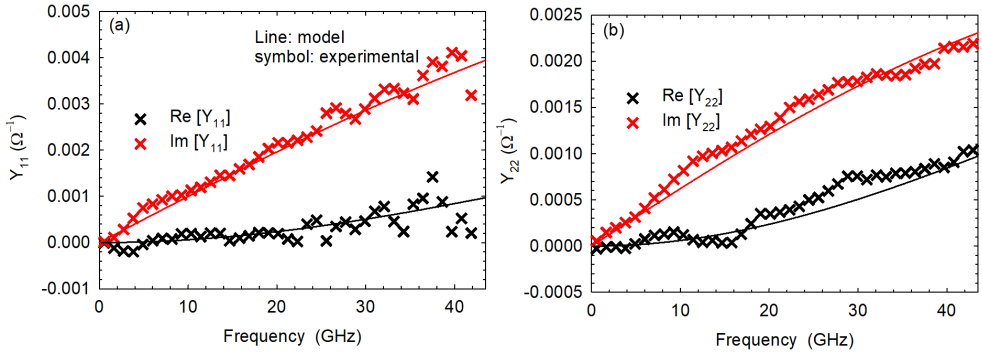

Figure 4.3: $\Re$[Y] and $\Im$[Y] for (a) Y_{11} and (b) Y_{22} in the open circuit. Symbols represent the experimental data and solid lines the model of the equivalent circuit.

In Figures 4.4(a) and (b), Y_{21} and Y_{12} (measured and modeled), respectively are plotted. These parameters are related to R_{acop} and C_{acop}, which represent the coupling between ports 1 (gate) and 2 (drain). Therefore, they should verify the condition $Y_{12} = Y_{21}$, which, as observed, is quite satisfactorily fulfilled by measurements. The resistance R_{acop} is considered in the model to reproduce the non-zero real part of Y_{21} and Y_{12}, while the capacity C_{acop} accounts for the frequency dependence of $\Im[Y_{21}]$ and $\Im[Y_{12}]$. An overall good agreement between measurements and values provided by the equivalent circuit is observed for the four Y-parameters, what supports the validity of the proposed equivalent circuit.

The topology of the equivalent circuit proposed for the short-circuit dummy corresponds to a T configuration due to the symmetry around the vertical axis, so that the adequate parameters for its analysis are the impedance parameters (Z). Therefore, like in the open circuit dummy, we measure the S-parameters and convert them to the adequate parameters (Z in this case) in order to fit the model and reproduce the experimental results. In a matched case the equations are [84]:

$$Z_{11} = 50\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}, \tag{4.5}$$

$$Z_{12} = 50\frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}, \tag{4.6}$$

$$Z_{21} = 50\frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}, \tag{4.7}$$

$$Z_{22} = 50\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}}. \tag{4.8}$$

Z_{11} and Z_{22} parameters are plotted as obtained from experimental measurements and the equivalent circuit in Figures 4.5(a) and (b), respectively. Impedance parameters Z_{11} and Z_{22} are quite similar due to the symmetry of the pad, which in this

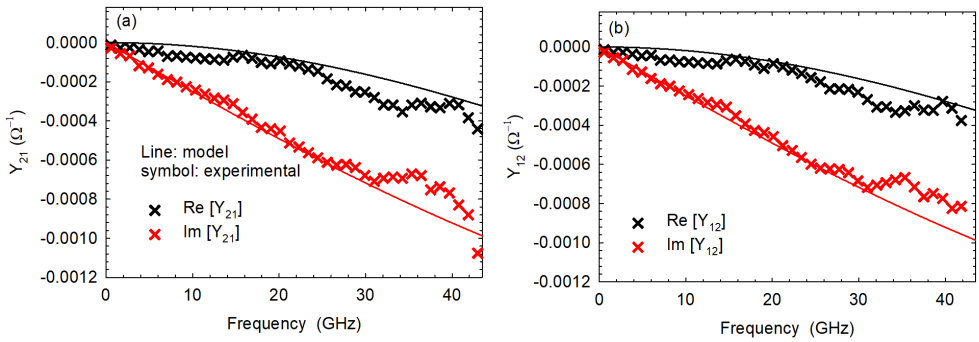

Figure 4.4: $\Re[Y]$ and $\Im[Y]$ for (a) Y_{21} and (b) Y_{12} in the open circuit. Symbols represent the experimental data and solid lines the model of the equivalent circuit.

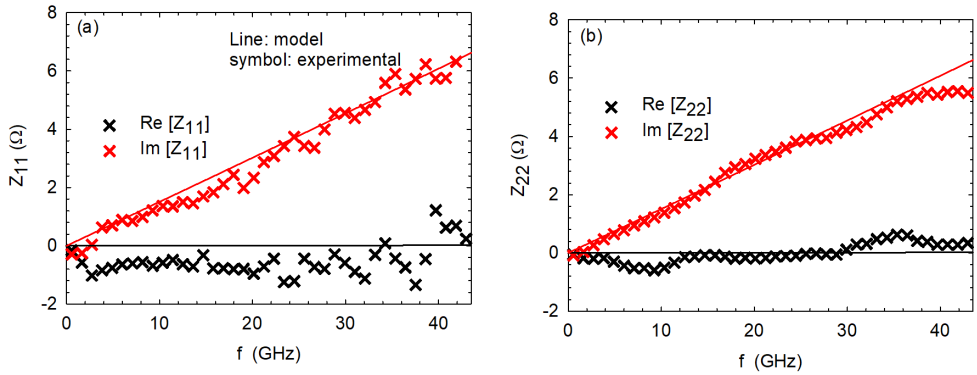

Figure 4.5: $\Re$[Z] and $\Im$[Z] for (a) Z_{11} and (b) Z_{22} in the short circuit. Symbols represent experimental data and solid lines the model of equivalent circuit.

dummy does not exhibit differences between ports. In the short-circuit model we maintain R_{pd} in series with C_{pd} in port 1 and R_{pg} in series with C_{pg} in port 2, since the geometry is the same as in the open. Moreover, due to the symmetry of the pad and the configuration of the circuit, the mentioned elements should be the same in both ports, as the experimental results of Z_{11} and Z_{22} confirm by the fact that $Z_{11} \approx Z_{22}$.

Regarding impedance parameters Z_{21} and Z_{12}, they are shown in Figures 4.6(a) and (b), respectively. In these parameters, the vertical symmetry of the pads is also evidenced, because the distance from the gate and drain pads to the central short-circuit with the source pads is the same. Therefore $Z_{12} = Z_{21}$, like in the case of Z_{11} and Z_{22}. This relationship between the parameters is different from that found in the Y parameters of the open, where $Y_{12} = Y_{21}$ but $Y_{11} \neq Y_{22}$. However, the actual pad

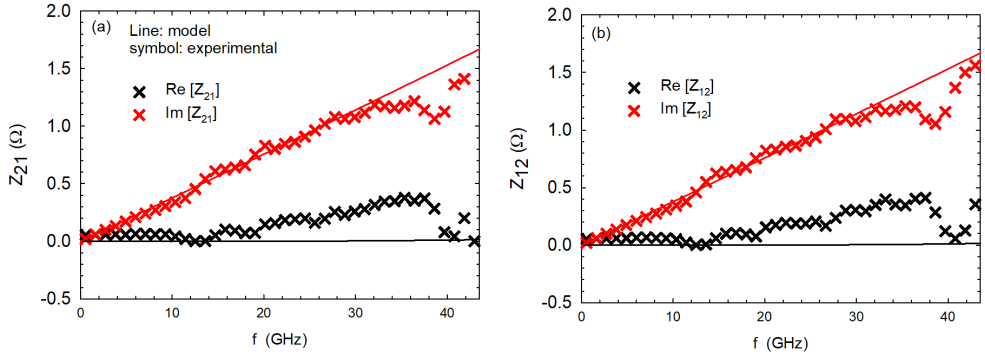

Figure 4.6: $\Re$[Z] and $\Im$[Z] for (a) Z_{21} and (b) Z_{12} in the short circuit. Symbols represent experimental data the solid lines the model of equivalent circuit.

W	2×25 μm		2×50 μm	
Dummy	open	short	open	short
$R_{pg,d}$	300 Ω	300 Ω	300 Ω	300 Ω
$C_{pg,d}$	6 fF	6 fF	6 fF	6 fF
C_{pd2}	6 fF	-	12 fF	-
R_{acop}	300 Ω	-	300 Ω	-
C_{acop}	4 fF	-	4 fF	-
$L_{1,2}$	-	18 pH	-	18 pH
L_p	-	6 pH	-	6 pH

Table 4.1: Extrinsic elements obtained from the measurements, extracted with the software Qucs according to the proposed equivalent circuits.

of the HEMTs is more similar to the open dummy and this is something to take into account. In Table 4.1, the values of the parameters of the equivalent circuit of the dummies are provided for both widths, $W = 2 \times 25$ μm and $W = 2 \times 50$ μm. The results evidence the symmetries of the pads, like the elements $C_{pg,d}$ or $R_{pg,d}$, which are independent of the type of dummy and the width, because they are just related to the gate and drain pads. As expected, the element that depends more on the width is C_{pd2}, because the surface of influence is higher due to the longer pad since its value is doubled for $W = 2 \times 50$ μm with respect to $W = 2 \times 25$ μm

The actual gate pad, by including the accesses to the gate contacts, is slightly different from that of the open circuit dummy. In Figure 4.7, a picture of the proposed equivalent circuit is shown. Some of the parameters are similar to those of the open circuit, like $R_{pg,d}$, $C_{pg,d}$, C_{acop}, R_{acop} and $L_{1,2}$. However, the element L_s should be different from L_p, because the actual pad of the device is shorter than that of the short-circuit dummy; we estimate $L_s = 2/3\ L_p$ according to the shape. Moreover, we include other parameters in the access to the device, which are related with the contacts: gate resistance (R_g), source resistance (R_s) and drain resistance (R_d). R_d and R_s are the contact resistances extracted from the measurements of the TLMs (see subsection 3.3.1.1), which we estimate around 2.5 Ω for a width of 100 μm. Therefore, for $W = 2 \times 25$ μm, $R_{d,s} = 5$ Ω, while for $W = 2 \times 50$ μm, $R_{d,s} = 2.5$ Ω. For R_g, we can suppose two conductive wires in parallel, and we use the following analytic expression to estimate its value [149]

$$R_g = \frac{W\rho}{nL_G h}, \tag{4.9}$$

where W is the width of the device, ρ is the resistivity of the material (mainly gold, with $\rho = 2.271 \cdot 10^{-8}$ Ω · m), n the number of fingers, L_G the gate length and h the

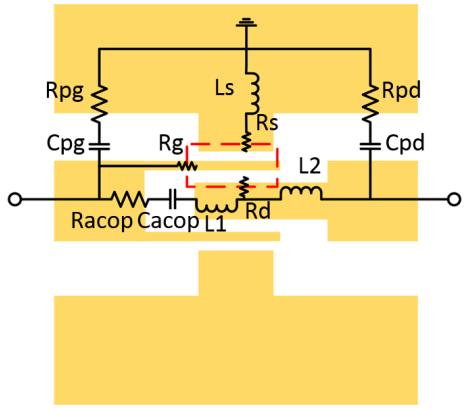

Figure 4.7: Actual pads of the HEMTs with the proposed equivalent circuit. The red square indicates the region corresponding to the device.

thickness of the gold layer ($h = 400$ nm). We have two gate fingers in parallel and we will analyze four devices with different values of W and L_g. For $W = 2 \times 25$ μm, with $L_G = 150$ nm we have $R_g = 1.5$ Ω and with $L_g = 75$ nm we have $R_g = 3$ Ω; while for $W = 2 \times 50$ μm, with $L_G = 150$ nm we have $R_g = 3$ Ω and with $L_g = 75$ nm we have $R_g = 6$ Ω.

4.1.2. Intrinsic parameters

Once the effect of the pads (extrinsic parameters) has been characterized and it is possible to remove it from the measurements, in this subsection, we extract the Small-Signal Equivalent Circuit (SSEC) of the HEMTs. A first model of an equivalent circuit is proposed in [144]. However, the most accepted is the one reported in [146]. This model has a resistance in series with a capacitance in the gate-to-source region, a capacitance in the gate-to-drain-region and a source of current in parallel with a resistance and a capacitance in the drain-to-source region. In [150], the authors propose some improvements, like the extraction of the extrinsic elements explained in subsection 4.1.1 or the inclusion of a resistance R_{gd} in the gate-to-drain region in order to account for a nonzero real part of Y_{12}. The better fitting of the Y-parameters achieved with this model also improves the model-to-measurement agreement of quantities like the maximum available gain (MAG) and the maximum stable gain (MSG). There are more models including distributed equivalent circuits, with more precision, but much more complex. In this work, the model of Figure 4.8 is considered.

The elements of the equivalent circuit are related with the physics of the device. C_{gd} and C_{gs} represent the effect of the depletion region under the gate. C_{ds} is asso-

ciated with carriers reaching the substrate. R_{gs} (or R_i) represents the ohmic region between gate and source. The resistance associated with the channel is R_{ds} (or g_d in terms of conductance). R_{gd} and R_i affect the times of charge and discharge of capacitors. The model also includes the transconductance g_m, which represents the control that the gate has on the current level between source and drain. Actually, this parameter can be expressed as function of frequency as

$$g_m = g_{m_0} e^{-j\omega\tau}, \tag{4.10}$$

where g_{m_0} is the static transconductance and τ the transit time.

In order to extract the elements of the equivalent circuit, we measure the S-parameters with the VNA from 10 MHz to 43.5 GHz. However, the SSEC elements are usually related to admittance parameters (Y) due to the topology of the equivalent circuit proposed for the HEMT, which is Π-type. Therefore, we start by de-embedding the extrinsic elements from the measured S-parameters to obtain the intrinsic S-parameters, which are then converted into Y-parameters using the equations in [84]. Finally, the so-obtained intrinsic Y-parameters can be expressed as a function of the elements of the equivalent circuit as [151]

$$Y_{11} = \frac{j\omega C_{gs}}{1 + j\omega C_{gs} R_i} + \frac{j\omega C_{gd}}{1 + j\omega C_{gd} R_{gd}}, \tag{4.11}$$

$$Y_{12} = -\frac{j\omega C_{gd}}{1 + j\omega C_{gd} R_{gd}}, \tag{4.12}$$

$$Y_{21} = -\frac{j\omega C_{gd}}{1 + j\omega C_{gd} R_{gd}} + \frac{g_{m_0} e^{-j\omega\tau}}{1 + j\omega C_{gs} R_i}, \tag{4.13}$$

$$Y_{22} = \frac{j\omega C_{gd}}{1 + j\omega C_{gd} R_{gd}} + j\omega C_{ds} + \frac{1}{R_{ds}}; \tag{4.14}$$

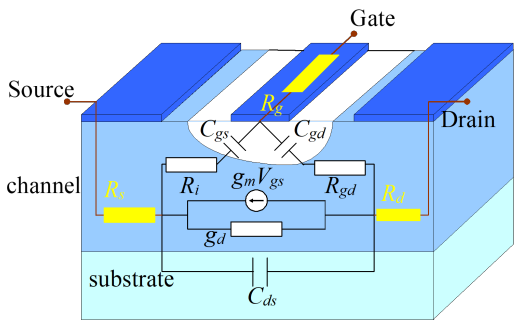

Figure 4.8: Scheme of the device with the proposed equivalent circuit according to [150].

and from these equations the SSEC elements can be expressed as [152]

$$C_{gd} = \frac{1}{\omega \Im(Y_{12}^{-1})}, \tag{4.15}$$

$$C_{gs} = \frac{-1}{\omega \Im(\frac{1}{Y_{11}+Y_{12}})}, \tag{4.16}$$

$$C_{ds} = \frac{\Im(Y_{12}+Y_{22})}{\omega}, \tag{4.17}$$

$$R_i = \Re\left(\frac{1}{Y_{11}+Y_{12}}\right), \tag{4.18}$$

$$R_{ds} = \frac{1}{\Re(Y_{12}+Y_{22})}, \tag{4.19}$$

$$R_{gd} = -\Re\left(\frac{1}{Y_{12}}\right), \tag{4.20}$$

$$g_{m_0} = \left|\frac{(Y_{12}-Y_{21})(Y_{11}+Y_{12})}{\Im(Y_{11}+Y_{12})}\right|, \tag{4.21}$$

$$\tau = \frac{\pi/2 - phase(Y_{12}-Y_{21}) + phase(Y_{11}+Y_{12})}{\omega}. \tag{4.22}$$

In the small-signal regime, for a given bias point, the parameters of Equations 4.15 to 4.22 should be constant, i.e., frequency independent. The values of the parameters are directly extracted from the equations by means of the use of the software Qucs. The advantage of using this software is its optimization algorithm [153], which fits the values of the SSEC elements by comparison with the experimental measurements of the S-parameters.

4.1.2.1. Dispersion effects

In this subsection we will show and discuss the results of the RF experimental characterization of the HEMTs. We will study a transistor whose dimensions are L_G = 150 nm, L_{DS} = 2.5 μm and $W = 2 \times 25$ μm, corresponding to the transistor named 6N in Table 3.2. The output and transfer characteristics of this HEMT are shown in Figures 4.9(a) and (b), respectively. As already mentioned, the intrinsic elements of the equivalent circuit depend on the bias conditions. We have chosen V_{GS} =-2.5 V and V_{DS} = 1.5 V,[10] a bias point with a low value of V_{DS}, which we will call Q-point (quiescent point, indicated in the figures with a red star).

During the DC characterization of our transistors, we surprisingly noticed that the levels of current changed from the very first measurement to subsequent ones.

[10] In this subsection we only study experimental results, therefore we will not distinguish between internal and external voltages.

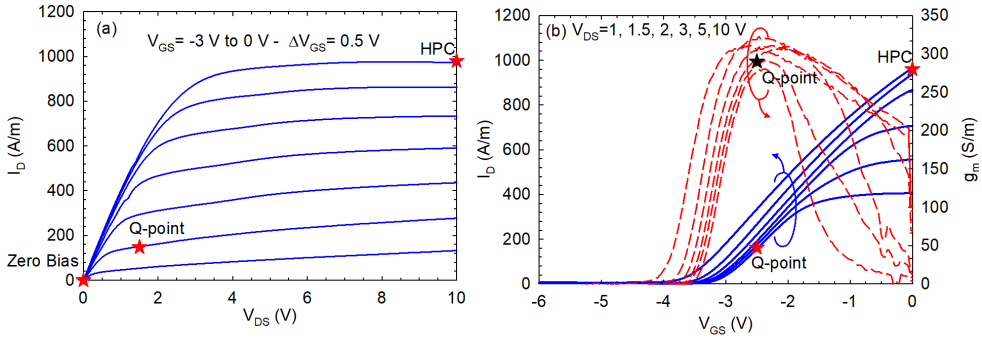

Figure 4.9: (a) Output and (b) transfer characteristics (left axis) and transconductance (right axis) of transistor 6N (L_G = 150 nm, L_{DS} = 2.5 μm and W = 2 × 25 μm). The relevant operation bias points are indicated with red stars.

Additionally, when we measure a virgin device (non-previously measured) in RF, we find that S_{21} and S_{22} show unnatural shapes at low frequencies, with a pronounced hump in S_{22} and an anomalous decrease and phase change in S_{21}. However, those effects are later mitigated after applying bias conditions corresponding to open channel and high current, called High-Power Conditions (HPC, as indicated in the I-V curves of Figure 4.9). The initial Q-point was chosen not to mitigate the observed effects. The intrinsic S-parameters (after de-embedding the effect of the extrinsic elements from the raw measurements) measured in the Q-point before and after HPC are shown in Figure 4.10, where the anomalous behavior of the S-parameters before HPC previously described can be observed. The lower values of frequency are in the axis.

Using Equations 4.15-4.22, we can extract the frequency behavior of the elements of the model in both measurements, before and after HPC. In particular, the elements more affected by S_{21} and S_{22} are g_{m_0} and R_{ds}, which show a remarkable frequency dispersion. In Figure 4.11 we show (a) g'_{m_0} and (b) R'_{ds}.[11] We call them apparent elements, because they are defined as constant assuming a standard small-signal equivalent circuit (S-SSEC), but they actually show dispersion in frequency. Before applying HPC, when the dispersive mechanism is particularly significant, both S_{21} and S_{22} show a prominent hump at low frequencies, which translates into a lower value of g'_{m_0} and a higher value of R'_{ds} (with a factor of two between both scenarios). This indicates that the S-SSEC is not the valid model in these conditions and some modification must be introduced to reproduce experiments. After HPC, the dispersion is mitigated and the cutoff frequency observed in both elements shifts to higher values of frequency.

[11] By adding the apostrophe, we denote them as apparent transconductance and resistance.

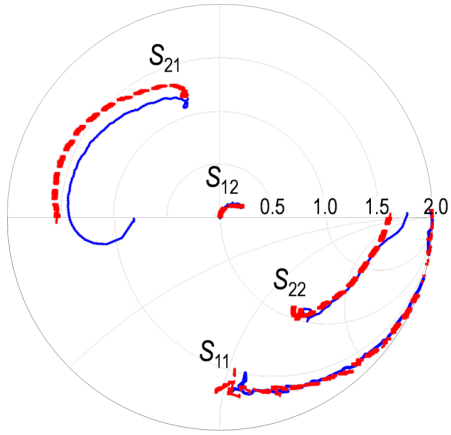

Figure 4.10: Intrinsic S-parameters extracted from the measurements at Q-point (V_{GS} =-2.5 V and V_{DS} = 1.5 V), before HPC in blue solid line and after HPC in dashed red line. S_{11} and S_{22} are plotted in a Smith Chart format, S_{21} and S_{12} are represented in polar format with a maximum scale of 2.0. Frequency from 10 MHz to 43.5 GHz.

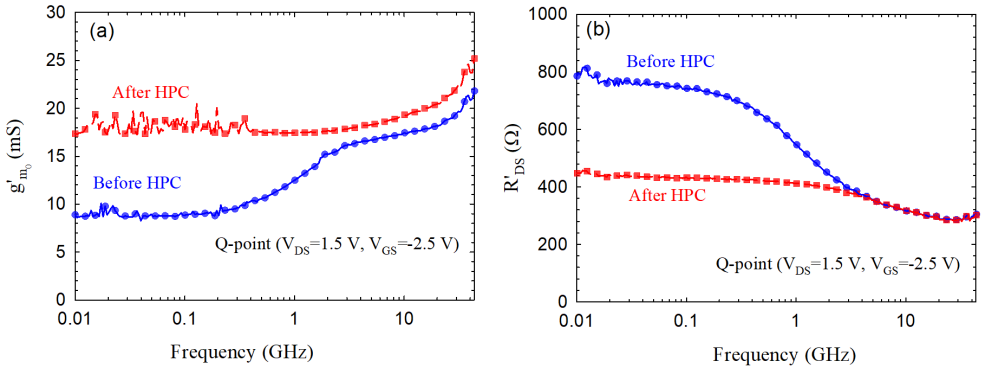

Figure 4.11: Apparent (a) transconductance and (b) drain-to-source resistance of the S-SSEC calculated at the Q-point before and after HPC.

In order to understand better the dispersion in these devices, we have measured the S-parameters of the transistors, starting from a non-previously measured reticle, performing a systematic process where the transistor is biased in each state for a period of several seconds, in which the S-parameters are extracted. The protocol for the RF measurements involves the following bias conditions (in chronological order):

1. Virgin device at zero bias (V_{GS} = 0 V and V_{DS} = 0 V).
2. Q-point (V_{GS} = -2.5V and V_{DS} = 1.5 V).
3. Zero bias (V_{GS} = 0 V and V_{DS} = 0 V).
4. HPC (V_{GS} = 0 V and V_{DS} = 10 V).

5. Zero bias (V_{GS} = 0 V and V_{DS} = 0 V).
6. Q-point (V_{GS} = -2.5 V and V_{DS} = 1.5 V).

In the protocol, we measure three times the S-parameters at zero bias. From these parameters, we can extract the drain-to-source impedance (Z_D): for the unstressed HEMT (step 1), after Q-point (step 3) and after HPC (step 5). In Figure 4.12, Z_D is plotted in these three conditions. Without any previous bias excitation, the virgin device shows a prominent increase of the impedance at low frequency, with values in excess of 1 kΩ. After biasing the device at the Q-point, the zero-bias impedance at low frequencies is reduced by more than one order of magnitude. A further reduction of Z_D is observed after applying HPC, while the transition from high to low resistance shifts to higher frequencies, as it was observed in R'_{ds} and g'_{m_0}. At frequencies higher than 2-3 GHz there are not significant differences in the values of the impedance. It must be noted that this process seems to be irreversible, since the state induced in the device at zero bias after applying a given bias condition is stable in the very long term (at least some weeks according to our tests).

The described anomalous behavior is attributed to the presence of some kind of trapping states (which are common in AlGaN/GaN devices [21]) within or in the vicinity of the channel, whose negative charge is able to decrease the electron concentration in the 2DEG, thus producing a substantial increase of the impedance of the HEMTs. Traps located in the ohmic contact regions could also provide a significant contribution to the observed evolution of the device resistance. Furthermore, the phenomenon is present up to a given cutoff frequency, which may be directly related to the characteristic times of these traps (much faster than those originating the typical drain and gate lag effects in GaN HEMTs). Biasing the device seems to force a de-trapping (or even trap-suppression) mechanism, more significant the stronger the bias conditions are. The fact that the cutoff frequency shifts to higher values indicates that mainly the slowest of these traps are affected by the bias.

As already mentioned, the observed frequency dispersion in Z_D, R'_{ds} and g'_{m_0} indicates that the S-SSEC is not the correct model to characterize these effects. Discrepancies between the drain conductance obtained from DC measurements and that measured at microwave frequencies have been found in different transistor technologies, and its frequency dependence has been traditionally modeled by incorporating a series RC branch to the intrinsic equivalent circuit model (connecting drain and source contacts, in parallel with the drain conductance, drain-to-source capacitance and transconductance branches [154]). From this type of model, it is possible to calculate a characteristic frequency given by $1/2\pi RC$, which determines the transition between the higher drain resistance at lower frequencies, and the lower drain resistance at higher frequencies.

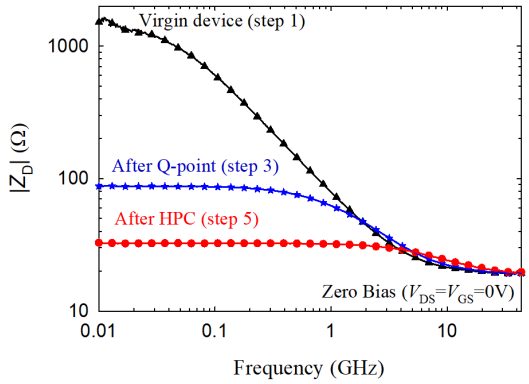

Figure 4.12: Magnitude of the drain-to-source impedance (Z_D) of the virgin device (step 1), after biasing it at the Q-point (step 3) and HPC (step 5), measured at zero bias ($V_{GS} = 0$ V and $V_{DS} = 0$ V).

Given that the frequency dispersive behavior observed in $R_{ds}^{'}$ is often accompanied by a frequency dependent value of $g_{m_0}^{'}$, both with the same characteristic frequency, successive works [155, 156] have proposed improved models that include an additional current source in parallel with the resistance of the RC branch. In such models, apart from the fact that the frequency dispersion on $R_{ds}^{'}$ and $g_{m_0}^{'}$ is modeled separately by adding an extra resistance and a current source respectively, the use of two current sources in parallel, between the drain and source contacts, may lead to the erroneous idea of multiple channels or signal paths within the real device structure. Furthermore, even if being able to reproduce the experimental measurements, the circuit module proposed to model the dispersive effects acts counterintuitively from a physical point of view, since it has no influence at low frequency, which is where trap-related dispersive effects manifest. Indeed, the added branch is blocked by the capacitor at low frequency, while it is at high frequency where both the resistor and the current source have effect on the circuit performance.

In order to model the observed frequency dispersion, we propose a modified small-signal equivalent circuit (T-SSEC) with a parallel RC tank. Figure 4.13 shows the modified equivalent circuit with the RC tank (R_T and C_T) incorporated to the S-SSEC model for FETs, placed in series with the conventional drain-to-source branch, without the need to add any additional current source.

This additional RC tank represents more faithfully the physics of the interaction of the current flow with the trapping effects within or close to the channel (and the ohmic contact regions, if it is the case). It produces an increase of the output resistance at low frequencies due to the resistor R_T, and has no effect at higher frequencies when the

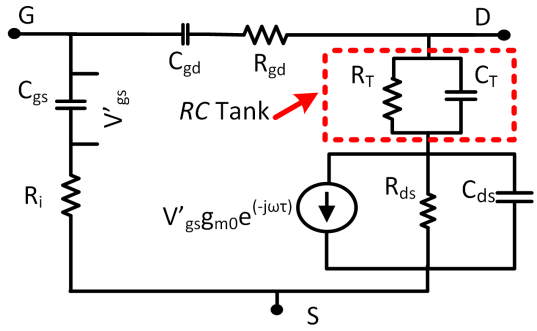

Figure 4.13: Proposed model (T-SSEC) including an RC tank into the S-SSEC to reproduce the observed frequency dispersion .

signal is bypassed by C_T. Despite its simplicity, this model is also able to reproduce the drop of g'_{m_0}, since the current source sees R_T in series with the drain current path. In addition, this T-SSEC easily allows decoupling the effect of the traps from the general small-signal model. In the case of working above the characteristic frequency of the traps, the device performance can simply be reproduced by eliminating the RC tank ($R_T = C_T = 0$) and using the S-SSEC model, keeping the same values for the rest of elements.

S-SSEC and T-SSEC models have been implemented in Qucs with the optimization algorithm. For the sake of comparison, the results obtained with the two models of equivalent circuit at the Q-point before HPC are plotted in Figure 4.14. The fitting obtained with the S-SSEC model (i.e., without R_T and C_T) is shown in Figure 4.14(a), evidencing that the standard model is able to reproduce the measured S-parameters only at high frequencies.

In contrast, the results obtained with the proposed T-SSEC model, shown in Figure 4.14(b), successfully reproduce the device performance in all the frequency range (including the low-frequency deviations in S_{22} and S_{21}). In this second case, all the common elements of both SSECs are kept with the same values (except for g_{m_0}, which is slightly increased), and the additional R_T and C_T have been optimized to properly reproduce the device response at low frequencies. In particular, as observed in the inset of Figure 4.14(b), they fit rather well the dispersion of the apparent R'_{ds} and g'_{m_0} parameters. The obtained values of $R_T = 380\ \Omega$ and $C_T = 550$ fF allow us to have an estimation of the characteristic frequency of the traps, which in this case corresponds to $f_T \approx 800$ MHz.

As it was shown in Figure 4.11 for the apparent R'_{ds} and g'_{m_0} parameters, the low frequency dispersion can be strongly suppressed when a high current passes through

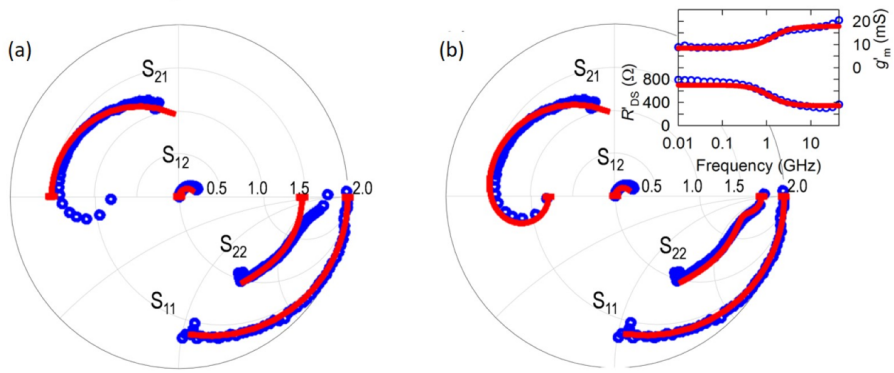

Figure 4.14: Intrinsic S-parameters extracted from the measurements (blue symbols) at Q-point (V_{DS} = 1.5 V, V_{GS} =-2.5 V) before HPC, and model fitting (red lines) using: (a) the S-SSEC and (b) the proposed T-SSEC. The inset shows the apparent $R_{ds}^{'}$ and $g_m^{'}$ parameters extracted from the S-parameters obtained from the T-SSEC (red line) and the measurements (blue symbols). Parameters S_{11} and S_{22} are represented in Smith chart format, and S_{21} and S_{12} are represented in polar format with a maximum scale of 2.0.

the channel (HPC), which presumably empties (or suppresses) in a long time scale the trapping states responsible of the anomalous frequency dependence. In this second scenario, the traps have a much lower effect, so that the value of R_T to be used in the T-SSEC is much lower, 100 Ω, and C_T is also smaller, 240 fF. This is shown in Figure 4.15, where the results of the T-SSEC model are compared with the intrinsic S-parameters measured at the Q-point after applying HPC. As observed, the dispersion in frequency has been nearly suppressed. The reduction of R_T and C_T provides a higher value of the characteristic frequency of the traps ($f_T \approx 6.5$ GHz), consistent with the shift to higher frequency of the dispersive effects after HPC already observed in the drain-to-source impedance (Figure 4.12).

In Table 4.2, the values of the elements of the equivalent circuit extracted with the S-SSEC and T-SSEC models at the Q-point before and after HPC are summarized. The more significant differences are observed in g_m, which is the parameter more closely related with the current level. R_{ds} is very similar in every condition, because the additional resistance included in the apparent $R_{ds}^{'}$ is given by R_T. At low frequencies, the equivalent circuit in the drain-to-source branch behaves as two resistances in series, $R_{ds} + R_T$. But at frequencies higher than the cutoff of dispersive effects, this branch behaves as just one resistance, R_{ds}. Moreover, after HPC, g_m is higher, which is consistent with the higher DC current measured in the device.

Based on the previous results, we propose two possible interpretations of the dispersive behavior found in the virgin devices in terms of additional traps or de-

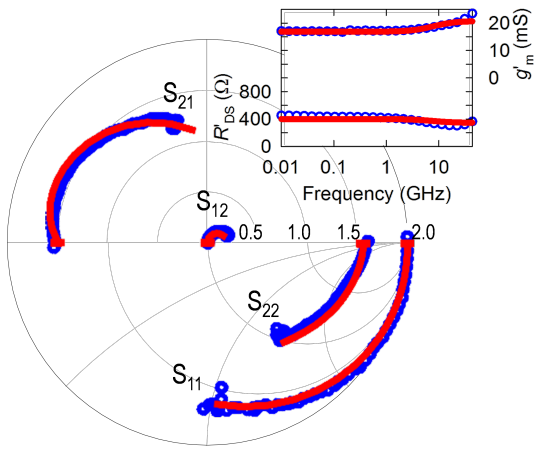

Figure 4.15: Intrinsic S-parameters extracted from the measurements (blue symbols) at Q-point (V_{DS} = 1.5 V, V_{GS} =-2.5 V) after HPC, and model fitting (red line) using the proposed T-SSEC. The inset shows the apparent R'_{ds} and g'_m parameters extracted from the S-parameters obtained from the T-SSEC (red line) and the measurements (blue symbols). Parameters S_{11} and S_{22} are represented in Smith chart format, and S_{21} and S_{12} are represented in polar format with a maximum scale of 2.0.

fects: (i) bulk traps in the gate-to-drain region of the GaN channel [157] which modify the conduction band of the heterostructure [158], and (ii) traps at the metal-semiconductor interface which degrade the conduction of the source and drain ohmic contacts and thus the on-resistance of the transistors. Both effects are compatible with the configuration of the proposed equivalent circuit, since both types of traps increase the source-to-drain resistance, an effect that is globally taken into account by the RC tank. In a virgin device, charged traps increase the impedance at low frequency,

Circuit element	S-SSEC (before HPC)	T-SSEC (before HPC)	T-SSEC (after HPC)
R_i	8 Ω	8 Ω	8 Ω
C_{gs}	50 fF	50 fF	50 fF
R_{gd}	45 Ω	45 Ω	45 Ω
C_{gd}	12 fF	12 fF	12 fF
R_{ds}	320 Ω	320 Ω	300 Ω
C_{ds}	20 fF	20 fF	20 fF
g_m	17.5 mS	18.5 mS	22.5 mS
τ	0.8 ps	0.8 ps	0.8 ps
R_T	-	380 Ω	100 Ω
C_T	-	550 fF	240 fF

Table 4.2: Parameters of the SSEC for the two models before and after HPC.

being around 1 kΩ at zero bias. When biasing the devices, the amount of the trapped negative charge is lowered, so that when reaching the HPC, the influence of the traps is reduced, and the zero bias impedance is reduced to around 40 Ω (Figure 4.12). We attribute the initial trapped charges to crystal defects that could possibly be repaired when enough power is dissipated in the device, so that afterwards their influence is permanently reduced. Such a restoration effect produced by the HPC bias would mainly affect the slower traps, thus leading to the shift to higher values observed in the cutoff frequency of the dispersion phenomena. Another possibility to explain the observed effects is that the onset of the current flow leads to a permanently empty state of the traps initially increasing the resistance in virgin devices.

4.1.2.2. MC simulation to extract the S-SSEC

We have seen that after applying HPC in the measurements, the trapping effects are negligible, which allows us to use our MC simulator to study the equivalent circuit without including the *RC* tank related to the dispersion effects, i.e., using the S-SSEC.

Low drain bias voltage

The objective now is to extract the equivalent circuit by means of MC simulations by considering the ETM with TBR (see Figure 3.26) in order to reproduce the values of the elements of the S-SSEC model obtained experimentally from the S-parameters of transistor 6N (L_G = 150 nm, L_{DS} = 2.5 μm and W = 2 × 25 μm). Note that, as in the previous chapter, in the case of MC modeling we will study transistor 2N (L_G = 150 nm, L_{DS} = 1.5 μm and W = 2 × 25 μm),[12] with the same L_G of transistor 6N, which is the key dimension.[13] The experimental and simulated output and transfer characteristics of this transistor were shown in Figures 3.26(a) and (b) respectively.

The method used in the MC tool to extract the equivalent circuit was explained in subsection 1.3.2. We first choose the DC values (V_{DS}^{MC} = 6 V, V_{GS}^{MC} =-8 V)[14] as the initial condition of the subsequent current transients. Then, two type of transient simulations are performed, one with a voltage step applied at the gate (ΔV_{GS} = 0.05 V) and another with a voltage step at the drain (ΔV_{DS} = 0.25 V). Before applying the voltage step, 3000 iterations (Δt = 1 fs) at the initial bias point are simulated. These steps are small enough to assume linear response (avoid harmonic generation) and

[12] The difference in the drain-to-source length only affects the low-bias slope of the output characteristics (see Figure A.3 of Appendix A)

[13] The impact of geometry will be discussed in subsection 4.1.3

[14] Note that this MC bias point provides a drain current value quite similar to the experimental one forV_{DS} = 6 V, V_{GS} =-3 V. We distinguish between MC and experimental voltages according to Figure 3.17, with V_{SCH} = 4.5 V and R_C = 1 Ω · mm.

high enough to originate a significant change in the current level. To remove the stochastic noise, an average over 50 transients is performed. Figure 4.16 shows the transients of gate (port 1) and drain (port 2) current resulting from such a process. In the transients, a peak at $t = 0^+$ (time moment at which the step is applied) always appear, which is related with the capacitance of the intrinsic device. This peak is proportional to the temporal derivative of the applied voltage perturbation and it is pure displacement current [55, 86]. To get a proper estimation of the intrinsic capacitances, the correct evaluation of these current spikes is essential [159].

The Y-parameters are obtained from the Fourier Transform of the current transients previously shown, following Equations 1.38 and 1.39 for the real and imaginary parts of Y_{ij} respectively, where the terms $I_i(0)$ and and $I_i(\infty)$ are the stationary currents before and after the voltage step, respectively. The integrals of Equations 1.38 and 1.39 must be evaluated along a time long enough for the current to reach $I_i(\infty)$. According to the transients shown in Figure 4.16, we consider that a time of 2 ps (2000 iterations) is reasonable for the integrals. Figure 4.17 shows the Y_{ij} obtained from the transients of Figure 4.16 as a function of frequency. Figure 4.17(a) reports the parameters Y_{i2}, which are extracted from the current response to the voltage step at the drain (port 2), and Figure 4.17(b) the parameters Y_{i1}, which are extracted from the current response to the voltage step at the gate (port 1). The real part of Y_{12} is practically 0 in the simulations, which means that R_{gd} is negligible (Equation 4.12). The real part of Y_{22} is constant and related to R_{ds} (Equation 4.14). In Equations 4.12 and 4.14, it can be observed that the sign of the imaginary part is opposite in Y_{12} and Y_{22}, and the slope of Y_{22} *vs.* frequency is higher than that of

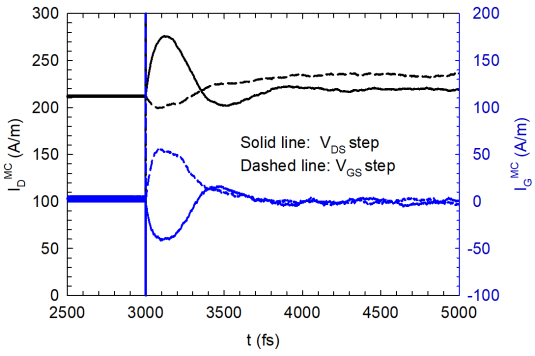

Figure 4.16: Gate (blue lines, right axis) and drain (black lines, left axis) current transients at the bias point $V_{DS}^{MC} = 6$ V, $V_{GS}^{MC} = -8$ V in response to voltage steps applied at the drain electrode ($\Delta V_{DS} = 0.25$ V, solid lines) and at the gate electrode ($\Delta V_{GS} = 0.05$ V, dashed lines).

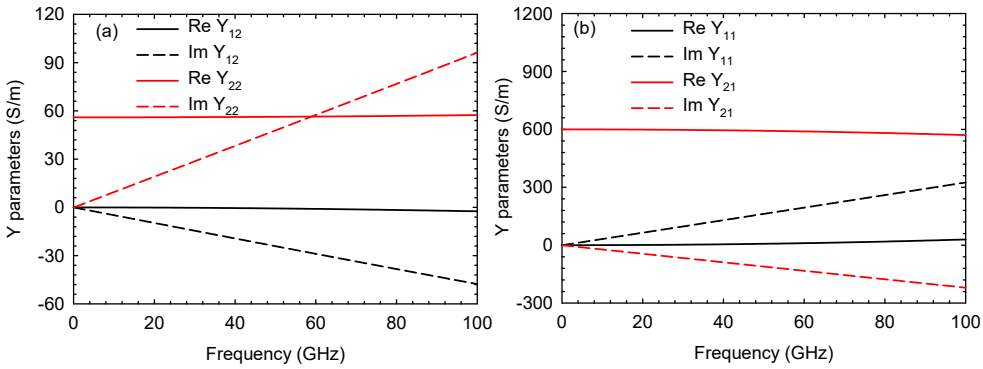

Figure 4.17: Frequency dependence of real and imaginary parts of the Y-parameters at the bias point V_{DS}^{MC} = 6 V and V_{GS}^{MC} =-8 V: (a) Y_{12} and Y_{22}, and (b) Y_{11} and Y_{21}.

Y_{12}, as it happens in the simulations. On the other hand, within the range of frequencies studied in this work, the real part of Y_{11} is practically zero, as it can be inferred from Equation 4.11, and the real part of Y_{21} is constant and related with g_{m_0} (Equation 4.13). Regarding the imaginary parts, they have different sign, as concluded from Equations 4.11 and 4.13. We conclude that the Y-parameters obtained from MC simulations follow the behavior described by Equations 4.11 to 4.14.

Once the admittance parameters are obtained, the elements of the S-SSEC are calculated like in the case of experimental results, using Equations 4.15-4.22. In Figure 4.18, the frequency dependence of the elements of the S-SSEC at the bias point V_{DS}^{MC} = 6 V and V_{GS}^{MC} =-8 V is reported. It is important to remind that we have chosen this bias point as case test because in the MC simulation it exhibits the same I_D than the experimental bias conditions V_{DS} = 6 V and V_{GS} =-3 V, for which we have also obtained experimentally the values of the S-SSEC elements. The validity of the S-SSEC model to describe the AC behavior of the transistor is confirmed by the fact that the different elements are frequency independent. In Figure 4.18(a), g_{m_0} and g_d are plotted in the left axis, and R_i in the right one. Figure 4.18(b) shows C_{gs}, C_{gd} and C_{ds} in the left axis, and τ in the right one. In Table 4.3, the results obtained from both simulations (at V_{DS}^{MC} = 6 V, V_{GS}^{MC} =-8 V) and measurements (at V_{DS} = 6 V, V_{GS} =-3 V) are shown. Although the agreement is not good, which was expected since the bias point is different even if the drain current is the same, MC results are well in the range of the experimental ones. The discrepancies between the values of the capacitances obtained in the simulations with the much higher ones found in the experiments are related to the fact that some parasitic capacitive effects associated with the topology of the devices cannot be de-embedded from experiments, even using the dummies studied in section 4.1.2. These capacitances should be added to the intrinsic

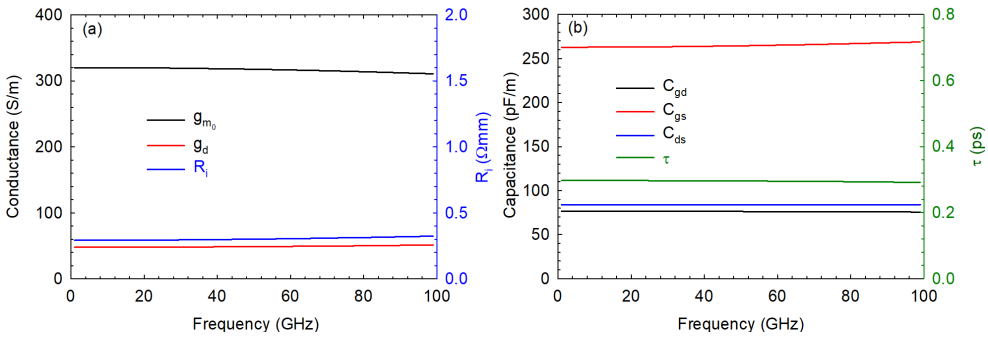

Figure 4.18: MC S-SSEC elements *vs.* frequency: (a) transconductance and drain conductance in the left axis and R_i in the right one, (b) capacitances in the left axis and τ in the right one. Bias point: V_{DS}^{MC} = 6 V, V_{GS}^{MC} =-8 V (with the same drain current as V_{DS} = 6 V, V_{GS} =-3 V in experiments)

S-SSEC as explained in [160], and their values have to be determined by fitting the experimental data at zero current, where it remains only the effect of the geometric (extrinsic and intrinsic) capacitances, which are independent of the biasing.

In order to check the dependence of the S-SSEC elements on the biasing, we perform MC simulations at V_{DS}^{MC} = 6 V and different V_{GS}^{MC} (from -9 V to -4 V). Figure 4.19(a) shows g_{m_0} and g_d as a function of the I_D^{MC} (without post-processing) obtained at each V_{GS}^{MC}. The experimental values at V_{DS} = 6 V, V_{GS} =-3 V are indicated by circles for the sake of comparison. g_d is practically constant with I_D and slightly higher than the experimental one. On the other hand, g_{m_0} changes with the bias conditions following the same behavior found at DC level. When the channel is closed (pinchoff), the transconductance is null and then increases as the channel opens, until reaching a saturation value and even decrease at the higher currents.

Circuit Element	Experimental	Monte Carlo
R_i (Ωmm)	0.65	0.3
C_{gs} (pF/m)	600	265
C_{gd} (pF/m)	200	76
g_d (S/m)	23	49
C_{ds} (pF/m)	180	84
g_{m_0} (S/m)	380	317
τ (ps)	0.8	0.3

Table 4.3: Parameters of the S-SSEC extracted from measurements (at V_{DS} = 6 V, V_{GS} =-3 V) and MC simulations (at V_{DS}^{MC} = 6 V, V_{GS}^{MC} =-8 V).

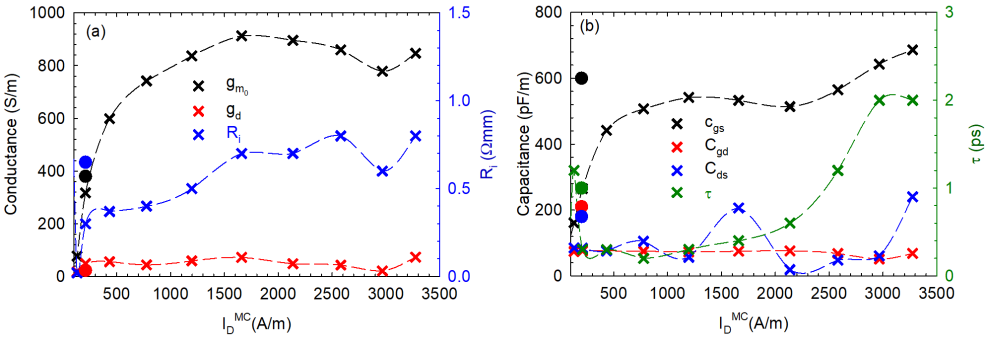

Figure 4.19: S-SSEC elements *vs.* I_D^{MC}: (a) transconductance and conductance in the left axis and R_i in the right one, (b) capacitances in the left axis and τ in the right one. $V_{DS}^{MC} = 6$ V. The circles indicate the values of the experimental S-SSEC elements in transistor 6N at the bias point V_{GS} =-3 V, $V_{DS} = 6$ V.

The experimental g_m is slightly higher than that extracted from the simulation. R_i is plotted in the right axis of Figure 4.19(a), showing a weak dependence on the drain current and a value similar to the experimental one. Concerning the capacitances as a function of I_D^{MC}, plotted in Figure 4.19(b), C_{gs} is the most dependent on the bias conditions, increasing with the current because it is related with the variation of carrier concentration with V_{GS} in the source side of channel [55]. Regarding C_{gd}, it is connected with the variation of the drain-side space-charge region originated by V_{DS}. The asymmetry of the space-charge region provokes that $C_{gd} < C_{gs}$, but they turn similar when V_{GS} is very negative [55]. Finally, C_{ds} is related with carriers reaching the substrate and it is nearly constant. Most of the values of C_{ds} and C_{gd} are smaller than the experimental ones. τ is represented in the right axis of Figure 4.19(b), taking values in the range 0.3 - 2 ps, increasing with I_D^{MC}.

High drain bias voltage

One of the objectives of this work is to study the impact of thermal effects on the RF behavior of the HEMT, in particular on the elements of the equivalent circuit. In the previous chapter we found that the ETM and the TRM provide the same current-voltage characteristics in DC regime and we concluded that the key parameter determining the influence of heating is the average temperature. Indeed, there is not a significant impact of hotspots on the drain current, at least at DC level [36]. However, in the case of the equivalent circuit, we have identified some parameters which depend on carrier concentration (and energy distribution) and type of transport in some specific regions of the device. Therefore, it is possible that in AC regime we may find

differences in the elements of the equivalent circuit between the TRM and the ETM when heating is significant. Is important to remind that in the TRM the temperature is homogeneous in the device, while the ETM approach considers the static solution of the heat conduction equation (HCE) (see subsection 1.2.2.2), resulting in a position-dependent temperature distribution.

In order to identify the influence of heating, we have performed simulations at bias points with much more dissipated power than in the previous subsection, with $V_{DS}^{MC} = 30$ V and different V_{GS}^{MC}. Under this biasing, the higher hotspot temperature with respect to the average temperature is expected to have an impact on the values of the S-SSEC parameters and originate differences between those calculated with the TRM and the ETM. The results of both models are compared in Figure 4.20(a) for g_m and g_d in the left axis and R_i in the right axis. Substantial differences are observed in g_m for $I_D^{MC} > 1000$ A/m, g_m being systematically higher when calculated with the ETM. In contrast, the values of R_i are quite similar, as expected since it is associated to an ohmic region far from hotspots.

In Figure 4.20(b) the extracted capacitances are plotted. Differences in C_{gd} are expected between both models due to the presence of the hotspot close to the gate in the gate-to-drain region, which could have an effect in the concentration and energy of carriers. However, due to the very small value of C_{gd}, we have not enough precision to identify significant differences. If we compare the S-SSEC parameters obtained at high V_{DS}^{MC} with those calculated at a lower value (shown in Figure 4.19), most of them take similar values for the same level of I_D^{MC}, except g_m, which is smaller for higher V_{DS}^{MC} due to thermal effects.

With the aim of explaining the differences found in g_m and g_d, in Figure 4.21(a) we compare the DC output characteristics obtained with both thermal models for

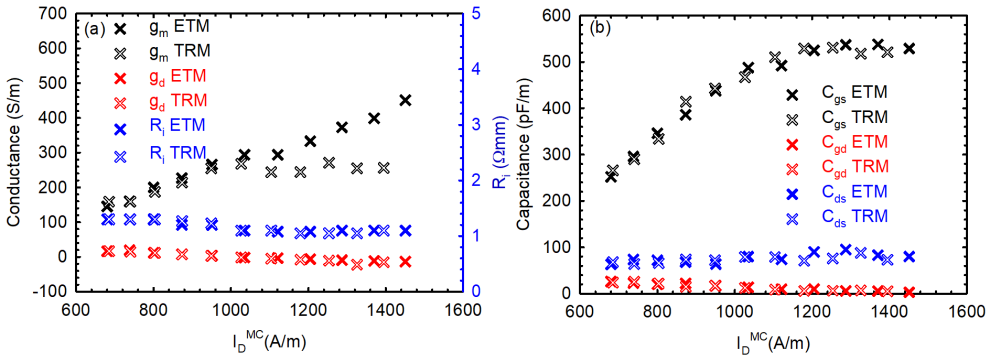

Figure 4.20: S-SSEC elements from ETM and TRM *vs.* I_D^{MC}: (a) transconductance and conductance in the left axis and R_i in the right one, (b) capacitances. $V_{DS}^{MC} = 30$ V.

high V_{GS}^{MC} providing large values of I_D^{MC} ($>$ 1000 A/m). As observed, due to the very high dissipated power, a remarkable decrease of I_D^{MC} takes place at increasing V_{DS}^{MC}. At low P_{Diss} both models provide essentially the same I_D^{MC} (see Figure 3.24), but when the channel is very open ($I_D^{MC} > 1000$ A/m), differences emerge, with the ETM current being systematically higher than the TRM one, this fact being at the origin of the behavior of g_m and g_d observed in Figure 4.20(a). In particular, the difference in I_D^{MC} is quite clear at the bias point $V_{DS}^{MC} = 30$ V and V_{GS}^{MC} =-4 V, corresponding to $I_D^{MC} \sim 1500$ A/m. To have a deep insight into this behavior, Figure 4.21(b) shows the average temperature T_{AV} extracted with the ETM as a function of the dissipated power P_{Diss}.[15] The black line corresponds with Equation 3.13 for $R_{TH} = 19.25$ mm·K/W. The TRM reproduces the results of the ETM at the lower dissipated powers, but the differences become evident when the channel is open and the dissipated power significantly increases.

Figure 4.22 shows the average and maximum temperatures (T_{AV} and T_{MAX}) extracted from the ETM (with TBR) and the temperature T_{latt} provided by the TRM for $R_{TH} = 19.25$ mm·K/W (used in the simulations) as a function of I_D for two values of V_{DS}. It can be observed that T_{AV} obtained with ETM is very similar to the temperature of the TRM for $V_{DS}^{MC} = 15$ V, when P_{Diss} is low. However, when I_D increases (and thus P_{Diss}), T_{AV} of the ETM always underestimates the temperature provided by the TRM. This effect is much more evident for $V_{DS}^{MC} = 30$ V, since it

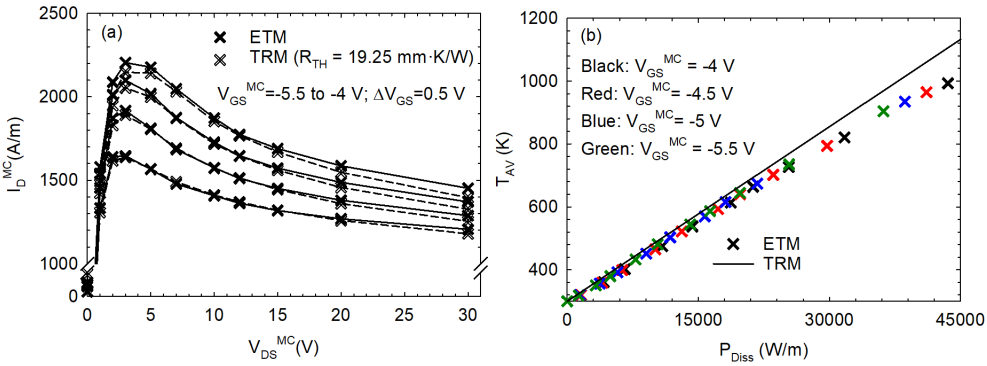

Figure 4.21: (a) Output characteristics obtained with the ETM (solid lines and symbols) and the TRM (dashed lines and void symbols) $R_{TH} = 19.25$ mm·K/W) and (b) dependence of the average temperature with the dissipated power. Symbols correspond to the points in the I_D-V_{DS} curves of the ETM and the black line to the temperature provided by the TRM with $R_{TH} = 19.25$ mm·K/W.

[15] Within the ETM, it is possible to calculate the power dissipated at every position inside the device and, by integration, the total dissipated power.

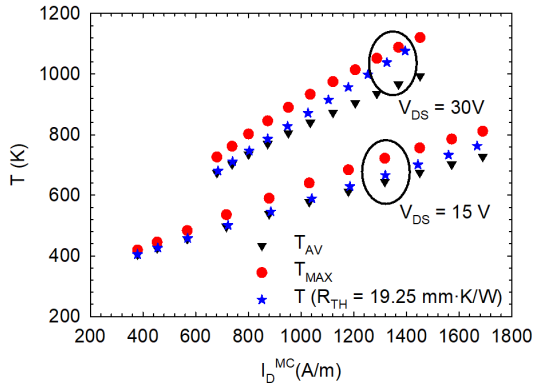

Figure 4.22: Average (T_{AV}) and maximum (T_{MAX}) temperatures extracted from the ETM, and T_{latt} used in the TRM simulations (obtained with R_{TH} = 19.25 mm·K/W), calculated for two values of V_{DS}^{MC}, 15 and 30 V.

leads to higher values of P_{Diss}. Indeed, in this case, for the higher values of I_D, the TRM temperature takes similar values to those of T_{MAX}. Therefore, we conclude that one of the two approaches, the TRM or the ETM, may not take properly into account some mechanism related to heating at very high dissipated powers.

In order to find the reasons for this behavior, we can have a look to the profile of electron energy inside the device (provided intrinsically by the Monte Carlo simulation), shown in Figure 4.23(a) for the bias point V_{DS}^{MC} = 15 V, V_{GS}^{MC} =-4 V. As observed, the energy of electrons in the meshes closer to the drain electrode is higher than in the vicinity of the source electrode, what indicates electrons have not been able to thermalize before reaching the drain contact, so that the excess of energy is not included in the resolution of the HCE. Figure 4.23(b) shows the same map of energies for V_{DS}^{MC} = 30 V, V_{GS}^{MC} =-4 V. At this bias point, the differences between the electron energy nearby the electrodes are even more evident. To correct the ETM simulations, such excess of energy had to be taken into account. Specifically, the energy of the electrons surpassing the thermal energy should be added in the meshes closer to the drain contact as a heat source in the resolution of the HCE.[16] The lack of this source of heat leads to the underestimation of temperature by the ETM observed when P_{Diss} is high. In [31], the authors suggest that the implementation of the electron-electron scattering of the devices gives a more accurate description of the thermalization of hot carriers that arrive to the vicinity of the drain contact coming from the high-field region of the channel.

[16] For time reasons this correction has not been included in this work.

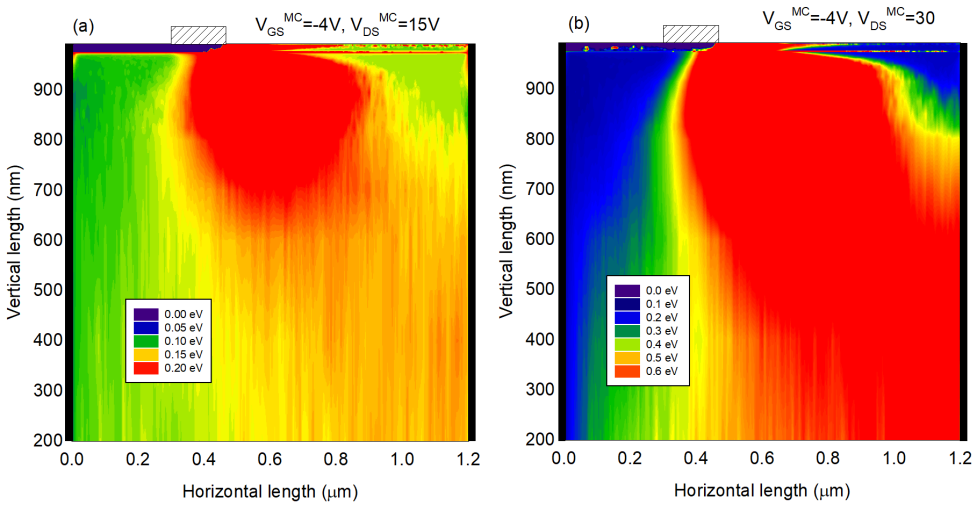

Figure 4.23: Map of electron energy inside the HEMT for the bias points V_{GS}^{MC} =-4 V, (a) V_{DS}^{MC} = 15 V, and (b) V_{DS}^{MC} = 30 V. The source and drain contacts are along the laterals in the figures.

Despite the mentioned problems, MC simulations allow to find some differences between the TRM and the ETM in the local contribution of the different regions of the device to some of the S-SSEC elements. Since the capacitances C_{gs} and C_{gd} are closely related with carrier concentration in the region around the gate, we can compare concentration maps in that region between both models, more specifically how the concentration changes with the gate voltage and thus contributes to the capacitances. We have calculated the difference in local carrier concentration for two different but close values of V_{GS}^{MC} (-5 and -6 V) and the same V_{DS}^{MC} (30 V). Figures 4.24 shows the results obtained with (a) the TRM and (b) the ETM for meshes under the gate around the channel, where the variations in the concentration between both bias points are more relevant.

In the gate-to-source region there are not noticeable differences between both models, but under the gate and in the gate-to-drain region (where heating effects are more relevant), despite the lack of resolution of the result, some changes are observed, both in the channel and in the bottom of the AlGaN layer,[17] which could be the origin of the different values of the capacitances (mainly C_{gd}) provided by the two models.

[17] At such high V_{DS}, electrons are able to reach the AlGaN layer.

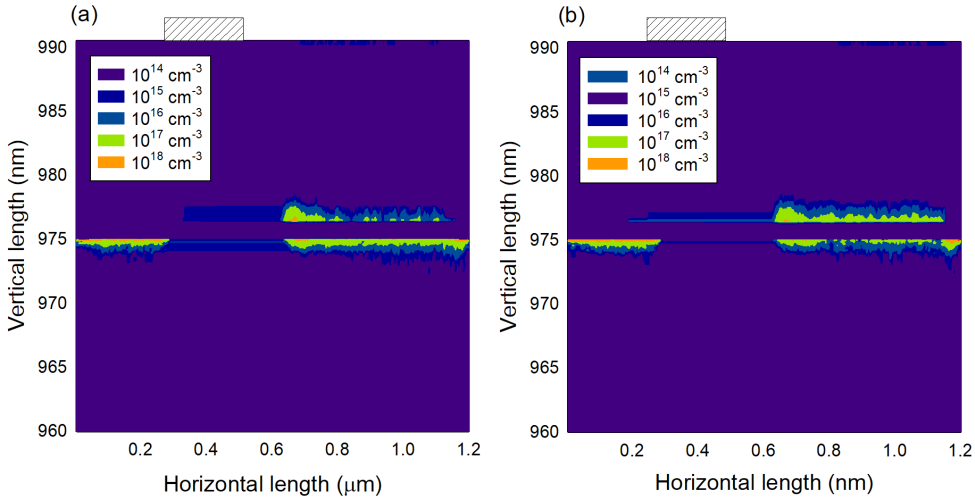

Figure 4.24: Map of local concentration difference between the gate bias points V_{GS}^{MC} =-5 V and V_{GS}^{MC} =-6 V, with V_{DS}^{MC} = 30 V. (a) TRM and (b) ETM.

4.1.3. Geometrical dependence of the S-SSEC

In previous subsections we have extracted general conclusions about several aspects of the physics of the device, like the origin of the dispersion in the S-parameters or the influence of self-heating on the equivalent circuit. However, the performance of the transistors also depends on geometrical parameters, like the gate size, drain-to-source distance or transistor width. We present now the influence of these parameters on the S-SSEC elements for the geometries in the wafer. We have measured devices (at V_{DS} = 6 V, V_{GS} =-3 V) with different L_{DS}, L_G and W in order to extract the elements of the S-SSEC from Equations 4.15-4.22 by applying the optimization algorithm, as explained in subsection 4.1.2. A summary of the elements of the S-SSEC model measured in eight different transistors are shown in Table 4.4. Since I_D and the area of the device scale with W, to allow a fair comparison, resistances have been multiplied by the width (R is inversely proportional to W), while capacitances have been divided (C is proportional to W).

The more relevant geometrical parameter is L_G, with a strong influence on the values of g_d and C_{gs}. Once again the behavior of g_d, which increases when L_G is shortened, can be explained in terms of the DC current-voltage characteristics (see Appendix A). A transistor with a longer gate has a more saturated I-V curve (lower drain conductance) due to the better control on carrier concentration in the channel. For not so short values of L_G as those considered here, g_m is not noticeably affected by the gate length. C_{gs} is always the higher of the three capacitances, with a decisive

Transistor	6N	8N	14N	16N	6W	8W	14W	16W
W (μm)	2×25	2×25	2×25	2×25	2×50	2×50	2×50	2×50
L_{ds} (μm)	2.5	2.5	4.5	4.5	2.5	2.5	4.5	4.5
L_G (nm)	150	75	150	75	150	75	150	75
R_{gs} (Ω mm)	0.65	0.60	0.55	0.65	0.30	0.40	0.20	0.20
C_{gs} (pF/m)	640	480	700	500	710	460	750	550
R_{gd} (Ω m)	5500	5000	6000	7500	5500	6500	5500	6000
C_{gd} (pF/m)	180	140	180	140	180	140	180	130
g_d (S/m)	33.3	55.5	33.3	58.82	32.25	76.92	33.3	66.7
C_{ds} (pF/m)	200	200	260	240	250	280	240	260
g_m (S/m)	380	400	380	380	420	420	430	420
τ (ps)	0.8	0.7	0.8	0.9	1	0.6	1.2	0.7

Table 4.4: Intrinsic elements of the S-SSEC model after the optimization with Qucs at the bias point V_{GS} =-3 V,V_{DS} = 6 V.

impact on the frequency response of the HEMT. It is closely related with the changes in carrier concentration in the source-side space-charge region originated by V_{GS}. In a similar way, C_{gd} is connected with the variation of the drain-side space-charge region originated by V_{DS}. However, the asymmetry of the space-charge region provokes that $C_{gd} < C_{gs}$ [55]. These premises explain the dependence of C_{gs} on L_G (higher capacitance for longer gate) and why C_{gd} is almost independent of L_G. The rest of geometrical parameters do not have a significant influence on the elements of the S-SSEC. L_{DS} does not modify the drain current level, so g_m hardly changes with L_{DS}. Moreover, a longer L_{DS} does not affect the depletion region, so the capacitances are practically constant with L_{DS}.

4.1.4. Cutoff frequencies f_t and f_{max}

To quantify the high-frequency capabilities of transistors or active devices, the two main figures of merit are the cutoff frequencies f_t and f_{max}. f_t is the frequency at which the hybrid parameter H_{21} takes the value 1, or 0 in dB units. In a two port device, H_{21} is the current gain (I_2 / I_1) when port 2 is short-circuited ($V_2 = 0$) [161]. Therefore, f_t is the maximum frequency at which the device is able to amplify the current and it is related to the the transit time of electrons below the gate. On the other hand, f_{max} is the frequency at which the unilateral power gain U reaches 0 dB. U is the maximum power gain that can be obtained from the two-port after it has been made unilateral under certain output matching conditions, according to the definition given by Mason [162]. U is an important figure of merit because it

is invariant. f_{max} is the maximum frequency at which the device is able to amplify power, i.e., the maximum frequency at which the device is still active. To extract f_t and f_{max} from measurements, H_{21} and U are calculated from the S-parameters with the usual matrix transformations [84]. U and H_{21} can be expressed in terms of S-parameters as

$$|H_{21}|(dB) = 20log\left|\frac{2S_{21}}{(1-S_{11})(1+S_{22})+S_{21}S_{12}}\right|, \tag{4.23}$$

$$U(dB) = 10log\frac{|(S_{21}/S_{12})-1|^2}{2k|S_{21}/S_{12}|-2\Re[S_{21}/S_{12}]}, \tag{4.24}$$

with k the stability factor, defined as

$$k = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{21}S_{12}|^2}{2|S_{12}S_{21}|}. \tag{4.25}$$

In subsection 4.1.1, we have explained how to extract the equivalent circuit of the pads in order to isolate their influence from the RF response of the HEMT. Therefore, we can derive two sets of cutoff frequencies, one including the effect of the pads (extrinsic) and another without it (intrinsic). We analyze the role of the geometry in f_t and f_{max} by means of the measurements done in the eight transistors with different L_G, L_{DS} and W. In Figure 4.25(a), the extrinsic H_{21} and U are plotted as a function of frequency up to 43.5 GHz, the available range of the VNA. The major differences between the values of H_{21} and U obtained with the S-SSEC model and the measurements are found in U mainly at low frequencies since the gate leakage current is not considered in the S-SSEC. However, at the higher frequencies, the model reproduces the measurements of both gains. The cutoff frequencies are estimated from Equations 4.23 and 4.24, which are functions with a -20 dB/dec slope (see Figure 4.25). Using the prediction obtained with the S-SSEC model, f_t and f_{max} are extracted just when H_{21} and U cross the value of 0 dB. For example, it is found that in transistor 6N ($L_G = 150$ nm, $L_{DS} = 2.5$ μm and $W = 2 \times 25$ μm), at the bias point V_{GS} =-3 V, $V_{DS} = 6$ V, has $f_t = 56$ GHz and $f_{max} = 79$ GHz.[18] Figure 4.25(b) shows the intrinsic H_{21} and U. It can be observed that now the cutoff frequencies are $f_t = 74$ GHz and f_{max} =105 GHz, higher than the extrinsic ones, as expected. Moreover, f_{max} is higher than f_t in this transistor.

In Table 4.5, the results of extrinsic and intrinsic f_{max} and f_t are summarized for the eight transistors with different dimensions. Again, it is evidenced that removing the parasitics increases the cutoff frequencies when compared with those extracted from direct measurements. Concerning the geometry dependence, as expected, the

[18] Note that these values are lower than the ones presented in Figure 3.6 because the operating point is not the same one.

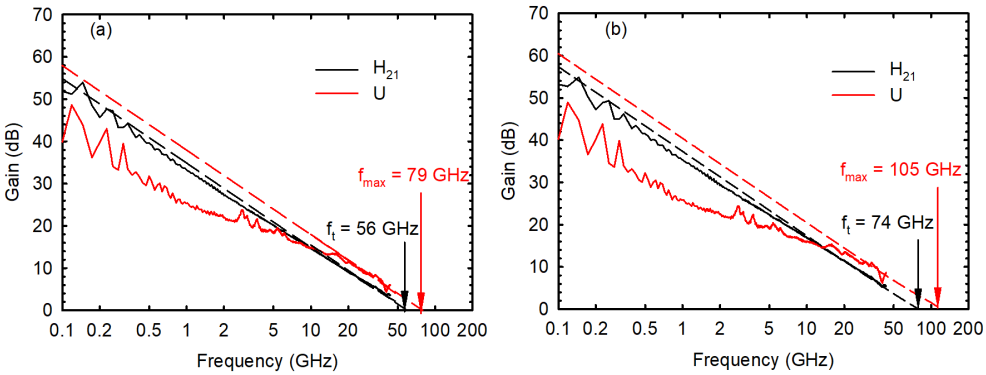

Figure 4.25: H_{21} and U in transistor 6N at the bias point V_{GS} =-3 V, V_{DS} = 6 V calculated from the (a) extrinsic and (b) intrinsic circuits. Solid lines represent the experimental results and dashed lines those extracted from the S-SSEC.

shorter the gate length the higher the value of f_t. In order to explain this behavior, we go to the first order approximation of f_t in the S-SSEC model [163]

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})}. \tag{4.26}$$

According to Equation 4.26, f_t is influenced by the two capacitances related with the space-charge region and accumulation of carriers below and close to the gate. According to Table 4.4, the longer the gate the higher C_{gs}, and we have also pointed out that $C_{gs} > C_{gd}$, becoming clear that the value of f_t is mainly affected by L_G via C_{gs}.

Concerning, f_{max}, we can also write a first order approximation expression, based on the S-SSEC, given by

$$f_{max} = \frac{f_t}{2((R_{gs} + R_s + R_g)g_d)^{1/2}}. \tag{4.27}$$

Transitor	Name	6 N	8N	14N	16N	6W	8W	14W	16W
Dimensions	W (μm)	2×25	2×25	2×25	2×25	2×50	2×50	2×50	2×50
	L_{DS} (μm)	2.5	2.5	4.5	4.5	2.5	2.5	4.5	4.5
	L_G (nm)	150	75	150	75	150	75	150	75
Extrinsic	f_t (GHz)	56	72	53	67	64	87	63	79
	f_{max} (GHz)	79	89	77	78	88	85	89	91
Intrinsic	f_t (GHz)	74	103	69	95	75	111	74	98
	f_{max} (GHz)	105	139	101	111	114	126	117	145

Table 4.5: Experimental intrinsic and extrinsic cutoff frequencies for eight transistors. Bias point V_{GS} =-3 V and V_{DS} = 6 V.

In Equation 4.27, the denominator, usually called input-to-output resistance ratio [164], should be smaller than unity to explain that $f_{max} > f_t$ (see Table 4.5). R_{gs} is the resistance of the gate-to-source ohmic channel, which takes a small value. R_g and R_s are the parasitic resistances, which should be minimized in the fabrication of the pads. In the saturation region g_d should be small if the control of the gate over the channel is good enough, about two orders of magnitude smaller than unity, making possible a denominator in Equation 4.27 also smaller than unity. f_{max} shows a dependence on L_G similar to that of f_t, the influence of L_G taking place again through C_{gs}, but also through g_d, which, as explained in the previous subsection, increases when L_G decreases. Such an increase of g_d in the denominator of Equation 4.27 is compensated by the increase of f_t in the numerator, so that an overall increase of f_{max} takes place when L_G decreases, even if not so pronounced like that of f_t. The values of f_t and f_{max} are much smaller than those shown in Figure 3.6 because the V_{DS} is much lower in this work (g_d and C_{gd} are higher).

To conclude, we can also study the influence of the bias conditions. Here we only show the intrinsic cutoff frequencies of transistor 2N (L_G = 150 nm, L_{DS} = 1.5 μm and $W = 2 \times 25$ μm) estimated from the MC simulations and extracted from the S-SSEC, shown in Figure 4.26. f_{max} is higher than f_t, reproducing the behavior found in the measurements.

Due to the discrepancies between modeling and experimental results of the S-SSEC already discussed (see subsection 4.1.2.2), the values of f_t and f_{max} extracted from the MC tool, as expected, are rather high as compared with the experimental ones from transistor 6N (L_G = 150 nm, L_{DS} = 2.5 μm and $W = 2 \times 25$ μm) at the bias

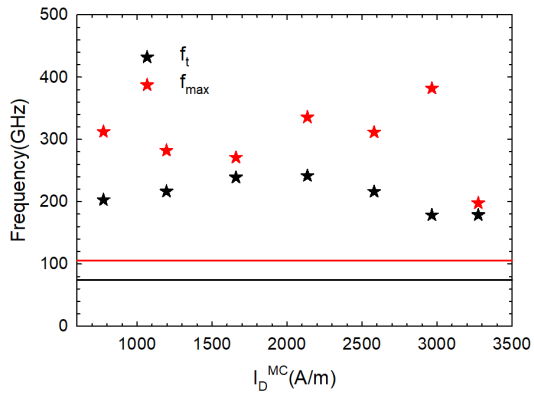

Figure 4.26: Dependence of f_t (black stars) and f_{max} (red stars) on drain current estimated from MC simulations in transistor 2N. Lines indicate the experimental values at the bias point V_{GS} =-3 V, V_{DS} = 6 V for transistor 6N.

point V_{GS} =-3 V, V_{DS} = 6 V, due to the influence of part of the parasitic elements that cannot be de-embedded in the experimental measurements [160]. In addition, the f_t and f_{max} of MC simulations have been estimated from Equations 4.26-4.27, which are approximated equations. More realistic values can be obtained from H_{21} and U [165]. Future experimental work will be oriented to study not only the dependence of the equivalent circuit on the bias conditions, but also on the operation temperature.

4.2. Detection with HEMTs

In Chapter 2 we have studied the RF detection capabilities of SSDs and G-SSDs. For completeness of this work, in addition to the previous section 4.1, where the RF behavior of HEMTs has been analyzed in detail in terms of the S-SSEC, this section aims to show that HEMT-like devices are also good candidates to operate as microwave detectors, even of sub-THz signals, well above their typical cutoff frequencies. For this purpose the very same GaN-HEMT wafer is now characterized, not only at room temperature but also up to 500 K, to extract the responsivity of HEMTs under different RF-coupling configurations. First of all, it is important to remark that when the transistor operates as detector, the framework is very different with respect to amplification or oscillation applications. The transistor acts as a one-port device with just one AC input, so two schemes can be defined depending in which terminal the RF power is injected: (i) drain-coupling scheme (DCS) or (ii) gate-coupling scheme (GCS). In both cases the source is grounded and the AC signal is superimposed to the DC bias.

The advances in the transistor speed have made possible to reach the THz milestone in amplification with a 25-nm InP HEMT [166], but the novelty of the FET-based THz detection concept is that transistors are able to detect RF signals much above their cutoff frequencies [167]. In HEMTs, the most accepted theory to explain the physical mechanism of detection is the Dyakonov-Shur plasma-wave theory [168]. Based in this theory, FETs used for THz detection have been imprecisely labeled as "plasma-wave detectors". However, instead of the enhanced responsivity at increasing frequency predicted by plasma-wave theory, a roll-off is found in many experiments, which can well be interpreted in terms of the effect of a parasitic capacitance [169]. Nevertheless, it must be noted that the rectification given by the non-linearity of the I_D *vs.* V_{DS} curves of transistors can be enhanced by resonant plasma waves at THz frequencies [170], but to a an extent lower than the expected by the Dyakonov-Shur theory because of the high-frequency dependence of the channel impedance [20], not usually considered in the theory [168].

The absence of a consensus about the plasma-wave origin of the experimental results has led to the study of other theoretical basements [105], for example using the well-established lumped element modeling of transistors in terms of the equivalent circuit (similar to the one presented in subsection 4.1.2). This model is able to explain the results obtained in some FETs (e.g. graphene FETs up to 67 GHz [105]) and has been helpful for the design optimization of the detectors. However, such a model is valid only for low frequencies ($<$ 100 GHz). For higher frequencies, a model with distributed elements should be considered [171].

We will now analyze the detection capabilities of the GaN HEMTs. In Chapter 2, we have used the (quasi-static) QS model to study the behavior of SSDs and G-SSDs. However, the use of the QS model when the channel is almost pinched-off is doubtful due to the low precision in the calculation of the derivatives, as discussed in subsection 2.4.2, and these bias conditions are precisely the more interesting ones in the case of the HEMTs. Therefore, here we put emphasis on the microwave experiments performed with a setup similar to that described in Figure 1.5 of subsection 1.1.2. We will analyze the HEMT with both DCS and GCS, trying to correlate the frequency response of the HEMT operating as a detector with the elements of the S-SSEC. Figure 4.27 shows the schematic picture of the S-SSEC, indicating the RF coupling in both schemes. In the DCS the gate is only used to bias the device in the appropriate region, while the drain terminal is the one used to inject the input signal. The DC output signal is recorded at the drain, commonly the DC drain voltage is measured in open circuit. On the other hand, in the GCS the gate contact is used to inject the input RF signal superimposed to the DC-bias gate voltage, and again the drain terminal is used to measure the DC output signal.

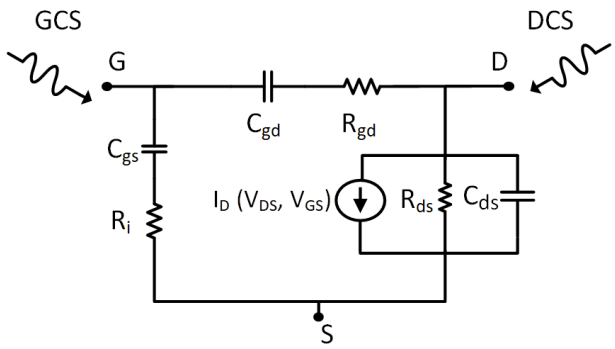

Figure 4.27: Schematic sketch of the S-SSEC with the corresponding parameters and illustration of RF coupling in both DCS and GCS when the HEMT operates as RF detector.

In this work we will follow the equivalent-circuit approach suggested for three-terminal devices in [105]. It consists basically in the use of the current source of the QS model, presented in subsection 1.1.1 for the two-contact SSD [87], combined with the classic S-SSEC of HEMTs to allow dealing with the DCS and GCS.

4.2.1. Drain-coupling scheme

In this configuration the microwave power is applied to the drain contact and the rectified voltage output is recorded in this terminal as well. For clarity, a DCS superscript will be used in the figures of merit. We start showing measurements corresponding to the HEMT 8N (L_G = 75 nm, L_{DS} = 2.5 μm and W = 2 × 25 μm). The DC output and transfer characteristics of this transistor can be found in Appendix A.

To understand the DCS results, it is very illustrative to analyze the effect of the RF signal on the output characteristics of the transistor around zero I_D by comparing them in presence and absence of the microwave power. The setup is essentially the same of Figure 1.5 in subsection 1.1.2. Figure 4.28(a) shows a schematic picture of the DCS for detection. The only difference is the use of the gate to bias the transistor in the appropriate point. In Figure 4.28(b), we show the I_D *vs.* V_{DS} measured with the RF signal ON and OFF. Power is 0 dBm (1 mW), frequency 1 GHz, and V_{GS} = -3.9 V. When the RF signal is ON the curve is shifted to the right, so that the detected voltage $\Delta V_{DCS} = V_{DS}^{ON} - V_{DS}^{OFF}$ is positive.

In order to evidence the influence of V_{GS}, Figure 4.29 shows (in the left axis) the responsivity $\beta_{50\Omega}^{DCS}$ *vs.* V_{GS}, again for 1 GHz and 1 mW of power applied to the drain, while biasing it with I_D = 0 A. The results correspond to transistor 7N (L_G = 100 nm, L_{DS} = 2.5 μm and W = 2×25 μm). In the right-axis, the I_D-V_{GS}

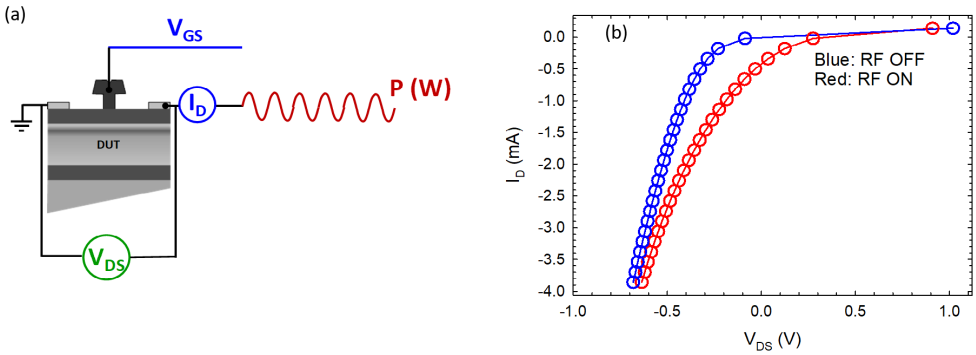

Figure 4.28: (a) Schematic picture of the setup used to characterize detection in the DCS. (b) I_D *vs.* V_{DS} measured in transistor 8N w/o an RF signal of 0 dBm and 1 GHz applied to the drain. V_{GS} =-3.9 V.

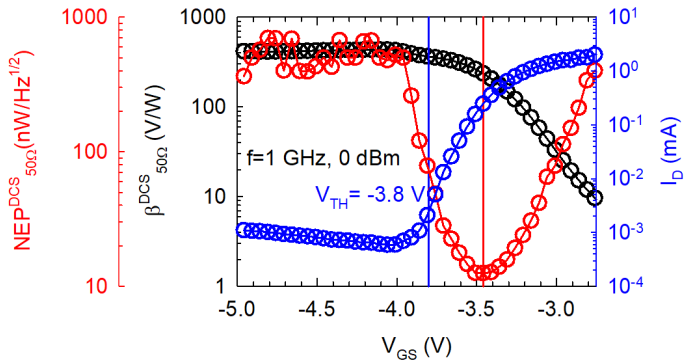

Figure 4.29: Left axis: $\beta_{50\Omega}^{DCS}$ and $NEP_{50\Omega}^{DCS}$ *vs.* V_{GS} measured in transistor 7N for a 1 GHz input signal of 0 dBm power applied to the drain (biased with zero current). The I_D-V_{GS} curve of the transistor at V_{DS} = 0.1 V is also plotted as a reference in the right axis.

curve of the transistor at V_{DS} = 0.1 V is shown.[19] When reducing V_{GS}, $\beta_{50\Omega}^{DCS}$ reaches a maximum of around 40 V/W at about V_{GS} =-3.9 V, when the HEMT is biased just below its threshold voltage V_{TH}, and then remains practically constant.

Regarding the $NEP_{50\Omega}^{DCS}$ (in the second left axis), we calculate it as explained in subsection 1.1.1

$$NEP_{50\Omega}^{DCS} = \frac{\sqrt{4k_BTR_j}}{\beta_{50\Omega}^{DCS}}, \tag{4.28}$$

with $R_j = \left(\frac{dI_D}{dV_{DS}}\right)^{-1}$ for every V_{GS}. The minimum of approximately 12 nW/Hz$^{1/2}$ is obtained around V_{GS} =-3.45 V, shifted 0.35 V with respect to the V_{TH} of this transistor. Hence, the transistor demonstrates quite good sensitivity as zero-bias detector.

Since we have access to transistors with different gate lengths, the influence of L_G on the RF detection can also be studied. In Figure 4.30 we compare the responsivity for three transistors with L_G = 75 nm (8N), 100 nm (7N) and 150 nm (6N) (all HEMTs with L_{DS} = 2.5 μm and $W = 2 \times 25$ μm) and V_{TH} of -4.3, -3.9 and -3.8 V respectively. To allow for a better comparison between transistors with different V_{TH}, the results are plotted *vs.* $V_{GS} - V_{TH}$, the gate voltage overdrive. As observed, at $V_{GS} - V_{TH} = 0$ V, $\beta_{50\Omega}^{DCS}$ takes it maximum value in the three transistors, being higher for longer L_G (6N).

According to the model proposed by [105], the frequency dependent expression of β_{opt}^{DCS} is

$$\beta_{opt}^{DCS}(\omega) = -\frac{1}{2}\gamma_{drain}R_j \frac{R_j}{R_j + R_d + R_s} \frac{1}{1 + \omega^2 C_{gd}^2 R_j (R_d + R_s)}, \tag{4.29}$$

[19] In the region where the device works in detection applications.

where R_d and R_s are the drain and source parasitic resistances respectively, and γ_{drain} stands for the bowing factor like in the QS model,

$$\gamma_{drain} = \left(\frac{\frac{\partial^2 I_D}{\partial V_{DS}^2}}{\frac{\partial I_D}{\partial V_{DS}}} \right) = \left(\frac{\partial^2 I_D}{\partial V_{DS}^2} \right) R_j. \tag{4.30}$$

It can be observed that under the condition $R_j >> R_d + R_s$ and in the low-frequency limit, the result of the QS model is recovered ($\frac{1}{2}\gamma_{drain} R_j$). In addition, taking into account the mismatch factor, it is straightforward to obtain the expression of $\beta_{50\Omega}^{DCS}$, when $R_j >> Z_s$, as

$$\beta_{50\Omega}^{DCS}(\omega) = -\frac{2 Z_s \gamma_{drain}}{1 + \omega^2 C_{gd}^2 (R_d + Z_s)^2}, \tag{4.31}$$

where Z_s is the characteristic impedance of the line. Since our measurements were done at 1 GHz and $C_{gd} = 9$ fF, the condition $\omega C_{gd}(R_d + Z_s) << 1$ is fulfilled, so that Equation 4.31 becomes that of the QS model for the strongly mismatched condition ($2Z_s\gamma_{drain}$). Therefore, the higher value of $\beta_{50\Omega}^{DCS}$ observed in the transistor with longer gate is consistent with the more pronounced non-linearity in the I_D *vs.* V_{DS} due to the better field-effect control achieved with a longer gate.

Finally, concerning the frequency dependence of the responsivity, Figure 4.31 shows the measurements up to 40 GHz for a 0 dBm input RF signal applied to the drain of transistor 7N (L_G = 100 nm, L_{DS} = 2.5 μm and W = 2×25 μm). A cutoff frequency f_c (-3 dB roll-off) of about 20 GHz is observed, obtained with a fitting to a Lorentzian decay $B/(1 + (f/f_c)^2)$.

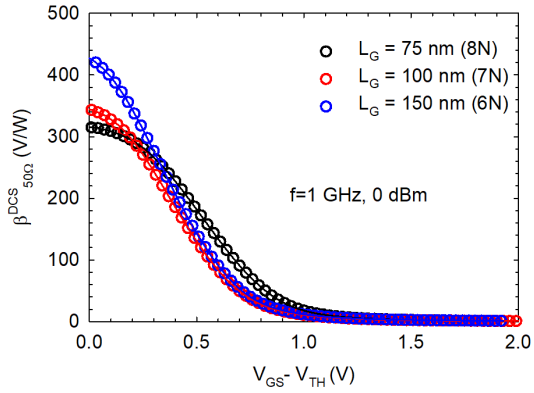

Figure 4.30: $\beta_{50\Omega}^{DCS}$ *vs.* gate bias for a 1 GHz input signal of 0 dBm power applied to the drain of three HEMTs with different gate length: 75 nm (8N), 100 nm (7N) and 150 nm (6N), V_{TH} =-4.3, -3.9 and -3.8 V respectively. The drain is biased with zero current.

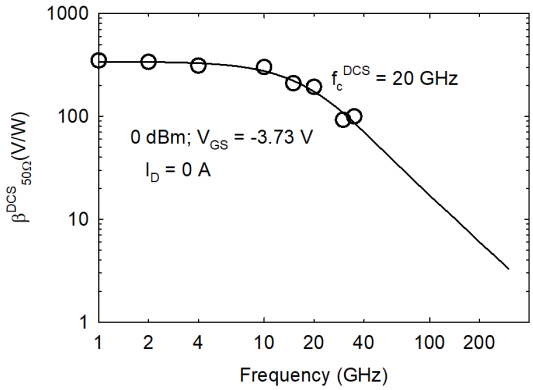

Figure 4.31: $\beta^{DCS}_{50\Omega}$ *vs.* frequency with power applied to the drain of transistor 7N. V_{GS} =-3.73 V.

According to the analytical model described in [105], the 3 dB frequency of halved responsivity is derived in terms of the equivalent circuit elements from Equation 4.29 and the mismatch factor as

$$f_{3dB}^{DCS} = \frac{1}{2\pi C_{gd}(R_d + Z_s)}. \tag{4.32}$$

It is remarkable that, according to Equation 4.32, C_{gd} is the key capacitance in the cutoff frequency of DCS responsivity, whereas in the case of amplification applications, that role is played by the total capacitance C_{gd}+C_{gs}, dominated by C_{gs} (see subsection 4.1.4). Since we are using the HEMT as one-port detector, only one of the capacitances of the S-SSEC (see Figure 4.27) is effective. In DCS the gate is AC grounded, so that C_{gs} is short-circuited, the influence of the gate resistance is null and only C_{gd} is effective. Moreover, according to the results observed in subsection 4.1.2.2, C_{gd} does not change with the bias conditions, corresponding to low current, and takes values of 9 fF, similar to that of C_{gs}. In addition to this value of C_{gd}, we have to consider the C_{acop} = 4 fF of the pad to compare with the experimental value. Thus, with C_{gd} = 13 fF, R_d = 5 Ω (extrinsic parameter obtained in subsection 4.1.1) and Z_s = 50 Ω in Equation 4.32, the 3 dB frequency is around 200 GHz, one order of magnitude higher than that observed in the measurements, what raises doubts about the validity of the model in [105] for the case of our HEMTs. Nevertheless, it is to be noted that the upper limit our setup is 43.5 GHz and therefore the value of f_c should be double-checked with measurements up to higher frequencies. In addition, we have estimated the corner frequency from S-SSEC elements obtained far from the conditions of the detection measurements, therefore a valid equivalent circuit should be extracted to have a more accurate estimation of the f_{3dB}^{DCS}.

4.2.2. Gate-coupling scheme

Now we analyze the detection for the case of the injection of the AC power into the gate contact. A GCS superscript will be used in the figures of merit. In this framework, the QS model developed in the subsection 1.1.1 has to be adapted to predict the matched responsivity as follows [105]

$$\beta_{opt}^{GCS}(\omega) = -\frac{1}{2}\gamma_{gate}R_j\frac{R_j}{R_j+R_s}\frac{1}{1+\omega^2C_{gs}^2R_sR_j}, \tag{4.33}$$

which, under the condition $R_j >> R_s$ and in the low-frequency limit, coincides with the the QS model ($\frac{1}{2}\gamma_{gate}R_j$). Now the bowing factor is

$$\gamma_{gate} = \left(\frac{\partial^2 I_D}{\partial V_{DS}^2} + 2\frac{\partial^2 I_D}{\partial V_{DS}\partial V_{GS}}\right)R_j. \tag{4.34}$$

Note that now the bowing factor contains not only the second partial derivative in V_{DS}, but also a mixed derivative involving V_{GS}. As usual, in the mismatched situation the responsivity includes the power reflection with the CPW of Z_s impedance. Taking the mismatch into account and under the condition $R_j >> Z_s$, we can write

$$\beta_{50\Omega}^{GCS}(\omega) = -\frac{2\gamma_{gate}Z_s}{1+\omega^2C_{gs}^2(R_s+Z_s)^2}. \tag{4.35}$$

In the low-frequency limit, this expression provides a responsivity $2\gamma_{gate}Z_s$. Since we are interested in experimental results, the setup is modified to implement this coupling configuration, shown schematically in Figure 4.32.

As done for the DCS, in order to understand the effect of the RF signal applied to the gate on the output characteristics of the transistor, it is useful to compare them around zero I_D measured in presence and absence of the RF signal, as reported in Figure 4.33(a) for an applied signal of 1 GHz and 0 dBm of input power to the gate of transistor 8N (L_G = 75 nm, L_{DS} = 2.5 μm and W = 2×25 μm) at V_{GS} =-4 V.

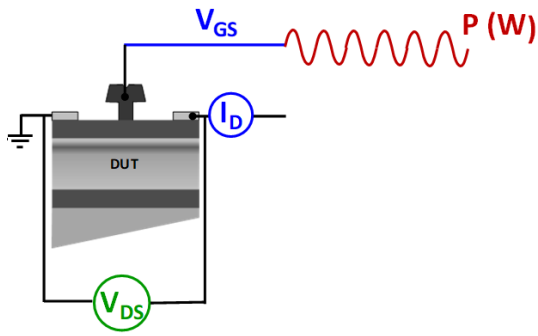

Figure 4.32: Schematic picture of the gate-coupling setup.

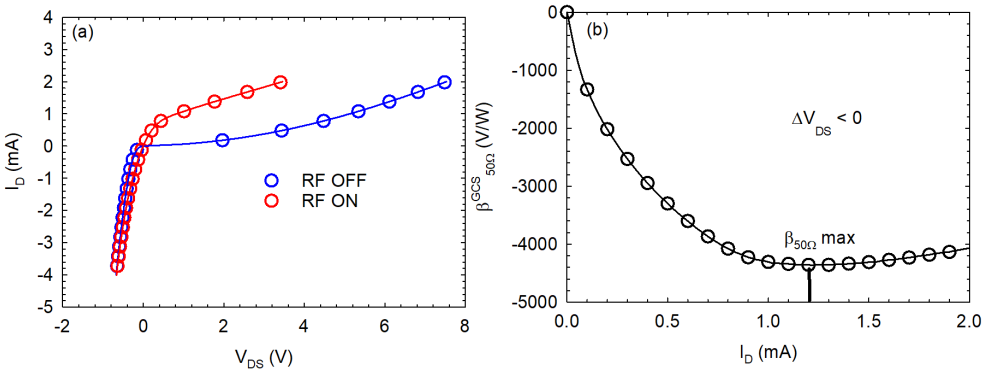

Figure 4.33: (a) I_D *vs.* V_{DS} measured in transistor 8N without and with a RF signal of 0 dBm and 1 GHz applied to the gate. (b) $\beta^{GCS}_{50\Omega}$ *vs.* I_D. V_{GS} =-4 V.

The first difference respect to the DCS evidenced in the figure is the shift of the curve to the left when the RF is ON, thus providing a negative detected voltage $\Delta V_{GCS} = V^{ON}_{DS}$- $V^{OFF}_{DS} < 0$. Figure 4.33(b) shows the results of the responsivity $\beta^{GCS}_{\beta_{50\Omega}}$ as a function of the drain current for V_{GS} =-4 V. Here, a second main difference compared with the DCS appears. When $I_D = 0$ A, the responsivity is nearly zero, however, a huge enhancement is achieved by increasing the drain current, reaching a maximum of more than 4 kV/W at about $I_D = 1.2$ mA, one order of magnitude higher than the maximum value obtained in Figure 4.29 for the DCS.

Now we will analyze the frequency dependence of the responsivity at the bias point where we have observed the maximum, i.e., for $I_D = 1.2$ mA. The results are reported in Figure 4.34(a). Like in the DCS, we have fitted the experimental data to a function $B/(1+(f/f_c)^2)$, obtaining a value of $f_c = 40$ GHz. From the circuit theory the 3 dB frequency of halved responsivity in the case of GCS f^{GCS}_{3dB} is given by [105]

$$f^{GCS}_{3dB} = \frac{1}{2\pi C_{gs}(R_s + Z_s)}, \tag{4.36}$$

where, in the GCS, C_{gs} is the key capacitance. Unlike C_{gd} in Equation 4.32, C_{gs} is a strongly bias-dependent parameter (see Table 4.4). If we use the values of the circuit elements in transistor 8N for channel pinch-off conditions ($C_{gs} = 13.2$ fF , $R_s = 5\ \Omega$ and $Z_s = 50\ \Omega$), the 3 dB frequency is around 150 GHz, while for open channel ($C_{gs} = 25$ fF) it is 80 GHz. Like in the DCS, the values of the 3 dB frequencies expected from the circuit model are higher than the measured ones. Anyway, the detection capabilities of our HEMTs in both DCS and GCS would require more systematic measurements up to frequencies beyond the 43.5 GHz limit or our available equipment. We believe that the low values obtained for the cutoff frequencies could be due to the parasitic capacitances associated to the coplanar wave accesses needed for the

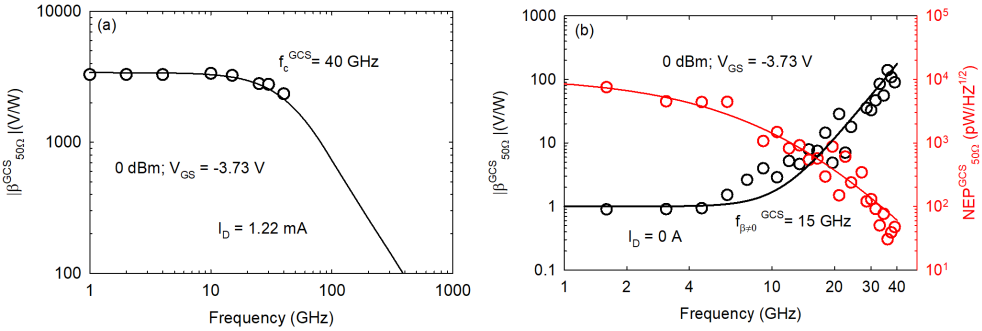

Figure 4.34: (a) $|\beta^{GCS}_{50\Omega}|$ *vs.* frequency measured at the bias point I_D = 1.22 mA. (b) GCS responsivity and NEP *vs.* frequency for I_D = 0 A. In both figures the input power is 0 dBm and V_{GS} =-3.73 V.

measurements with RF probes. The use of free-space RF coupling by means of well-designed antennas is the way to overcome the limits imposed by RF characterization under probes, thus possibly allowing sub-THz detection with these devices.

According to the equivalent circuit shown in Figure 4.27 and the rectification mechanism of the GCS, at low frequencies and with I_D = 0 A, the gate-to-drain branch is open circuited, and so the detected voltage is 0, since the signal does not reach the origin of the non-linearity at the drain terminal. Only if the AC signal is applied to the drain, this terminal provides a non-zero DC output. However, at higher frequencies fulfilling the condition $1/\omega C_{gd} \rightarrow 0$, the RF reaches the drain since this branch is short-circuited and now a DC drain output voltage is measured. Figure 4.34(b) demonstrates that this interesting effect takes place in our HEMT: at low frequency $\beta^{GCS}_{\beta_{50\Omega}}$ is very small, while for frequencies higher than a threshold denoted by $f^{GCS}_{\beta\neq0}$, it increases significantly. $f^{GCS}_{\beta\neq0}$ can be expressed in terms of the elements of the S-SSEC associated to the gate-to-drain region, R_{gd} and C_{gd}, as

$$f^{GCS}_{\beta\neq0} = \frac{1}{2\pi R_{gd} C_{gd}}. \tag{4.37}$$

Using the values shown in Table 4.4 for transistor 8N, $R_{gd} \sim 50\,\Omega$ and $C_{gd} \sim 12$ fF, one obtains $f^{GCS}_{\beta\neq0} \sim 15$ GHz, indeed the frequency at which both the responsivity and $NEP^{GCS}_{\beta_{50\Omega}}$ change their behavior in Figure 4.34(b), with the $NEP^{GCS}_{\beta_{50\Omega}}$ decreasing from values around 10^4 to values around 10^2 pW/Hz$^{1/2}$.

4.2.3. Influence of temperature

This last subsection is devoted to the study of the influence of temperature on the detection of the HEMTs. First, we measure the *I-V* curves of transistor 2N

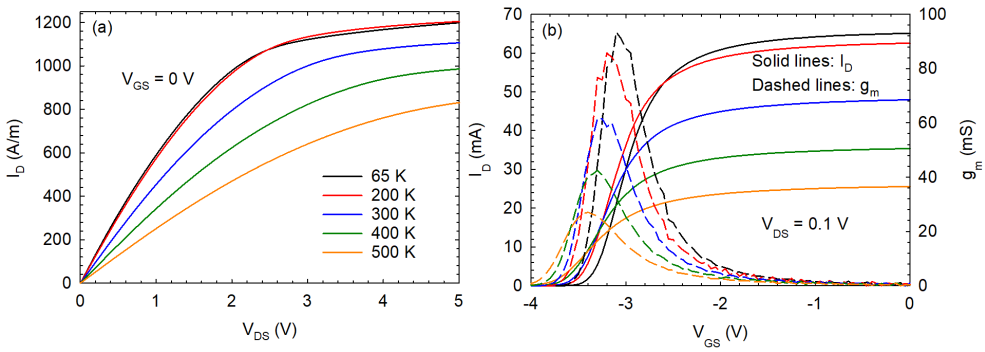

Figure 4.35: (a) Output characteristic for V_{GS} =0 V, and (b) transfer characteristic (left axis) and transconductance (right axis) at V_{DS} = 0.1 V measured at different temperatures in transistor 2N.

(L_G = 150 nm, L_{DS} = 1.5 μm and W = 2 × 25 μm) at different temperatures. Figure 4.35(a) shows the output characteristic for V_{GS} =0 V, exhibiting the expected decrease of I_D as T increases. It is remarkable that the more pronounced differences between curves take place at the higher temperatures. Figure 4.35(b) shows the transfer characteristic and g_m at V_{DS} = 0.1 V, in the region where the device works in detection applications. A substantial decrease of g_m with temperature is observed, again more noticeable at the higher temperatures and a threshold voltage shift towards lower voltage.

Figure 4.36 shows the dependence of V_{TH} with temperature. The increase of temperature makes harder to pinch off the channel, leading to a more negative V_{TH}. Two regions with different slope can be identified, below and above 250 K. Once again, the changes in V_{TH} are more pronounced at the higher temperatures (larger slope). This behavior could be related to the activation of defects in the bulk or traps in the heterojunction, which affect the concentration and current level in the channel of the transistors.

Drain-coupling scheme

Once the dependence of the static behavior on temperature has been presented, we analyze the microwave detection under the DCS. Figure 4.37(a) shows $\beta_{50\Omega}^{DCS}$, for T < 250 K and Figure 4.37(b) for $T \geq$ 250 K. In both cases, an RF signal of P_{IN} =-0.96 dBm and 1 GHz is applied to the drain, biased at zero current. When decreasing V_{GS}, starting from open-channel conditions, the responsivity increases as pinch-off is approached for all temperatures. However, in the sub-threshold region, different results are observed depending the temperature range. For T < 250 K, $\beta_{50\Omega}^{DCS}$

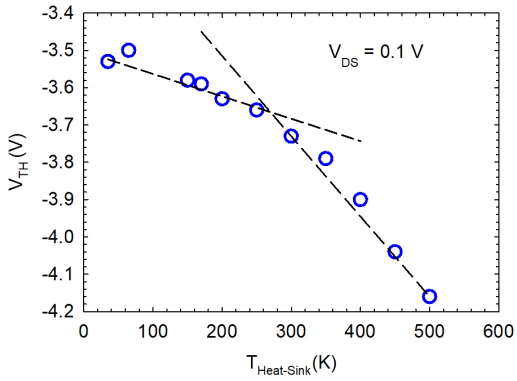

Figure 4.36: V_{TH} *vs.* temperature in transistor 2N. Dashed lines are an eye-guide to mark the two regions.

decreases abruptly after reaching the maximum at a gate voltage slightly more negative than the threshold voltage, while for $T \geq 250$ K the values of $\beta_{50\Omega}^{DCS}$ remain practically constant once the maximum is reached, as already observed in Figure 4.29 for room temperature. The temperature range observed, around 200-250 K, is similar to that found in the SSDs of subsection 2.3.6. Thus, it could be explained in terms of trapping phenomena in the bulk with characteristic activation energies [111, 112, 113].

Finally, Figure 4.38 shows $\beta_{50\Omega}^{DCS}$ measured as a function of frequency at V_{GS} =-4.5 V (sub-threshold region). Despite the results are rather noisy, a frequency roll-off is observed for $T > 200$ K, while at lower temperatures $\beta_{50\Omega}^{DCS}$ is nearly flat. Measurements up to much higher frequencies are required in order to properly extract the cutoff

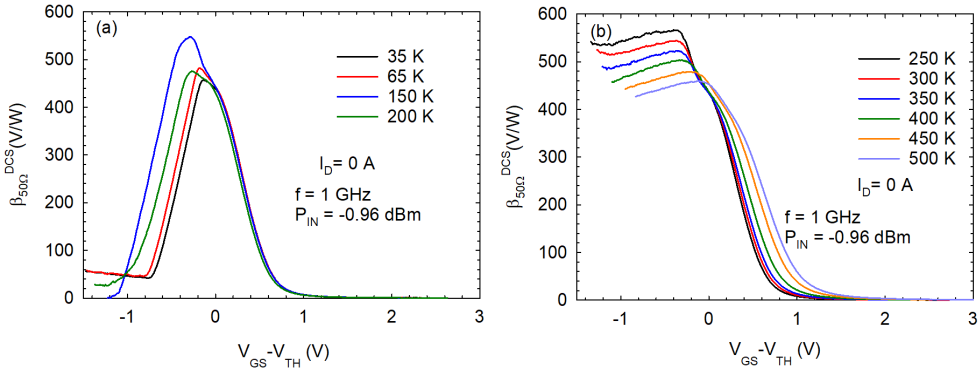

Figure 4.37: $\beta_{50\Omega}^{DCS}$ *vs.* V_{GS}-V_{TH} for a 1 GHz input signal of -0.96 dBm power applied to the drain of transistor 2N (biased at zero current), measured at (a) T <250 K (b) $T \geq 250$ K.

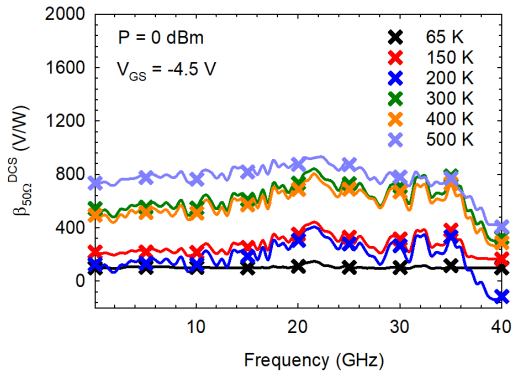

Figure 4.38: $\beta_{\beta_{50\Omega}}^{DCS}$ *vs.* frequency measured in transistor 2N at different temperatures. The applied signal has 0 dBm power. V_{GS} =-4.5 V (subthreshold).

frequency and confirm the theoretical expectations, as already explained in previous subsection 4.2.1.

Gate-coupling scheme

To conclude, we have also characterized the detection capabilities of the transistor as a function of temperature in the GCS. Figure 4.39 shows the detected voltage $\beta_{50\Omega}^{GCS}$ at different temperatures as a function of the drain current bias I_D. As expected, according to the gate-coupling framework explained in subsection 4.2.2, the detected voltage is zero at $I_D = 0$ A, and the dependence on increasing I_D is the same as that observed at room temperature in subsection 4.2.2.

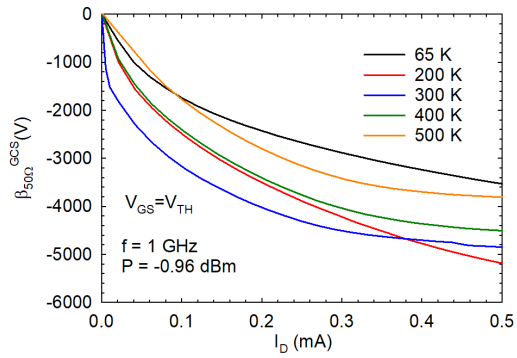

Figure 4.39: $\beta_{50\Omega}^{GCS}$ *vs.* I_D for a 1 GHz input signal of -0.96 dBm power applied to transistor 2N at different temperatures.

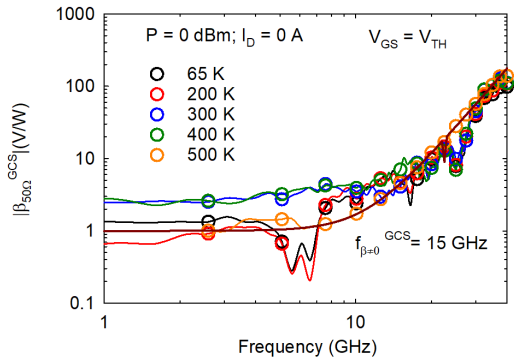

Figure 4.40: $|\beta_{50\Omega}^{GCS}|$ *vs.* frequency in transistor 2N at different temperatures for $I_D = 0$ A and $V_{GS} = V_{TH}$.

Unfortunately, due to the small range of bias current analyzed, we did not reach a maximum in $\beta_{50\Omega}^{GCS}$, as in the measurements performed at room temperature (see Figure 4.33).

When we measure $\beta_{\beta_{50\Omega}}^{GCS}$ as a function of frequency for a bias of $I_D = 0$ A and $V_{GS} = V_{TH}$ at each temperature, we recover, as expected, the behavior of null detected voltage at low frequencies and then a pronounced increase once a certain frequency is reached, as observed in Figure 4.40. The corner frequency $f_{\beta\neq0}^{GCS}$ seems to be temperature independent and takes a value about 20 GHz. We can justify this result based on the elements of S-SSEC involved in this characteristic frequency, R_{gd} and C_{gd} (see Equation 4.37). Since R_{gd} and C_{gd} are not strongly affected by the operating conditions (current and dissipated power levels), as it was found in subsection 4.1.2.2, one can expect that $f_{\beta\neq0}^{GCS}$ is neither significantly affected by the change of temperature.

Conclusions

This work deals with the experimental characterization, Monte Carlo (MC) modeling and analytical study of two types of high-frequency electronic devices based on GaN: Self-Switching Diodes (SSDs) and High-Electron-Mobility Transistors (HEMTs). The main electronic properties of GaN are presented in the introduction, putting special emphasis on two limiting factors to be traps and heating effects due to the relatively novel and immature GaN technology. The fundamentals of the different setups, techniques and particularities of the MC home-made tool have been carefully detailed in the first chapter. Characterized devices have been manufactured at the IEMN (Institut d'Électronique, de Microélectronique et de Nanotechnologie) in Lille (France).

Chapter 2

The main results obtained in this chapter, devoted to the analysis of SSDs and G-SSDs, are the following:

- Trapping effects have been analyzed in AlGaN/GaN SSDs by means of measurements of pulsed current-voltage curves and transient AC impedance. The transient behavior of the zero-bias AC impedance measured just after the application of a voltage pulse of different amplitude and time width allows us to identify and distinguish between electrons trapped or released in surface or bulk states. In the case of diodes with narrow channels, as the surface-to-volume ratio of the device is high, trapping/detrapping of electrons at the states present at the sidewalls of the trenches, originated by the etching process, are found to play a major role. Characteristic times of the order of ms were identified for these processes, being shorter as the voltage amplitude increases. As expected, in the case of wide channels and V-shape diodes, the described phenomena are absent, since surface effects are much less important, and we attribute the anomalies observed in the I-V curve to the influence of both bulk traps and heating effects.

- GaN based SSDs fabricated on SiC substrate were explored extensively as zero-bias detectors, and were confirmed to provide similar performances as those fabricated on Si substrate. First, for a diode with $L = 2\,\mu$m and $W = 100\,$nm, a responsivity of around 26 V/W in the 0.01-43.5 GHz band has been measured. In the G-band (between 140 and 220 GHz), a 20 dB/dec frequency drop-off is observed, with a cutoff frequency of around 200 GHz, along with a square-law response up to 20 dBm of input power. Then, responsivities calculated with a quasi-static (QS) model based on DC measurements were confirmed to correctly reproduce the low-frequency (1 GHz) experiments for different channel widths. Responsivities are in the order of 50 V/W, with a noise equivalent power NEP around 200 pW/Hz$^{1/2}$. This QS estimation of the responsivity constitutes a robust tool for the further optimization of the main figures of merit of the SSDs operating as detectors for, e.g., THz imaging applications. Both the QS model and experiments show an enhancement of the detected voltage under non-zero bias conditions, reaching up to 200 V/W for a biasing of $I = 45\,\mu$A. The optimum detector performance, in terms of minimum NEP, is achieved with an array of SSDs providing a resistance 3 times that of the characteristic impedance of the transmission line to which it is connected. In these conditions the responsivity decreases to 9/16 of its maximum value, obtained for only one diode. The use of a high-impedance transmission line has also been explored as a useful way of improving the detector performances.
- We have also analyzed the on-wafer performance of SSDs as microwave zero-bias detectors in a wide range of temperatures ranging from 10 K to 300 K. Temperature plays a key role: a remarkable enhancement of responsitivy, reaching values of 100 V/W, is found when lowering T for frequencies below 1 GHz, and its sign changes at around 150 K. The increase of the low-frequency responsivity is consistent with the increase of the resistance of the SSD at low temperature, due to a smaller effective width of the channel, which we attribute to the increasing presence of trapped charge at the sidewalls of the trenches. At low temperatues, a pronounced frequency roll-off in the responsivity is observed until reaching a plateau above 5 GHz, at a value which approximately coincides with the responsivity exhibited by the diode at 300 K in the full frequency span. These results have been corroborated by means of the QS model. The inspection of the behavior of the resistance, bowing coefficient and responsivity *vs.* temperature suggests the presence of different kinds (surface and bulk) of traps.

- Gated-SSDs (G-SSDs), fabricated by depositing a Schottky contact gate on the top of the channel, benefit from improvements in the main figures of merit of RF detectors, i.e., responsivity and NEP. Free-space measurements confirm sub-THz (300 GHz) operation with enhanced voltage-controlled responsivity thanks to the top gate. The best values of voltage responsivity and NEP, around 600 V/W and 50 pW/Hz$^{1/2}$, respectively, are achieved when the gate bias approaches the threshold voltage. Once again, the simple QS model is able to predict the role played by the gate bias in the device performance. A good agreement is found between modeled results and those obtained from RF measurements under probes at low frequency (900 MHz) and in free space at 300 GHz.
- The performance of the G-SSD architecture can approach the state-of-the-art of mm-and sub-mm-wave detectors, since the impedance-tunability provided by the voltage control of the characteristics of the device can be combined with additional design efforts aiming to mitigate the strong mismatch presented by these devices. In the responsivity, the width is the most relevant parameter, since a narrower channel provides higher responsivity. The more the number of channels in parallel, the lower the NEP. The use of a high-impedance transmission line is also an option. The deposition of a thin layer of SiN on the top of the AlGaN before the gate fabrication step allows to correctly isolate the gate contact and solve some issues related with the small leakage current through the gate. Very preliminary results revealed a fairly flat frequency response up to 40 GHz with a maximum responsivity of 200 V/W measured at V_{GS} - V_{TH} =-1.1 V for a W = 100 nm G-SSD. The QS model fails in bias conditions close to pinch-off because the estimation of the huge channel resistance from the derivative of very low values of current is problematic within the QS model. Preliminary measurements at different temperatures down to 36 K have evidenced a decrease in the current when lowering the temperature, which can be attributed to the influence of charge trapped at surface states present in the sidewalls of the channel.

Chapter 3

This chapter is devoted to the numerical and experimental analysis of AlGaN/AlN/GaN HEMTs operating under DC conditions. It contains the complete protocol to adjust all the parameters of the MC tool in order to replicate DC measurements. The main results are the following:

- A sheet carrier density $n_s = 1.0{\cdot}10^{13}$ cm^{-2} and an electron mobility $\mu_n = 2022$ cm^2/Vs have been extracted for the heterostructure at room temperature from measurements of TLMs using the 4-wire or Kelvin method. The estimated contact resistance and sheet resistance are 0.28 $\Omega{\cdot}$mm and 302.52 $\Omega_\square$, respectively. Polarization charges, surface states and surface roughness in the MC tool have been adjusted through isothermal simulations by fitting the experimental resistance values for different diodes lengths. Simulations at different ambient temperatures, and also with the TRM, evidence the presence of heating in the measured TLMs.
- Once the simulator has been calibrated, the experimental output and transfer characteristics of transistor number 2 ($L_{DS} = 1.5$ μm, $L_G = 150$ nm) have been replicated. To his end, we have included the effect of the contact resistances and the Schottky barrier, with the values $R_C = 1$ $\Omega{\cdot}$mm and $V_{SCH} = 4.5$ V providing the best agreement between MC results and measurements. However, isothermal simulations are not capable of reproducing entirely the experimental output and transfer curves, and the TRM and ETM have been considered to account for heating effects. As a general conclusion, both thermal models achieve a much better agreement with the experimental DC curves than isothermal simulations. The ETM, apart from providing a map of temperatures inside the device, allows us to extract the proper equivalent thermal resistance, $R_{TH} = 19.25$ mm$\cdot$K/W, to be used in the TRM. ETM and TRM provide practically identical DC curves when this value of R_{TH} is considered in the TRM. The effect of a TBR has also been taken into account within the ETM, with a value of $\sim 15\cdot\ 10^{-8}$ m^{2}K/W. The remaining discrepancies with respect to experimental DC curves are mainly attributed to DIBL effects. The ETM is able to capture the combined effect of V_{DS} and V_{GS} on heating effects in the transistors and it allows locating hot-spots. However, it requires of immense computational resources, not only to deal with the steady-state heat conduction equation (HCE), but also with the detailed layer structure of the thermal domain.
- The differences between continuous DC and pulsed measurements are similar those observed between TRM and isothermal simulations. A simple electrical method in which the the heat-sink temperature is modified allows to extract a thermal resistance of about $\sim$10 mm$\cdot$K/W and estimate the channel temperature based on the difference in drain current between DC and short-pulse (and low duty cycle) conditions overcoming the self-heating of the channel. Van der Pauw measurements in the HEMT heterostructure reveal a reduction of mobility at increasing temperatures, attributed to the more intense action of

scattering. As a consequence, the drain current level of the HEMT progressively decreases when the temperature increases, along with a shift in the V_{TH} attributed to trapping effects.

- The influence of different design parameters on the DC characteristics of HEMTs is beyond the objectives of this work. However, some indications can be provided. In an appendix we have analyzed the influence of L_G and L_{DS} on the performance of the transistors. A strong influence of L_G was found in relevant aspects, as the I_D^{max} level at V_{GS} = 0 V; I_D^{max} takes a lower value (980 A/m) with longer L_G = 150 nm, while in the transistor with L_G = 75 nm, the current takes the value I_D^{max} = 1180 A/m. Regarding the V_{TH}, we observe that it is less negative (-3.4 V) in the transistor with the longer L_G = 150 nm, while the shorter gate (L_G = 75 nm) exhibits a more negative V_{TH} =-4.1 V. Finally, we investigate the behavior of g_m^{max} at V_{DS} = 1 V. In the shorter gate (L_G = 75 nm), it is measured the higher g_m^{max} (340 S/m) at V_{GS} =-3 V, while in the transistor with L_G = 150 nm, g_m^{max} takes the value 320 S/m at V_{GS} =-2.5 V. The influence of L_{DS} is only observed in the slope of I_D at low V_{DS}. Its inverse for V_{GS} = 0 V, R_{ON}, takes higher values in transistors with longer L_{DS}: R_{ON} = 3.5 Ωmm in the transistor with L_{DS} = 4.5 μm, while in the transistor with L_{DS} = 2.5 μm, R_{ON} = 2.8 Ωmm. We conclude that L_G is the most relevant geometrical design parameter in the analyzed transistors.

Chapter 4

This chapter analyzes AlGaN/AlN/GaN HEMTs. Virgin transistors evidencing an anomalous DC and RF behavior have been analyzed. A small-signal equivalent circuit (SSEC) has been determined and the maximum frequencies of operation have been estimated. RF detection capabilities have also been analyzed using drain and gate signal-coupling schemes. Finally, the influence of heating and operation temperature are studied. The main results are the following:

- The intrinsic Y-parameters of the transistors were extracted after properly deembedding the effect of the parasitic resistances, inductances and capacitances thank to measurements of dummy open and short structures. A strong frequency dispersion, accompanied by a high on-resistance value, is evident in virgin devices and is still noticeable when the transistors are biased at low drain current levels. This anomalous effect is irreversibly reduced, but never completely cancelled, when the device is biased at high power conditions. We attribute these effects to the presence of crystal defects in the gate-drain region of the

GaN channel and the ohmic contacts of virgin devices, creating trapping states initially charged with electrons which are progressively released (or defects are repaired) by the applied bias. A simple circuit model, based on incorporating an RC tank to the standard FET equivalent circuit, has been proposed to replicate the observed frequency dispersion.

- MC simulations are also employed to extract the elements of the SSEC, found to be frequency independent up to 100 GHz. MC results are well in the range of the experimental ones. For relatively low drain bias, g_m and C_{gs} are the elements more affected by the bias conditions, while the other elements of the SSEC are practically constant. At elevated dissipated power, significant differences appear in the values of g_m and g_d extracted by the TRM and ETM, mainly originated by the fact that when drain current increases, the average temperature of the ETM always underestimates the temperature provided by the TRM.
- RF measurements have allowed us to determine the influence of the critical dimensions of the transistor in its figures of merit. The longer the gate, the smaller the channel conductance g_d, due to the better control over the current in the device. Concerning the capacitances, C_{gs} increases with the gate length, while C_{gd} remains almost constant. It has been demonstrated that these devices are able to operate at frequencies higher than 100 GHz, with the shorter-gate transistors, as expected, exhibiting the higher cutoff frequencies.
- RF drain- and gate-coupling detection schemes have been implemented, and measurements have been explained in terms of a well-established model based on the lumped elements of the equivalent circuit. When the gate is biased just below the threshold voltage, a peak of 400 V/W is reached in the responsivity under DCS at zero drain current. Under GCS, as predicted by the model, zero responsivity is obtained at low frequencies when $I_D = 0$, since no drain voltage is excited. Interestingly, when the condition $f > 1/(2\pi R_{gd} C_{gd})$ is fulfilled, the gate-to-drain path is short-circuited and an output drain voltage is measured. In contrast to the zero-current case, a huge enhancement (also at low frequency) is obtained when sourcing drain current at 1.2 mA, where the responsivity reaches a maximum of almost 4 kV/W, one order of magnitude higher than in DCS. Both configurations show a -3 dB roll-off at about 20-40 GHz. The last collection of measurements were done inside the LakeShore CRX-VF cryo-probe station. Two ranges of temperature where identified in the DCS. When entering the subthreshold region by decreasing V_{GS}, for T$<$250 K the responsivity decreases abruptly after reaching its maximum value, while for T $>$ 250 K it remains almost constant with the gate bias. For GCS, the results follow the same trend

as at 300 K and hardly depend on temperature. This is attributed with the fact that C_{gd} is constant in a broad range of V_{GS}.

Future outlook

This thesis presents measurements contributing to the progress of GaN SSDs (with or without gate) and AlGaN/GaN HEMTs operating as microwave detectors. In addition, DC and AC Monte Carlo simulations of transistors, including thermal effects, provide insight into the related physics and feedback to the technology. Throughout the manuscript we have suggested some ideas and possible improvements that, either due to lack of time or because they were beyond the scope and objectives of this work, could not be addressed in detail. We collect them here as future research lines:

- Trapping effects in SSDs should be analyzed in more detail at low temperatures. Impedance and noise measurements could provide much more information about the kind of traps present in the devices and their energy location.
- V-shape SSDs may be potential candidates to generate Gunn oscillations. Measurements of S_{11} and noise power density are very appropriate characterization techniques to confirm the expectations.
- The hysteresis found in the SSDs of Run 2 could be used for memory applications.
- The on-wafer frequency range of the equipment available in the laboratory is 43.5 GHz, below the upper frequency limit of operation of many of the devices characterized in this thesis. Extending the measurements up to higher frequencies would allow to compare the performance between the different devices (SSDs, G-SSDs and HEMTs) and corroborate the enhancements predicted by the optimization of their geometries.
- In the HEMTs, the MC model has not been able to fit the the experimental curves when the channel is almost closed. Including a p-type doping in the GaN layer of the heterostructure would help to reduce short-channel effects and reproduce the experimental results.
- Electrothermal simulations changing the heat-sink temperature would help to understand more deeply self-heating effects.
- From the point of view of experiments, the method to extract the thermal resistance could be improved and compared with other techniques.
- The small-signal equivalent circuit has been measured only at room temperature. Next step will be to use the new cryogenic probe station to study the impact of temperature and bias conditions. For that purpose, the S-parameter

calibration would require more time and knowledge about its dependence on temperature.

- The characterization of the transistor as an amplifier is part of the future work, for example measuring the 1 dB compression point or the PAE.
- The issues concerning the the excess of energy of electrons reaching the drain contact within the ETM at high V_{DS} need to be solved. Once done, the possible differences between the parameters of the equivalent circuit extracted with the ETM and the TRM could be identified.
- Microwave detection with the HEMT in DCS and GCS needs to be analyzed in more detail, especially the influence of temperature under sub-threshold bias conditions.

Conclusiones

Este trabajo presenta la caracterización experimental, el modelado Monte Carlo (MC) y el estudio analítico de dos tipos de dispositivos electrónicos de alta frecuencia basados en GaN: diodos autoconmutantes (SSDs) y transistores de alta movilidad de electrones (HEMTs). Las características eléctricas más relevantes del GaN se presentan en la introducción, poniendo especial énfasis en dos factores limitantes como son las trampas y los efectos de calentamiento debidos a la relativa novedad e inmadurez de la tecnología de GaN. Los fundamentos de los diferentes montajes, técnicas y particularidades de la herramienta MC se detallan en el primer capítulo. Los dispositivos medidos se han fabricado en el IEMN (Institut d'Électronique de Microélectronique et de Nanotechnologie), en Lille (Francia).

Capítulo 2

Los principales resultados obtenidos en este capítulo, dedicado al análisis de SSDs y G-SSDs, son los siguientes:

- Se han analizado efectos de trampas en SSDs de AlGaN/GaN mediante medidas pulsadas de curvas corriente-voltaje y transitorios de impedancia AC. El comportamiento transitorio de la impedancia AC en polarización nula medido tras aplicar un pulso de voltaje con diferente amplitud y duración temporal permite identificar y distinguir electrones atrapados y liberados por los estados superficiales y volúmicos. En el caso de diodos con canales estrechos, puesto que la relación superficie-volumen es alta, la captura/emisión de electrones por parte de los estados presentes en las paredes de las zanjas, originados durante el proceso de grabado, juegan un papel muy relevante. Como es de esperar, en el caso de canales anchos y diodos con forma de V, estos fenómenos están ausentes, puesto que los efectos superficiales son mucho menos importantes y las anomalías observadas en la curva I-V son atribuidas a efectos volúmicos y de calentamiento.

- Se ha estudiado el comportamiento de SSDs de GaN fabricados sobre sustratos de SiC como detectores a polarización nula de señales de microondas y se ha confirmado que proporcionan resultados similares a los fabricados sobre Si. En primer lugar se midió un diodo con $L = 2\,\mu$m y $W = 100\,$nm, que muestra una responsividad de 26 V/W en la banda 0.01-43.5 GHz. En la banda G (entre 140 y 220 GHz), se observa una caída de 20 dB/dec, con una frecuencia de corte en torno a 200 GHz, junto a una respuesta cuadrática hasta 20 dBm de potencia de entrada. Después se calcularon responsividades mediante el modelo cuasi estático (QS), basado en medidas DC, que reproducen los resultados de baja frecuencia (1 GHz) para distintas anchuras del canal. Las responsividades están en el orden de 50 V/W, con una potencia equivalente del ruido (NEP) en torno a 200 pW/Hz$^{1/2}$. Esta estimación del modelo QS es una herramienta muy útil para una posterior optimización de las figuras de mérito del SSD como detector, por ejemplo en aplicaciones de realización de imágenes en THz. Tanto los resultados QS como los experimentos muestran una mejora del voltaje detectado en condiciones de polarización distinta de cero, alcanzando hasta 200 V/W para una polarización de $I = 45\ \mu$A. El mejor funcionamiento en términos de menor NEP se obtiene con una matriz de SSDs que presenta una resistencia 3 veces menor que la característica de la línea a que están conectados. En tales condiciones la responsividad decrece a 9/16 del máximo, obtenido para un único diodo. Asimismo se ha estudiado el uso de una línea de transmisión de alta impedancia para mejorar el funcionamiento del detector.
- También se han analizado los SSDs como detectores a polarización nula en un amplio rango de temperaturas entre 10 K y 300 K. La temperatura juega un papel importante. Se encuentra un aumento de la detección a frecuencias menores que 1 GHz cuando disminuye la temperatura, alcanzando 100 V/W, y su signo cambia a 150 K. El aumento de la responsividad a baja frecuencia es consistente con el aumento de la resistencia del SSD a baja temperatura, por la menor anchura efectiva del canal, que atribuimos a la presencia de cargas atrapadas en la paredes de las zanjas. A bajas temperaturas se encuentra que el voltaje detectado cae al aumentar la frecuencia hasta alcanzar un valor constante a partir 5 GHz, que coincide con la responsividad del diodo a 300 K en todo el rango de frecuencias. Estos resultados se han corroborado con el modelo QS. El comportamiento de la resistencia, el coeficiente de curvatura y la responsividad frente a la temperatura sugiere la presencia de diferentes tipos de trampas (en superficie y volumen).

- SSDs con puerta (G-SSDs) fabricados depositando un contacto Schottky sobre el canal mejoran las principales figuras de mérito de los detectores (responsividad y NEP). Medidas realizadas en espacio libre confirman el funcionamiento de estos dispositivos a frecuencias de sub-THz (300 GHz), con una responsividad mejorada, controlada en voltaje gracias a la puerta. Los mejores valores de responsividad y NEP, en torno a 600 V/W y 50 pW/Hz$^{1/2}$ respectivamente, se obtienen cuando la puerta se polariza cerca del umbral. De nuevo, el modelo QS consigue predecir el papel del voltaje de puerta en el funcionamiento del dispositivo. Se obtiene un buen ajuste entre los resultados del modelo y los obtenidos en medidas RF con puntas a baja frecuencia (900 MHz) y en espacio libre a 300 GHz.
- Las prestaciones de los G-SSDs se pueden aproximar a las del estado del arte de detectores milimétricos y submilimétricos, puesto que el control sobre la impedancia proporcionado el voltaje de puerta puede ser combinado con esfuerzos adicionales por mitigar la desadaptación presente en estos dispositivos. En la responsividad, la anchura es el parámetro más relevante, dado que con un canal más estrecho se obtiene una responsividad mayor. Cuanto mayor sea el número de canales en paralelo, menor es la NEP. También existe la opción de usar de una línea de transmisión de alta impedancia. La deposición de una capa de AlN sobre el AlGaN antes de la fabricación de la puerta permite aislarla y resolver algunos problemas relacionados con fugas de corriente. Resultados preliminares revelan una respuesta plana en frecuencia hasta 40 GHz con una responsividad máxima de 200 V/W, medida para $V_{GS} - V_{TH}$ =-1.1 V en un G-SSD con W = 100 nm. El modelo QS falla en condiciones de polarización cercanas al umbral, porque la estimación de la enorme resistencia del canal a partir de la derivada de valores muy bajos de corriente es problemática en este modelo. Se han realizado medidas preliminares a diferentes temperaturas desde 36 K que evidencian una caída de la corriente al bajar la temperatura, que se puede atribuir a la influencia de cargas atrapadas en estados superficiales presentes en las paredes del canal.

Capítulo 3

Este capítulo está dedicado al anślisis numérico y experimental de HEMTs de AlGaN/AlN/GaN en condiciones de operación DC. Contiene el protocolo completo de ajuste de los parámetros de la herramienta MC para reproducir las medidas DC. Los principales resultados son los siguientes:

- La densidad superficial de portadores $n_s = 1.0 \cdot 10^{13}$ cm^{-2} y la movilidad electrónica $\mu_n = 2022$ cm^2/Vs de la heteroestructura se han extraído a temperatura ambiente a partir de medidas de TLMs con el método de 4 puntas o Kelvin. La resistencia de contacto es 0.28 $\Omega \cdot$mm y la resistencia de capa 302.52 $\Omega_\square$. Hemos ajustado las cargas superficiales de la heterounión, los estados superficiales y la rugosidad superficial para calibrar de forma satisfactoria la herramienta MC a través simulaciones isotérmicas que reproducen las resistencias experimentales medidas en diodos con diferente longitud. Las simulaciones a diferentes temperaturas ambiente con el modelo de resistencia térmica muestran la presencia de efectos térmicos en los TLM medidos.
- Una vez validado el simulador, se han reproducido las curvas experimentales del transitor 2N ($L_G = 150$ nm, $L_{DS} = 1.5$ μm y $W = 2 \times 25$ μm). Para ello, hemos incluido el efecto de la resistencia de los contactos y la barrera Schottky, siendo los valores que proporcionan el mejor acuerdo entre el modelo MC y las medidas experimentales $R_C = 1$ $\Omega \cdot$mm y $V_{SCH} = 4.5$ V. Sin embargo, las simulaciones isotérmicas no son capaces de reproducir por completo el comportamiento DC de las curvas de salida y transferencia. En consecuencia, se han implementado en el simulador dos técnicas autoconsistentes para incluir efectos de calentamiento: (i) el método de la resitencia térmica (TRM) y (ii) el modelo electrotérmico (ETM), en el que se resuelve la ecuación de conducción de calor independiente del tiempo. El ETM nos permite determinar el valor más apropiado de la resistencia térmica para nuestros dispositivos, $R_{TH} = 19.25$ mm·K/W. Además, se ha considerado el efecto de una barrera térmica (TBR) entre la capa de GaN del canal y el sustrato de valor $\sim 15 \cdot 10^{-8}$ m^{2}K/W. Como conclusión general, ambos modelos muestran un mejor acuerdo con los resultados experimentales que las simulaciones isotérmicas. Las discrepancias observadas en los valores de la corriente máxima y el voltaje umbral los atribuimos a que en las simulaciones no es posible cerrar completamente la conducción en el canal por el denominado efecto de disminución de la barrera inducido por el drenador (DIBL). Encontramos los siguientes pros y contras del ETM respecto al TRM. EL ETM es capaz de capturar el efecto combinado de los voltajes puerta-fuente y drenador-fuente en el calentamiento de los transistores y además permite localizar los puntos calientes dentro del HEMT. Sin embargo, requiere muchos recursos computacionales tanto para resolver la ecuación de conducción de calor como para tener en cuenta la estructura de capas completa del dominio térmico.
- Las diferencias entre las medidas DC y pulsadas son similares a las observadas entre los resultados obtenidos con el simulador empleando el TRM y si-

mulaciones isotérmicas. Un método eléctrico simple en el que se modifica la temperatura ambiente de la medida permite extraer una resistencia térmica del orden de 10 mm·K/W y estimar la temperatura del canal, basándose en la diferencia entre la corriente de drenador medida en condiciones DC y pulsadas (con pulsos cortos y bajo *duty cycle*) que mitigan el autocalentamiento del canal. Medidas van der Pauw revelan una reducción de la movilidad a altas temperaturas atribuida a la mayor intensidad de los mecanismos de scattering. Como consecuencia de todo ello, el nivel de corriente de drenador del HEMT va disminuyendo progresivamente cuando aumenta la temperatura, observándose también un desplazamiento en la tensión umbral.

- El estudio de la influencia de las dimensiones del transistor está fuera del objetivo de este trabajo. Sin embargo, se pueden proporcionar algunas indicaciones. En un apéndice hemos analizado la influencia de L_G y L_{DS} en el funcionamiento de los transistores. Se encuentra un importante efecto de L_G en aspectos relevantes como el nivel máximo de corriente de drenador a V_{GS} = 0 V, que toma un valor menor (980 A/m) para mayor L_G (150 nm), mientras que en el transistor con L_G = 75 nm, el valor es de 1180 A/m. Por lo que respecta a la tensión umbral, V_{TH} es menos negativa (-3.4 V) para una L_G más larga, mientras que para L_G = 75 nm el valor es -4.1 V . Finalmente, analizamos el comportamiento de la transconductancia. Aunque no se observa una gran diferencia en el máximo de g_m, para la puerta más corta (L_G = 75 nm) se mide una mayor g_m (340 S/m a V_{GS}=-3 V). La influencia de L_{DS} sólo se observa en la pendiente de I_D a valores bajos de V_{DS}. Su inversa a V_{GS} = 0 V, R_{ON}, toma valores más altos (3.5 Ωmm) en el transistor de mayor L_{DS} (4.5 μm), mientras que el transistor con L_{DS} = 2.5 μm muestra una R_{ON} de 2.8 Ωmm. Por lo tanto, concluimos que L_G es el parámetro geométrico más importante en el diseño de estos transistores.

Capítulo 4

Este capítulo analiza el funcionamiento en RF de HEMTs de AlGaN/AlN/GaN. Se han estudiado transitores vírgenes que muestran un comportamiento anómalo en DC y RF. Se ha determinado un circuito equivalente de pequeña señal (SSEC) y se han estimado las frecuencias máximas de operación. Se ha estudiado la capacidad para detectar de estos transistores usando los esquemas de acoplamiento en puerta (GCS) y drenador (DCS). Finalmente, se analiza la influencia del calentamiento y la temperatura de operación. Los resultados más importantes son:

- Los parámetros Y de los transistores han sido extraídos tras desembeber los efectos parásitos de resistencias, inductancias y capacidades mediante medidas realizadas en *dummies* de corctocircuito y circuito abierto. Se observa una dispersión en frecuencia muy significativa en dispositivos vírgenes (acompañada de un alto valor de la resistencia) que es todavía apreciable tras polarizar los transistores a niveles de corriente bajos. Este efecto anómalo es irreversiblemente reducido, pero nunca completamente cancelado, cuando el dispositivo se polariza en condiciones de alta potencia. Atribuimos estos efectos a la presencia de defectos cristalinos en la región puerta drenador del canal de GaN y en los contactos óhmicos de los dispositivos vírgenes, que crean trampas inicialmente cargadas con electrones que progresivamente desaparecen (o los defectos son reparados) con la polarización aplicada. Se propone un modelo simple de SSEC, incorporando un tanque RC al SSEC estándar del FET, para replicar la dispersión observada.
- Se emplean simulaciones MC para extraer los elementos del SSEC y se encuentra que son independientes de la frecuencia hasta 100 GHz. Los resultados MC están en el rango de los experimentales. Para una polarización relativamente baja, g_m y C_{gs} son los elementos más afectados por las condiciones de polarización, mientras que el resto son prácticamente constantes. A alta potencia disipada aparecen diferencias significativas en los valores de g_m y g_d extraídos mediante el ETM y el TRM, principalmente originados por el hecho de que al aumentar la corriente de drenador, la temperatura media del ETM siempre infraestima la proporcionada por el TRM.
- La medidas RF nos han permitido determinar la influencia de las dimensiones críticas del transistor en sus figuras de mérito. Cuanto mayor es la puerta, menor es la conductancia del canal g_d, debido al mejor control sobre la corriente en el dispositivo. En lo que respecta a las capacidades, C_{gs} aumenta con la longitud de puerta, mientras C_{gd} permanece prácticamente constante. Se ha demostrado que estos dispositivos son capaces de operar hasta frecuencias mayores que 100 GHz, mostrando mayores frecuencias de corte los transistores con puerta más corta, como cabe esperar.
- Han sido implementados esquemas de detección con acoplamiento de la señal en puerta y drenador. Las medidas se han interpretado a partir de un modelo bien establecido, basado en los elementos discretos del circuito equivalente. Cuando se polariza la puerta justo en el voltaje umbral, se alcanza un pico de 400 V/W bajo DCS en condiciones de corriente nula. Operando en GCS y como predice el modelo, se obtiene responsividad nula a bajas frecuencias cuando la polarización

en corriente es cero, puesto que no se excita ninguna corriente de drenador. Sin embargo, bajo la condición $f > 1/(2\pi R_{gd}C_{gd})$, el camino puerta-drenador queda cortocircuitado y se puede medir un voltaje de salida. Se obtiene un gran crecimiento en responsividad (también a baja frecuencia) cuando se polariza con una corriente de drenador de 1.2 mA, donde la responsividad alcanza un máximo de 4 kV/W, un orden de magnitud mayor que en DCS. Ambas configuraciones muestran una caída de 3 dB en torno a 20-40 GHz. La última colección de medidas se realizó en la mesa criogénica LakeShore CRX-VF. Se identifican dos rangos de temperatura en DCS. Cuando el dispositivo se adentra en subumbral disminuyendo V_{GS}, si T $<$ 250 K la responsividad disminuye abruptamente tras alcanzar un máximo, mientras que para T $>$ 250 K se mantiene constante con la polarización de puerta. Para GCS los resultados siguen la misma tendencia que a 300 K y apenas dependen de la temperatura. Esto se atribuye al hecho de que C_{gd} es constante en un amplio rango de V_{GS}.

Líneas futuras

Esta tesis presenta medidas que contribuyen al progreso de las prestaciones de SSDs de GaN (con y sin puerta) y HEMTs de AlGaN/GaN operando como detectores de microondas. Además, las simulaciones MC, tanto de DC como de AC e incluyendo efectos térmicos, dan una visión profunda de la física involucrada y proporcionan una realimentación sobre la calidad de la tecnología. A lo largo del manuscrito hemos sugerido numerosas ideas como posibles mejoras del trabajo que, debido a la falta de tiempo o a que se encuentran más allá de los objetivos, no han podido ser desarrolladas en detalle. Las recogemos aquí como posible líneas de investigación futuras:

- Los efectos de trampas en los SSDs a bajas temperaturas deberían ser analizados más en detalle. Medidas de impedancia y ruido pueden proporcionar mucha información sobre el tipo de trampas presentes en los dispositivos y su localización en energía.
- Los diodos en forma de V son candidatos potenciales para generar oscilaciones Gunn. Las medidas de S_{11} y de densidad espectral del ruido son técnicas de caracterización muy apropiadas para confirmar estas expectativas.
- La histéresis encontrada en los SSDs del Run 2 puede ser usada en aplicaciones de memoria.
- El rango experimental del laboratorio para medidas sobre oblea llega hasta 43.5 GHz, por debajo de la frecuencias límite de operación de muchos de los dispositivos estudiados. Extender las medidas hasta frecuencias más altas per-

mitiría comparar el funcionamiento de SSDs, G-SSDs y HEMTs y corroborar las mejoras previstas a partir de la optimización de su geometría.

- En los HEMTs, el modelo MC no ha sido capaz de reproducir las medidas experimentales cuando el dispositivo está prácticamente cortado. Se deben realizar simulaciones incluyendo un dopaje tipo p en la capa de GaN de la heteroestructura, lo que ayudará a reducir los efectos de canal corto y a reproducir los resultados experimentales.
- Simulaciones electrotérmicas cambiando la temperatura del foco térmico permitirían una comprensión más profunda de los efectos de calentamiento.
- Desde el punto de vista experimental, el método para extraer la resistencia térmica podría ser mejorado y comparado con otras técnicas.
- El circuito equivalente de pequeña señal se ha medido sólo a temperatura ambiente. El siguiente paso será usar la nueva estación criogénica de puntas para estudiar el impacto de la temperatura y las condiciones de polarización. Para ello se requiere un mayor conocimiento acerca de la calibración para medir parámetros S y su dependencia con la temperatura.
- Caracterizar el transistor como amplificador es parte del futuro trabajo, por ejemplo para medir el punto de compresión a 1 dB y la PAE.
- Los problemas relacionados con el exceso de energía de los electrones que alcanzan el drenador encontrados en el contexto del ETM a voltajes altos deben ser resueltos. Una vez logrado, se podrían identificar posibles diferencias entre los parámetros del circuito equivalente extraídos con el ETM y el TRM.
- La detección de señales de microondas con los HEMTs en los esquemas DCS y GCS debe ser analizada con mayor detalle, prestando especial atención a la influencia de la temperatura en condiciones de polarización subumbral.

Appendix A

Influence of the Geometry

This appendix reports the DC current-voltage characteristics of several transistors that were not shown in Chapters 3 and 4. Although beyond the scope of this work, providing some information about the influence of the geometrical design parameters on the transistor DC performance is quite useful for the discussion of the results included in this dissertation, so that we estimate that this analysis is of interest.

In Chapter 3, we presented the devices available in the wafer, in particular transistors and TLMs with different geometries. The characteristics of several of them have already been shown to illustrate the discussions in the previous chapters, but many others with different features have not been reported. In Table A.1 we indicate the geometries selected to characterize the transistors in this appendix, trying to ensure that we cover the variations of all the available geometrical parameters. We have chosen eight transistors with two widths (W), two drain-to-source lengths (L_{DS}) and two gate lengths (L_G).

Name	W (μm)	L_G (nm)	L_{DS} (μm)
6N	2×25	150	2.5
8N	2×25	75	2.5
14N	2×25	150	4.5
16N	2×25	75	4.5
6W	2×50	150	2.5
8W	2×50	75	2.5
14W	2×50	150	4.5
16W	2×50	75	4.5

Table A.1: Dimensions of the transistors characterized in the wafer.

A.1. Influence of gate length

In this section, the influence of the gate length on the DC characteristics is analyzed. In Figure A.1(a) and (b), we plot the output and transfer characteristics of transistors 6N and 8N, respectively, which differ only in the gate length (150 nm in transistor 6N and 75 nm in transistor 8N). The main differences are related to enhanced short-channel effects in transistor 8N, with shorter gate length. In the output characteristics [see Figure A.1(a)], a difference in the maximum current is evidenced. In transistor 6N a lower maximum current (980 A/m for V_{GS} = 0 V) is measured and the saturation is more pronounced than in transistor 8N (1120 A/m maximum current). Difficulties to pinchoff the channel for high V_{DS} are also observed in transistor 6N. In the transfer characteristics shown in Figure A.1(b), a shift in V_{TH} towards more negative values is observed when the gate is shortened. V_{TH} =-3.4 V for V_{DS} = 1 V in transistor 6N, while V_{TH} =-4.1 V for V_{DS} = 1 V in transitor 8N. As well known, this fact evidences the more efficient control on carrier concentration in the channel achieved with a longer gate.

The previous tendencies are also present in the transconductance, shown in Figure A.2. Drain-induced barrier lowering (DIBL) can be observed in both transistors, more pronounced in the 8N, as corresponds to its shorter gate. Moreover, there is a shift in the value of V_{GS} at which g_m^{max} is located. In transistor 6N, with longer gate, this maximum can be found at V_{GS} =-2.5 V (V_{DS} = 1 V), while in transistor 8N the maximum is located at V_{GS} =-3.0 V (V_{DS} = 1 V), a similar shift to that found in V_{TH}. For not so short gate-lengths, and since transistors are not scaled in the vertical direction, no substantial differences in the maximum values of g_m are

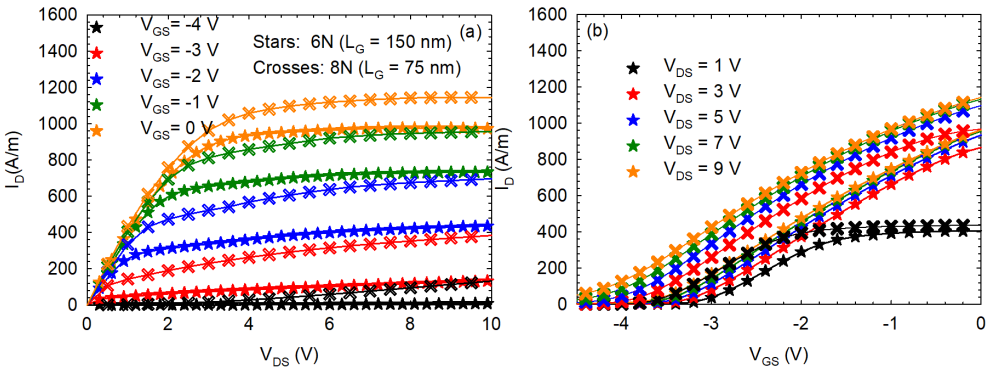

Figure A.1: (a) Output and (b) transfer characteristics measured in two transistors with the same L_{DS} (2.5 μm) and different L_G (150 nm in transistor 6N and 75 nm in transistor 8N).

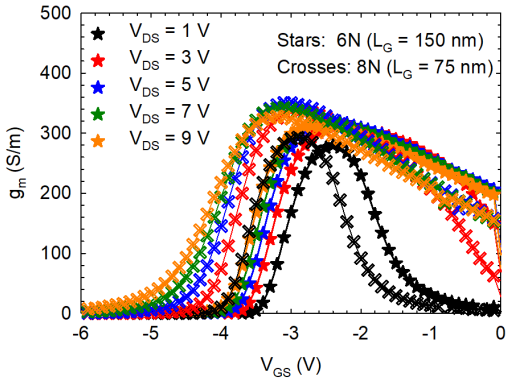

Figure A.2: Transconductance measured in two transistors with the same L_{DS} (2.5 μm) and different L_G (150 nm in transistor 6N and 75 nm in transistor 8N).

expected. Anyway, for all the values of V_{DS}, g_m^{max} is slightly higher in the transistor with L_G = 75 nm. For example, at V_{DS} =-1 V, g_m^{max} = 340 S/m in transistor 8N, while g_m^{max} = 320 S/m in transistor 6N.

A.2. Influence of the drain-to-source length

In this section, the influence of the drain-to-source length on the DC behavior is studied. The output and transfer characteristics of transistors differing only in L_{DS} are compared in Figure A.3, in particular, transistor 6N with L_{DS} = 2.5 μm and transistor 14N with L_{DS} = 4.5 μm, both with L_G= 150 nm. The main influence of L_{DS} is expected at the lower values of V_{DS}, in the linear region of the output characteristics, shown in Figure A.3(a). The measurements confirm this prediction. The slope of the output characteristics in transistor 6N is higher than that of transistor 14N. The inverse of the slope for V_{GS} = 0 V is called R_{ON}. Thus, R_{ON} = 3.5 Ω·mm in transistor 14N (L_{DS} = 4.5 μm), higher than in transistor 6N (L_{DS} = 2.5 μm), where R_{ON} = 2.8 Ω·mm. Despite the differences at low V_{DS}, the level of current reached in the saturation region is similar in both transistors, around 980 A/m. Figure A.3(b) shows the corresponding transfer characteristics. There are not significant differences in the threshold voltage of both transistors (around -3.5 V at V_{DS} = 1 V), but we can observe some differences in the current measured at V_{GS} >-2 V and V_{DS} < 4 V, due to the difference previously mentioned in R_{ON}.

These tendencies are also observed in the transconductance, shown in Figure A.4. In the saturation region, the behavior and maximum value of g_m (around 320 S/m) are similar in both transistors. However, for V_{DS} < 4 V in the linear region, a shift is

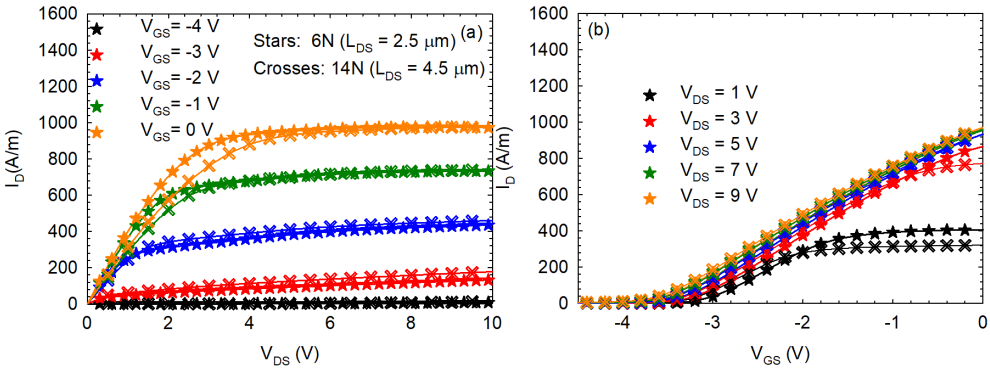

Figure A.3: (a) Output and (b) transfer characteristics measured in two transistors with the same L_G (150 nm) and different L_{DS} (2.5 μm in transistor 6N and 4.5 μm in transistor 14N).

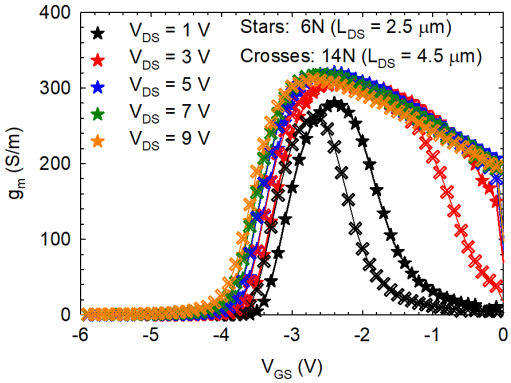

Figure A.4: Transconductance measured in two transistors with the same L_G (150 nm) and different L_{DS} (2.5 μm in transistor 6N and 4.5 μm in transistor 14N).

observed in the maximum of g_m, which takes a higher value for the shorter L_{DS} due to the lower R_{ON}. From these results, it can be concluded that the gate length (L_G) is the most important geometrical parameter, since it leads to the most relevant changes in the current levels. This conclusion can also be applied to the results obtained in the RF operation of the transistors (see sections 4.1.3 and 4.1.4).

Appendix B

Publications and Conference Contributions

Publications

Some of the results presented in this work have been published in the following scientific international journals:

- **H. Sánchez-Martín**, Ó. García-Pérez, S. Pérez, P. Altuntas, V. Hoel, S. Rennesson, Y. Cordier, T. González, J. Mateos and I. Íñiguez-de-la-Torre, "Anomalous DC and RF behavior of virgin AlGaN/AlN/GaN HEMTs", *Semiconductor Science and Technology*, vol. 32, no. 3, pp. 035011, Feb. 2017.
- **H. Sánchez-Martín**, J. Mateos, J. A. Novoa, J. A. Delgado-Notario, Y. M. Meziani, S. Pérez, H. Theveneau, G. Ducournau, C. Gaquière, T. González and I. Íñiguez-de-la-Torre, "Voltage controlled sub-THz detection with gated planar asymmetric nanochannels", *Applied Physics Letters*, vol. 113, no. 4, pp. 043504, Jul. 2018.
- **H. Sánchez-Martín**, S. Sánchez-Martín, I. Íñiguez-de-la-Torre, S. Pérez, J. A. Novoa, G. Ducournau, B. Grimbert, C. Gaquière, T. González and J. Mateos, "GaN nanodiode arrays with improved design for zero-bias sub-THz detection", *Semiconductor Science and Technology*, vol. 33, no. 9, pp. 095016, Aug. 2018.

Moreover, two new contributions have been submitted for publication at the end of this work:

- E. Pérez-Martín, T. González, D. Vaquero, **H Sánchez-Martín**, C. Gaquière, V. J. Raposo, J. Mateos and I. Íñiguez-de-la-Torre,"Trap-related frequency dispersion of zero-bias microwave responsivity at low temperature in GaN-based self-switching diodes", *IOP Nanotechnology*, submitted Apr. 2020.

- E. Pérez-Martín, T. González, D. Vaquero, **H Sánchez-Martín**, C. Gaquière, V. J. Raposo, J. Mateos and I. Íñiguez-de-la-Torre,"Analysis of trap states in AlGaN/GaN self-switching diodes via impedance measurements", *Microelectronics Reliability*, submitted May 2020.

Conference contributions

Some of these results have been presented in the following communications at national and international conferences:

- **H. Sánchez-Martín**, Ó. García-Pérez, I. Íñiguez-de-la-Torre, S. Pérez, T. González, J. Mateos, P. Altuntas, N. Defrance, M. Lesecq, V. Hoel, Y. Cordier and S. Rennesson, "Characterization and modeling of traps and RF frequency dispersion in AlGaN/AlN/GaN HEMTs", *2016 11th European Microwave Integrated Circuits Conference (EuMIC 2016)*, London, U. K. (2016). **Oral Presentation**.
- **H. Sánchez-Martín**, Ó. García-Pérez, I. Íñiguez-de-la-Torre, S. Pérez, J. Mateos, T. González and C. Gaquière, "Geometry and bias dependence of trapping effects in planar GaN nanodiodes", *2017 Spanish Conference on Electron Devices (CDE 2017)*, Barcelona (2017). **Oral Presentation**.
- **H. Sánchez-Martín**, S. Sánchez Martín, Ó. García-Pérez, S. Pérez, J. Mateos, T. González, I. Íñiguez-de-la-Torre and C Gaquière, "Microwave detection up to 43.5 GHz by GaN nanodiodes: Experimental and analytical responsivity", *2017 Spanish Conference on Electron Devices (CDE 2017)*, Barcelona (2017). **Oral Presentation**.
- S. Sánchez-Martín, **H. Sánchez-Martín**, J. A. Novoa, S. Pérez, J. Mateos, T. González, I. Íñiguez-de-la-Torre and C. Gaquière, "Detection enhancement by gate control in GaN nanodiodes", *20th International Conference on Electron Dynamics in Semiconductors, Optoelectronics and Nanostructures (EDISON 20)*, Buffalo, USA (2017). **Oral Presentation**.
- **H. Sánchez-Martín**, E. Pérez-Martín, P. Altuntas, V. Hoel, S. Rennesson, Y. Cordier, J. A. Novoa, S. Pérez, T. González, J. Mateos and I. Íñiguez-de-la-Torre, "Analysis of microwave detection with GaN HEMTs under RF probes", *2018 Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe (WOCSDICE 2018)*, Bucharest, Romania (2018). **Oral Presentation**.
- **H. Sánchez-Martín**, N. Defrance, C. Gaquière, J. Mateos, T. González and I. Íñiguez-de-la-Torre, "Gated GaN nanodiodes for enhanced THz detection", *2018 Spanish Conference on Electron Devices (CDE 2018)*, Salamanca (2018). **Oral Presentation**.

- **H. Sánchez-Martín**, I. Íñiguez-de-la-Torre, J. Mateos and T. González, "Electro-thermal modelling of AlGaN/GaN HEMTs: from DC to equivalent circuit parameters", *2018 Spanish Conference on Electron Devices (CDE 2018)*, Salamanca (2018). **Poster Presentation**.
- J. A. Novoa, Y. Lechaux, J. A. Delgado-Notario, V. Clerico, E. Diez, **H. Sánchez-Martín**, B. G. Vasallo, I. Íñiguez-de-la-Torre, J. Mateos, S. Pérez and T. González, "Fabrication Process of Non-Linear Planar Diodes Based on GaN", *2018 Spanish Conference on Electron Devices (CDE 2018)*, Salamanca (2018). **Poster Presentation**.
- E. Pérez-Martín, D. Vaquero, **H. Sánchez-Martín**, C. Gaquière, T. González, J. Mateos and I. Íñiguez-de-la-Torre, "Temperature dependence of microwave responsivity in GaN-based self-switching diodes", *21st International Conference on Electron Dynamics in Semiconductors, Optoelectronics and Nanostructures (EDISON 21)*, Nara, Japan (2019). **Poster Presentation**.
- J. Mateos, E. Pérez-Martín, **H. Sánchez-Martín**, G. Paz, J. A. Novoa, S. Pérez, N. Defrance, C. Gaquière, G. Ducournau, T. González and I. Íñiguez-de-la-Torre, "Temperature dependence of microwave responsivity of gated and ungated self-switching diodes based on GaN", *9th Asia-Pacific Workshop on Widegap Semiconductors (APWS 2019)*, Okinawa, Japan (2019). **Oral Presentation**.
- E. Pérez-Martín, D. Vaquero, **H. Sánchez-Martín**, C. Gaquière, V. J. Raposo, T. González, J. Mateos and I. Íñiguez-de-la-Torre, "Analysis of trap states in AlGaN/GaN self-switching diodes via impedance measurements", *31st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2020)*, Athens, Greece (2020). **Oral Presentation**.

Research stay

A research stay of three months (16/04/2018-16/07/2018) was carried out at the Institut d'Électronique de Microélectronique et de Nanotechnologie (IEMN), University of Lille, Villeneuve d'Ascq, (France) through Programa IV: ayuda de movilidad del personal inverstigador of the University of Salamanca.

Financial assistance and research projects

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the University of Salamanca, recognized as Consolidated Research Unit by the Junta de Castilla y León, in the context of the following research projects:

- Nanoelectrónica de gap ancho y estrecho para la mejora de la eficiencia en aplicaciones de RF y THz (TEC2013-41640-R). Ministerio de Economía y Competitividad (MINECO).
- Estudio de efectos térmicos en dispositivos de RF. Modelado y caracterización experimental (SA052U13). Consejería de Educación de la Junta de Castilla y León.
- Emisores y detectores de terahercios basados en nanodiodos semiconductores para comunicaciones e imagen médica y de seguridad (SA022U16). Consejería de Educación de la Junta de Castilla y León.
- Tecnologías de diodos de GaN para generación y detección en la banda de subterahercios (TEC2017-83910-R). Ministerio de Economía y Competitividad (MINECO).
- Simulación y caracterización de efectos electrotérmicos en dispositivos de subterahercios para comunicaciones de alta velocidad (SA254P18). Consejería de Educación de la Junta de Castilla y León.

Equipment

The experimental results presented in this work were obtained in the RF Devices Laboratoty of USAL-NANOLAB (Laboratory of Nanoelectronics and Nanomaterials of the University of Salamanca), sited in the Edifcio Multiusos I+D+i. The following equipment was employed:

- Cascade M150 probe station
- Keithley 4200-SCS semiconductor analyzer
- Agilent PNA-X N5244 vector network analyzer
- LakeShore CRX-VF cryogenic probe station
- Agilent B2902A source/measure unit

The simulations were run in a cluster formed of 3 nodes with 2 CPUs Intel Xeon ES-2680 with 8 cores at 2.7 GHz (32 Gb RAM)

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