Reverse-bias current hysteresis at low temperature in GaN Schottky barrier diodes

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Abstract: In this paper we report an analysis of reverse current mechanisms observed in GaN Schottky barrier diodes leading to a hysteretic behavior of the I-V curves at low temperature. By means of DC measurements from 33K to 475 K, we demonstrate the presence of two leakage mechanisms when comparing the experiments with the results obtained using a unified model to predict the ideal reverse current of the diode. Poole-Frenkel emission is the dominant mechanism for temperatures above 200 K, while trap-assisted tunneling prevails for lower temperatures, where also hysteresis cycles are revealed by means of DC dual sweep voltage measurements. The energy of the corresponding traps has also been determined, being around 0.2 and 0.45 eV, respectively. The hysteresis phenomenon is attributed to the bias-induced occupancy of the energy states originating the leakage-current processes, which leads to the reduction of the reverse current after a high negative voltage is applied to the diode.

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I. INTRODUCTION

Terahertz technology has advanced significantly during the last decades, however there are still challenges, like the development of solid-state THz devices capable of generating signals with an appropriate power level in this frequency range.[1] Schottky Barrier Diodes (SBDs) play an important role in solid-state THz sources based on frequency multiplication, with GaAs being the dominant technology. GaAs SBDs are used in multiple applications due to its good performance as detectors, mixers, and frequency multipliers. However, they are not able to handle high power due to its relatively low breakdown voltage and thermal conductivity. In this perspective, GaN is a promising material[2] since its wide bandgap allows to manage much higher input power and can help to reduce the size and complexity (avoiding power-combining) of frequency multipliers.[3,4,5,6] GaN SBDs may expand the practical application of THz technology to fields such as security scanning, medical diagnosis and ultrahigh-bandwidth wireless communications.[7] For these applications, the high breakdown voltage of GaN SBDs is a key parameter for increasing its power performance.[8] However, its real breakdown voltage is effectively reduced from its ideal limit due to multiple mechanisms, typically related to traps and defects located in the epilayer or at the interface[9], such as Poole-Frenkel emission (PFE), tunnelling assisted by traps (TAT) or variable range hopping, which generate an excess of current with respect to the one expected from the ideal mechanisms, thermionic emission and tunnelling current.[10,11,12,13] In this work we analyze in temperature non ideal reverse-leakage current mechanisms related to traps present in GaN SBDs fabricated on MOCVD grown layers on a sapphire substrate. A complete experimental characterization reaching temperatures down to 33 K, lower than those typically used in the literature, has allowed us to identify a hysteretic behavior of the reverse current in dual-sweep measurements not previously described, which becomes notorious below 125 K. This effect is explained in terms of some of the above leakage mechanisms.

The paper is organized as follows. The structure of the measured diodes and the experimental setups are described in Sec. II. The results and their discussion are reported in Sec. III. Finally, the main conclusions are drawn in Sec. IV.

II. DEVICES AND EXPERIMENTAL SETUP

The diodes under analysis were fabricated on an epitaxial structure consisting of a 600 nm thick epilayer (with doping of 5×10^{16} cm^{-3}) and a 750 nm thick substrate of highly doped GaN (10^{19} cm^{-3}) on sapphire

substrate. The Pt/Au Schottky contact is placed on the top of the epilayer while the ohmic contact formed by Ti/Al/Ni/Au is on the highly doped GaN layer. The fabrication process is similar to that decribed in Ref. 14. Circular diodes with different sizes all along the wafer have been analyzed, finding similar effects. Here we present results for a diode with nominal diameter of 221 μm, see Fig. 1.

Current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements have been performed at different temperatures, from 33 K to 475 K, by means of a LakeShore CRX-VF cryogenic probe station. The experimental setup for the characterization of the diodes is different depending on the type of measurements. On one hand, the probe station is connected to an impedance analyzer (Agilent E4980A) for the *C-V* measurements. On the other hand, the *I-V* curves were obtained using a semiconductor analyzer (Keithley 4200-SCS) and four continuously variable temperature probes (which allow temperature sweeps without the need to lift the needles, thus minimizing the damage of the pads). The semiconductor analyzer is connected to the probe station as shown in Fig. 1.

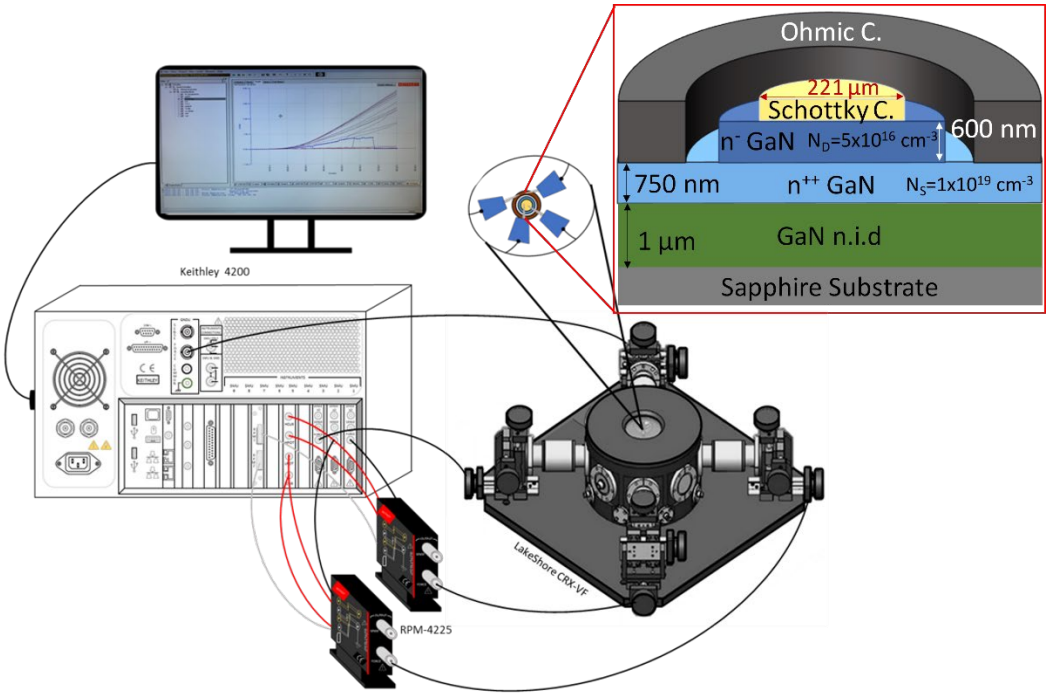

FIG. 1. Scheme of the experimental setup for measuring the *I-V* characteristics. A cryogenic probe station is used to carry out measurements in temperature. The probe station is connected to a semiconductor analyzer (Keithley 4200-SCS). 4 probes are used to perform these measurements. A sketch of the SBD under analysis is also shown, where the position of the ohmic and Schottky contacts, and the doping level and thickness of the different layers, are indicated.

III. RESULTS AND DISCUSSION

Firstly, *C-V* measurements were carried out. Fig. 2 shows the parameters extracted from the *C-V-T* analysis, performed at 1 MHz with V_{osc}=30 mV. The C^{-2} vs. *V* characteristics, which show the typical behavior of a SBD (linear with the applied voltage), is represented in the inset, allowing to extract the epilayer doping, N_D (red), the built-in voltage, V_B (blue) and the barrier height, ϕ_B (pink), shown in Fig. 2 as a function of temperature. Both ϕ_B and N_D remain practically constant with temperature, with values around 0.7-0.8 eV and 4.0-4.5×10^{16} cm^{-3}, respectively. On the other hand, qV_B monotonously increases when decreasing *T*, from below 0.6 eV to around 0.75 eV, almost coinciding with ϕ_B for low *T*.

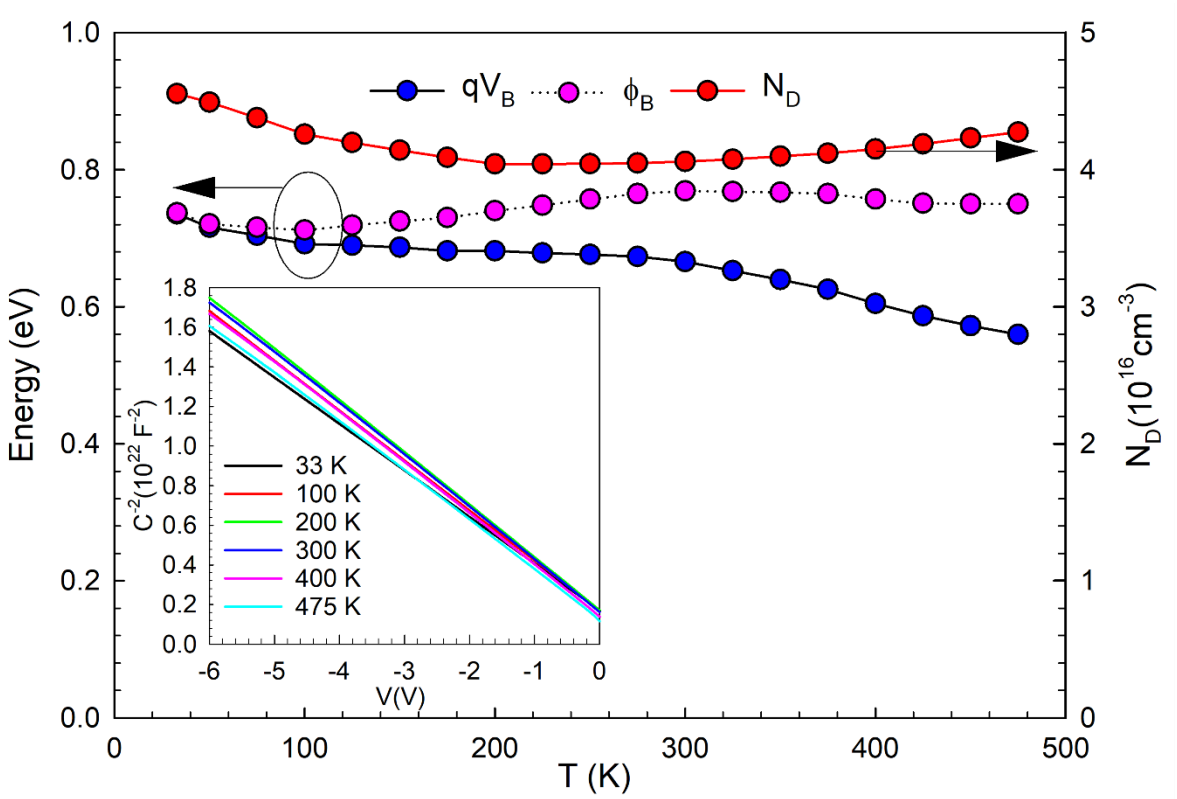

FIG. 2. Characteristic parameters of the SBD extracted from the *C-V* curves as a function of temperature. The inset shows the linear behavior of the C^{-2}-*V* curve, revealing a slight variation with temperature.

The *I-V* characteristic of the GaN SBD has been measured as a function of *T*. Fig. 3 shows the dual sweep *J-V-T* curves of the device (starting at 0 V) in (a) reverse and (b) forward bias, jointly with the results of the model developed in Ref. 14. In forward bias the model only includes the thermionic contribution, while in reverse bias both thermionic (J_{th}) and tunneling currents (J_{tunnel}) are considered. A constant value for the doping

of 4.5×10^{16} cm^{-3} has been used for all temperatures, as well as a series resistance of 1 Ω. The values of ϕ_B and η, shown in the inset of Fig. 3(b), have been extracted at each temperature by fitting the measurements in forward bias, ϕ_B then being used to predict the ideal contribution in reverse bias. Comparing the values of ϕ_B extracted from *C-V* and *I-V* curves, they are similar for the highest temperatures. However, for low *T*, ϕ_B obtained from the ideal current model shows a significant decrease (not observed in the value extracted from the capacitance) and η increases concurrently. This behavior, already found in the literature,[15,16] is attributed to the presence of inhomogeneities of the barrier height.

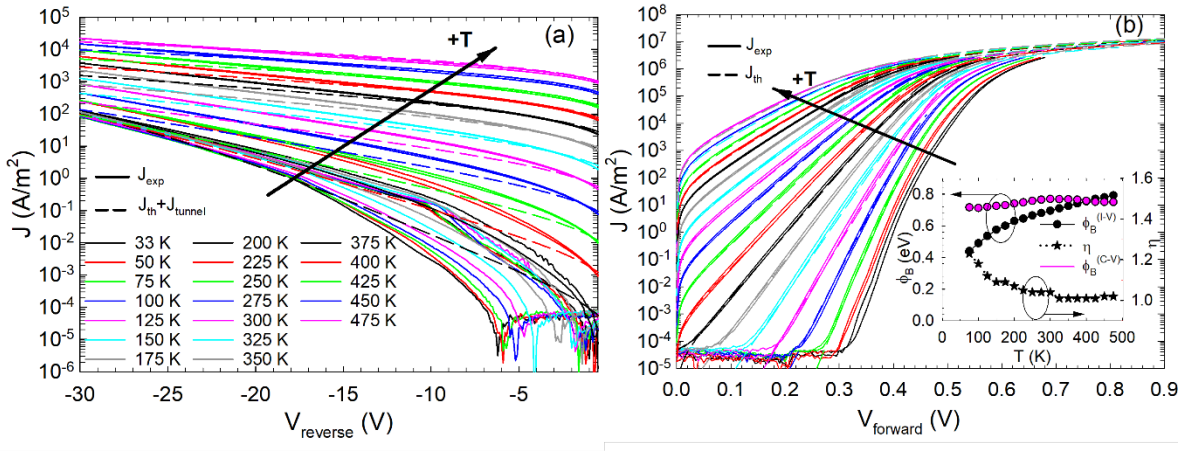

FIG. 3. *J-V* curves measured (solid lines) and modelled (dashed lines) for (a) reverse and (b) forward bias. The inset includes ϕ_B and extracted from the fitting of the ideal model and the experimental curves in forward bias (in black), as well as ϕ_B extracted from the *C-V* curves (in pink).

Let us analyze now the reverse bias results. Fig. 3(a) shows how the ideal model almost perfectly reproduces the behavior of the measurements, J_{exp}, for the highest temperatures. For temperatures from 400 K to 225 K, the experimental curves start to deviate from the model in reverse bias, which evidences the progressive increase of the contribution of nonideal leakage mechanisms. For temperatures below 200 K, the results of the model are not represented in reverse bias, since the values obtained are negligible with respect to the experimental ones. Interestingly, a hysteresis phenomenon is found for the lower temperatures, whose origin will be explained later.

From these DC measurements, by comparison with the model, it is possible to extract the excess of current density due to the non-ideal mechanisms as $J_{exc}=J_{exp}-J_{th}-J_{tunnel}$. This value is represented as a function of the inverse of temperature in Fig. 4(a). For the highest temperatures up to 400 K, J_{exc} is negligible as compared to the high values of J_{th} and J_{tunnel} and the reverse *I-V* curve of the SBD is nearly ideal. Thus, we calculate J_{exc} only for temperatures below 400 K. Two behaviors are observed: for high *T*, a temperature-dependent mechanism is

present, while a temperature-independent one arises at low T. DC dual voltage sweep measurements for the I-V curves were carried out. Since a hysteresis cycle takes place, the current in excess has been represented for both directions of the sweep (go and return). While at high T, J_{exc} does not change between the go and the return, for low T, J_{exc} in the return sweep decreases with respect to the go sweep. Moreover, all the I-V curves tend to reach the same current at -30 V [see Fig. 3(a)].

Regarding the mechanism dominant at high temperatures, a linear behavior with $1/T$ is observed in the return sweep of $ln\ (J_{exc})$, indicating that it can be described as a PFE process, providing an excess current given by[12]

$$J_{PFE} \propto E exp\left(\frac{-q(\phi_t - \sqrt{qE/\pi\varepsilon_{sc}})}{k_B T}\right), \quad (1)$$

where E is the maximum electric field (that appearing at metal-semiconductor interface), q is the electron charge, ε_{sc} is the permittivity of the semiconductor, k_B is the Boltzmann constant and ϕ_t the energy level of the trap at the origin of the PFE process. The permittivity of the GaN used in this work is $8.9\varepsilon_0$,[17] being ε_0 the vacuum permittivity. PFE consists in the thermal promotion of an electron from a trap into the conduction band, process which is fed by tunneling from the metal in reverse bias conditions. Following equation 1, the fitting of $ln\ (J_{exc})$ versus $1/T$, as shown in Fig. 4(b), allows to obtain the energy level of the trap producing the PFE mechanism, which is around 0.2 eV.

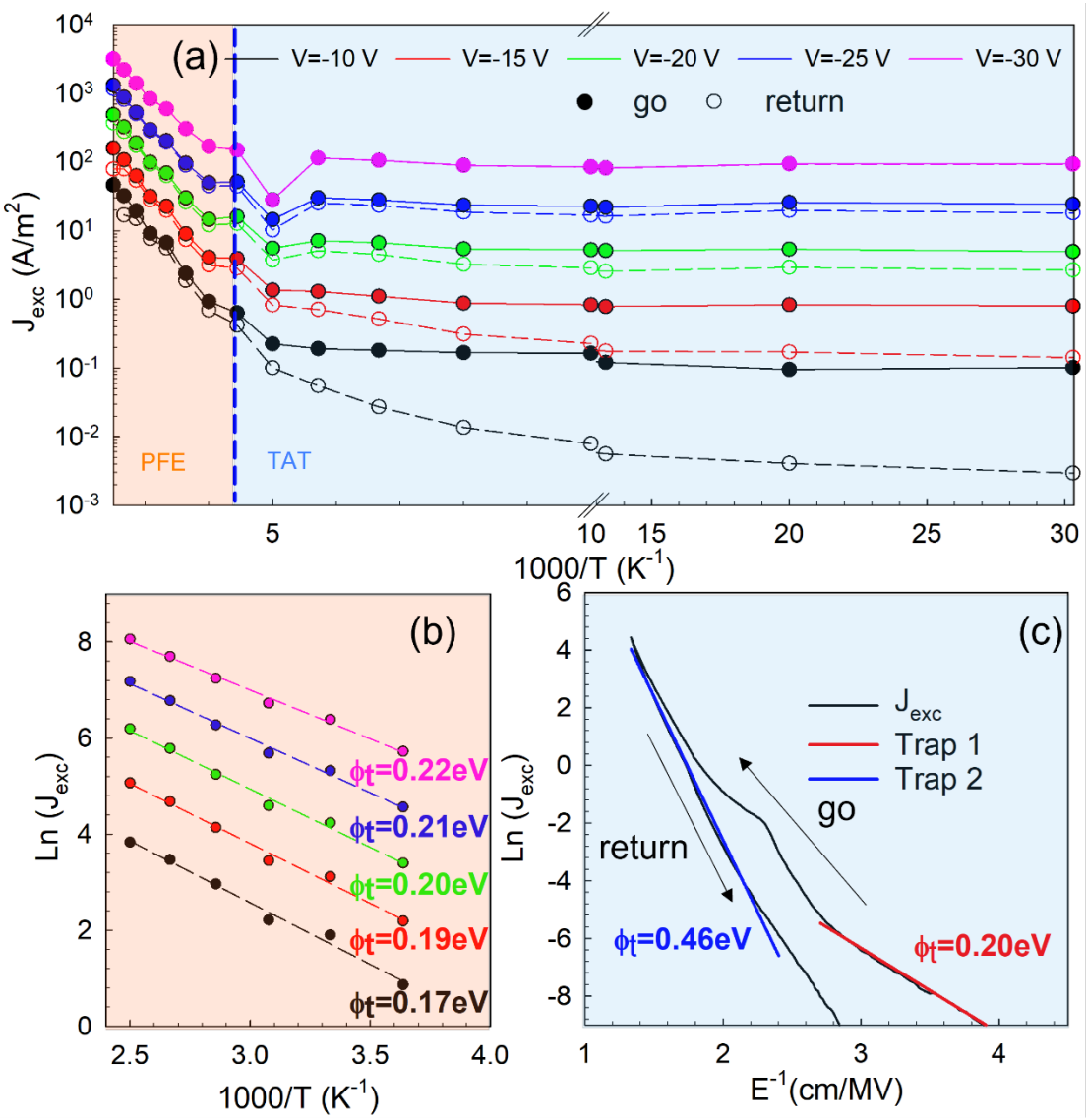

FIG. 4. **(a)** Excess of reverse current as a function of 1/*T* (from 33 K to 400 K) for different bias points. Fitting of the results to the characteristic dependence of **(b)** Poole-Frenkel emission for the highest temperatures and **(c)** trap assisted tunneling at low temperatures (100 K in this case).

On the other hand, for low *T*, J_{exc} is nearly constant with temperature, as observed in Fig. 4(a). Such behavior is typically due to TAT, whose associated leakage current is given by[12]

$$J_{TAT} \propto exp\left(\frac{-4\sqrt{2qm^*}\phi_t^{3/2}}{3\hbar E}\right), \quad (1)$$

where $\hbar$ is the Planck constant and m^* is the effective mass of the electrons (in our case $0.22m_0$).[18] The representation of $ln\ (J_{exp})$ at low *T* (100 K) in the go and return sweeps as a function of the inverse of the maximum electric field is provided in Fig. 4(c). At other (low) values of temperature, a similar behavior is found. The observed linear dependence in different ranges of 1/*E* indicates the presence of TAT mechanisms.

TAT allows the tunnel injection of electrons from the metal to the semiconductor through the traps states as long as these are not occupied.

In Fig. 4(c), two slopes, corresponding to different traps, can be distinguished. The energy level extracted for these trap states is around 0.2 eV for trap 1 and around 0.45 eV for trap 2. Interestingly, the energy of trap 1 is very similar to that at the origin of PFE at higher temperatures, which means that as electrons do not have the enough thermal energy to be injected by PFE, they use the same trap to tunnel into the semiconductor.

The go curve in Fig. 4(c) exhibits a higher current level with respect to the return one. For low values of reverse bias (low electric field, linear dependence on $1/E$) the current due to electrons tunneling through trap 1 is dominant, because the trap states are located closer to the conduction band. When the reverse applied voltage is increased, the influence of trap 2 starts being significant due to the narrowing of the barrier, so that the probability of electrons tunneling through trap 2 increases, as well as the slope of the curve. A transition between TAT processes dominated by each of the traps takes place around a value of $1/E$ of 2.7 cm/MV. If the applied voltage is further increased, some of the trap states become occupied and the current increase is softer. When decreasing the reverse applied voltage, a lower current level is measured in the return curve. For the highest voltages (highest electric fields), a linear behavior of ln (J_{exc}) with respect to $1/E$ is found again, which fits the TAT dependence described by equation 2 with the energy of trap 2.

The explanation to this behavior is as follows. As the applied voltage is raised in the go sweep, the occupancy of both traps increases, first that of the lower-energy trap 1, and then that of trap 2 for the highest voltages. When the bias is decreased in the return sweep, due to the fact that some of trap states remain occupied, mainly those of trap 1, TAT processes are less frequent and obviously the current is lower than in the go sweep. Even if both traps have a higher occupancy, the effect of trap 1 on the current is more significant due to its closer proximity to the conduction band as compared with trap 2. Thus, while the lower concentration of free traps has an important effect on the current for the case of trap 1, by drastically reducing the associated TAT processes, in the case of trap 2 it is not so crucial, and it is this trap that dominates the TAT current in the return sweep.[19] Also the capture cross section of the traps could be important.

If just after a first dual voltage sweep measurement a second one is performed, both the go and return curves essentially coincide with the return curve of the initial sweep, indicating that the traps remain occupied. Only if the device is appropriately illuminated or after a long time (several days), both leading to the release of

the trapped electrons, the initial hysteresis cycle is recovered. Additionally, pulsed measurements applying different base voltages (of 0, -20 and -30 V) prior to each measured point were performed, evidencing higher initial occupancy of the trap states linked to higher base voltages. All these facts confirm that the hysteresis observed in the reverse *I-V* curves is due to electron trapping impeding the current flow through TAT processes. This effect has been found in all the diodes of the wafer, with just a little variability in the voltage range and the current levels for which the hysteresis takes place, but with the same qualitative behavior. The trap energies obtained are in a narrow range of 0.18-0.22 eV and 0.46-0.50 eV, respectively.

IV. CONCLUSIONS

In summary, the reverse current of a GaN on sapphire SBD has been analyzed from 33K to 475 K. While it shows a nearly ideal behavior for the highest temperatures, below 400 K an extra leakage current contribution with respect to the ideal one is obtained. The analysis of this current in excess has clearly evidenced the presence of two mechanisms related to traps. For temperatures above 200 K, PFE through a trap with an energy level around 0.2 eV is dominant, while for lower temperatures, TAT is the prevailing mechanism. Remarkably, two different traps contribute to the TAT current, causing an hysteresis phenomenon in the reverse *I-V* curves. The energies of these traps are around 0.2 eV (trap 1, the same one that provokes PFE) and 0.5 eV (trap 2). The hysteresis is caused by the increase in the occupancy of both trap states as the reverse bias is raised, and the stronger influence of the occupancy of trap 1 on the current level.

ACKNOWLEDGEMENTS

This work has been partially supported through Grant PID2020-115842RB-I00 funded by MCIN/AEI/10.13039/501100011033 and by the French project SchoGaN (ANR-17-CE24-0034). B. Orfao acknowledges the PhD contract from the Junta de Castilla y León. R. A. Peña acknowledges the “Investigo” contract funded by the Junta de Castilla y León and by “European Union NextGenerationEU/PRTR.

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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