Exploring Digital Logic Design Using Ballistic Deflection Transistors Through Monte Carlo Simulations

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***Abstract*—We present exploratory studies of digital circuit design using the recently proposed ballistic deflection transistor (BDT) devices. We demonstrate a variety of possible logic functions through simple reconfiguration of two drain-connected BDTs. We further propose the creation of a three-BDT logic cell to yield differential versions of each logic function, improving overall flexibility of BDT circuit design. Each of the proposed gate configurations has been verified through extensive numerical calculations using an in-house Monte Carlo simulator. Simulation results show that the proposed gate arrangements are capable of achieving 400-GHz operating frequencies at room temperature. A compact fit-based analytical model to aid circuit design using BDTs is also introduced.**

***Index Terms*— Monte Carlo simulations, room-temperature ballistic transport, logic design, high-frequency transistor structures, III-V compound semiconductors, two-dimensional electron gas.**

Manuscript received October 26, 2010; revised April 30, 2011. This work was supported in part by the NSF NIRT under Grant ECS-0609140, in part by the ONR under Grant N00014-08-1-0093, in part by the AFOSR under Grant FA9550-07-1-0032, by the European Commission through the ROOTHz Project ICT-2009-243845, by the Dirección General de Investigación (MICINN) and FEDER through Project TEC2010-15413 and by the Consejería de Educación, Junta de Castilla y León through Project GR270. Device fabrication was performed at the Cornell NanoScale Facility and at the Harvad's Center for Nanscale Systems, supported by the NSF under Grant ECS-0335765, Grant EEC-0117770 and Grant 0646547, and by the NYSTAR under Contract C020071. The review of this paper was arranged by Associate editor Roger Lake.

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I. Introduction

AGGRESIVE scaling in complementary metal–oxide–semiconductor (CMOS) technology has allowed designers to integrate billions of transistors on a single die. These advances have ensured continuous development of extremely complex, high-performance integrated circuits; however, with commercial CMOS technology having already passed into the 32-nm node, device scaling is fast approaching the limits of reliable fabrication. Consequently, over the past few years, researchers have been actively exploring novel devices for the progress of semiconductor technology beyond CMOS and a wide variety of alternative structures have been proposed. Some devices offer improved speed, some promise unmatched power efficiency, while others are reconfigurable at runtime to offer both versatility and robustness [1].

One promising solution is the use of devices based on high-mobility III–V compound heterostructure systems. These systems can be designed to create a two-dimensional electron gas (2DEG) layer, in which electrons travel with an estimated electron velocity of the order of 10^8 cm/s—more than 2.5× faster than electron transport in silicon. The use of advanced electron-beam lithography tools and conventional epitaxial growth techniques for III–V materials allow one to fabricate 2DEG structures with dimensions smaller than the electron mean free path l ($l \approx 140$ nm at room temperature in InGaAs channels). Therefore, the 2DEG facilitates electron transport with few, if any, scattering events. The latter is referred to as ballistic transport and can be observed even at room temperature. This behavior and its applications have been studied by a number of research groups and presented in many articles [2]–[11], including a detailed overview of developments in room-temperature ballistic nanostructures by Song [12].

In recent years, several efforts have been made to design and characterize new nanometer-scale (nano) ballistic transport devices in which electrons are guided by device geometries (strategically placed shapes, edges, and internal deflectors) rather than applied potentials. Examples of this emerging family of nano-devices include ballistic rectifiers

(BRs) [3]–[4], T-shaped or Y-shaped branch junctions (TBJs or YBJs) [5]–[9], and self-switching diodes (SSDs) [10]. BRs based on GaAs/AlGaAs heterostructures were first proposed by Song *et al.* in [3] and were shown to operate at cryogenic temperatures. In [7] Xu *et al.* theoretically predicted the nonlinear operation in TBJs. These devices have demonstrated manifold functionalities since their nonlinear properties allow for rectification, frequency doubling, and Boolean logic functionality, all being able to work at very high frequencies. The most important from the point of view of circuit applications, however, is the fact that all these devices successfully operate at room temperature. Monte Carlo simulations have shown that ballistic nano-devices are intrinsically capable of working at THz frequencies [13], [14] and experiments confirmed nonlinear effects occurring at GHz-range frequencies, including rectification up to 50 GHz in BRs [15], negative differential transconductance up to 110 GHz in TBJs [16], RF to DC rectification up to 94 GHz in TBJs [17],[18], frequency doubling up to 4 GHz in TBJs [19], and detection up to 110 GHz at 300 K [20] and up to 2.5 THz at temperatures below 150 K in SSDs [21]. In addition, most recently, Irie and Sobolewski [22] have experimentally demonstrated operation of TBJs of up to above 0.5 THz, when excited by picosecond electrical pulses.

Based on the pioneer works of Hieke *et al.* [4], [5], our group recently proposed a novel ballistic device, called ballistic deflection transistor (BDT) [23]. Kaushal *et al.* [24] studied the DC behavior of BDTs and their performance dependence on the nanostructure geometry, while Wolpert *et al.* [25] highlighted potential circuit applications through the design of a NAND gate. Aside from technological challenges associated with the fabrication complexity of nano-devices, there is an increasing gap between the device physicists and circuit engineers that needs to be bridged to achieve success with novel device platforms, such as the BDT. The main contribution of this work is not only to validate the feasibility of BDT-based logic design through simulations but also to stress the need for a combined effort at both the device and circuit levels, aimed toward exploring new and interesting capabilities offered by ballistic nanostructures such as, e.g., BDT, in order to continue the immense performance improvements of the last few decades.

The remainder of this paper is organized as follows. In Sec. II, we provide a brief overview of the BDT concept, its operating principle, and utility for logic applications. In Sec. III, we have present a validation of our models by replicating experimental results previously reported for the BDT NAND gate [25] through the use of our Monte Carlo (MC) tool. We then analyze the bias conditions to maximize the device's current output and optimize its high/low margins. The feasibility of the device for frequency doubling has also been demonstrated. In Sec. IV, we discuss novel, two-transistor and three-transistor configurations for constructing BDT-based logic circuits, while Sec. V introduces a compact-fitting analytical model to aid circuit design using BDTs. Our summary and concluding remarks are in Sec. VI.

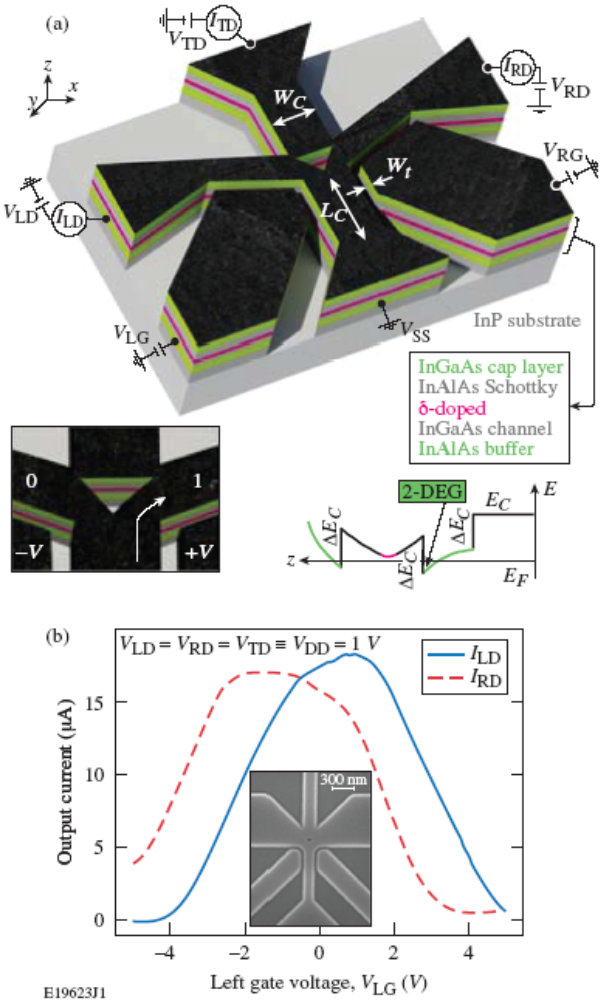

Fig. 1. (a) 3-D topology and heterostructure of a typical BDT. Inset shows the energy-band diagram of the conduction band. Electrons in the high-mobility 2DEG are provided by the δ- doped layer, which is highly doped and separated from the channel by the undoped spacer to reduce the interaction with remote impurities. The top-left and top-right ports are drain ports (V_{LD} and V_{RD}, respectively); the bottom-left and bottom-right ports are gates (V_{LG} and V_{RG}, respectively); the top port is a bias port (V_{TD}) that controls gain, and the bottom port is the source (V_{SS}). Inset: Schematic showing electrons trajectory for positive right gate bias condition ($V_{RG} = -V_{LG} = V$). (b) Transfer characteristic I_{RD} and I_{LD} for gates in push–pull bias ($V_{LG} = -V_{RG}$). Process variation causes a subtle difference in I_{RD} and I_{LD}. Inset: SEM (with scale indicator) of the top view of BDT with channel width (W_C) = 140 nm, channel legth (L_C = 700 nm), and trench width (W_t) = 100 nm. Room temperature electron sheet density is 10^{12} cm^{-2}.

II. The Ballistic Deflection Transistor

A. Device description

The BDT is a six-terminal coplanar structure etched into an InGaAs 2DEG. The device consists of a grounded electron source, left and right gates, and three biased drains. Electrons in the BDT travel through a 2DEG medium experiencing a very large l value (very high mobility), and, under specific conditions, their motion is almost unhindered by either carrier-carrier collisions or scattering of lattice defects, impurities, or

phonons. The BDT augments the ballistic channel with two in-plane gates and a triangular obstacle to selectively deflect electrons. The gates induce the steering effect and, along with the additional electron guidance provided by the triangular deflector, provide nonlinear BDT transfer characteristics [23], [24], distinctly different from the conventional pinch-off field effect control of standard CMOS devices. In comparison to gated YBJ structures, called also Y-branch switches [6], [8] the BDT has an extra terminal, the top drain. This top terminal is required to aid the electrons in moving upwards, away from the source. It also helps to accelerate electrons, resulting in an increase in the electron velocity. These electrons with increased momentum, upon collision with the deflector, move towards the side channels faster, and thus provide a higher gain. As a result, the gain in the device can be controlled through the top terminal as shown in [24]. The latter is in addition to the control exerted by the in-plane gates in BDT. In other words, even if the top terminal does not directly impact the logic operation of the device, it offers increased control over the strength (magnitude) of the signal. On the negative side, this electrode is responsible for the BDT leakage current; however, a proper design (position of the deflector and top opening aperture) can enhance the side drain output with no significant top drain current, thus, avoiding extra power consumption. In gated YBJs where the top drain is absent, the transport inside the device can only be controlled through the in-plane gates.

Figure 1(a) shows a sketch of the heterostructure of a generic BDT structure. It is a commercial $In_{0.53}Ga_{0.47}As$-$In_{0.52}Al_{0.48}As$ heterolayer grown on an InP substrate, with the 2DEG channel occurring about 60 nm deep. The value of the electron sheet density at room temperature is 10^{12} cm^{-2}. A typical transfer characteristics obtained under push–pull bias conditions ($V_{RG} = -V_{LG}$) is shown in Fig. 1(b). This result was measured in a BDT with a channel width W_C of 140 nm. It is observed that the bottom branch is pinched off for very high V_{LG}. As V_{LG} is increased, the bottom branch begins to conduct current, steering it toward the right drain. As V_{LG} increases beyond a critical voltage (slightly less than 0 V because of process variations), more current is steered toward the left drain; as V_{LG} is further increased, the branch pinches off again. Additional information about the fabrication process and operating parameters of our test BDTs is available in [24], while the DC performance is presented in [26].

B. Logical behavior of the BDT

During our study of the BDT, the switching behavior between the two side terminals became a research focus to achieve Boolean logic applications. When the carrier current moves along the right drain in the BDT, the transistor is said to register “logic 1” at the right drain and “logic 0” at the left drain [inset in Fig. 1(a)]. The potential for implementing the Boolean logic, combined with the high operating speed, opens up many interesting avenues for high-performance BDT-based

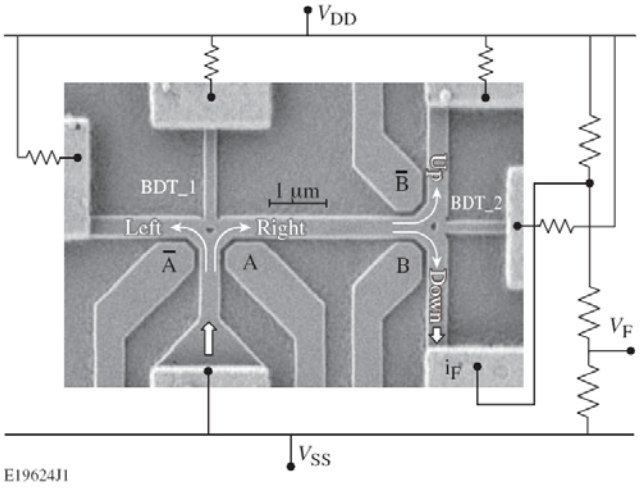

Fig. 2. Scanning-electron-microscope (SEM) image of BDT NAND gate with proposed experimental setup. Similar figure presented in [25].

circuit implementations. What makes it particularly interesting is the possibility of achieving the progress with no significant changes to the system and logic portions of our developed digital design flow.

A two-input NAND gate logic function created with BDTs has been previously studied by Wolpert *et al.* [25]. Figure 2 shows an SEM image of the BDT-NAND gate along with a super-imposed circuit. The NAND gate operation can be understood as follows: the source is shown as the arrow entering the bottom channel of the BDT_1. The differential gate inputs A and $\bar{A}$ guide electrons into the channel labeled “right” when A = 1 (gate high) and $\bar{A}$ = 0 (gate low), and into channel “left” in the opposite case. The differential gate inputs B and $\bar{B}$ of the BDT_2 guide electrons from the central region into the channels labeled “up” or “down” similar to gate A. This results in a flow of electrons at the output i_F only when both A and B are high. For each other input combination, electrons are diverted either to the left output of BDT_1 or BDT_2. This behavior results in the logic function: NAND AB.

One of the major challenges of creating logic with BDTs is the method of converting the output current of one device into the input gate voltage of the next one. In the BDT, the accumulated gate charge is not dissipated by switching the driving gate input; instead, the lack of driving current creates a high-resistance path to V_{DD} and ground through the driving device. One solution is to use a string of resistors between V_{DD} and V_{SS} as a current-to-voltage converter, as drawn outside the SEM picture box in Fig. 2. The output current i_F from the BDT affects the voltage division between V_{DD} and V_{SS}, and the resistor values (in the MΩ range to limit standby current) can be calculated such that the voltage at the output nodes v_F matches the range of input gate voltages A and B. The resistors are externally connected [27]–[28] or integrated as recently demonstrated by Muller *et al.* [29] in similar types of nano-devices like TBJs to fabricate logic circuitry.

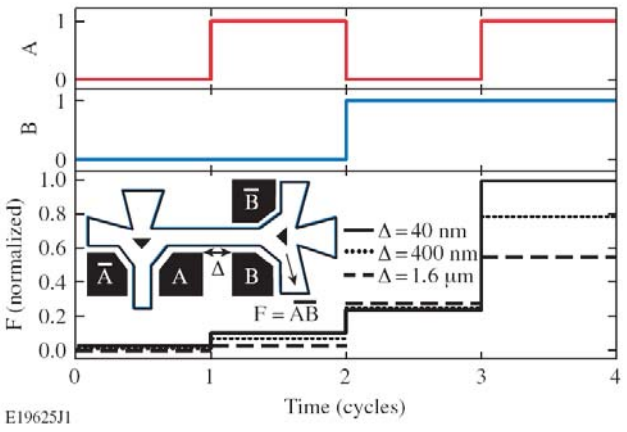

Fig. 3. MC-simulated DC values of BDT NAND gate for different separations Δ between BDTs, represented in transient waveform format for presentation purposes and normalized against the maximum value of 2.1 μA. These results are in agreement with the experiments in [25].

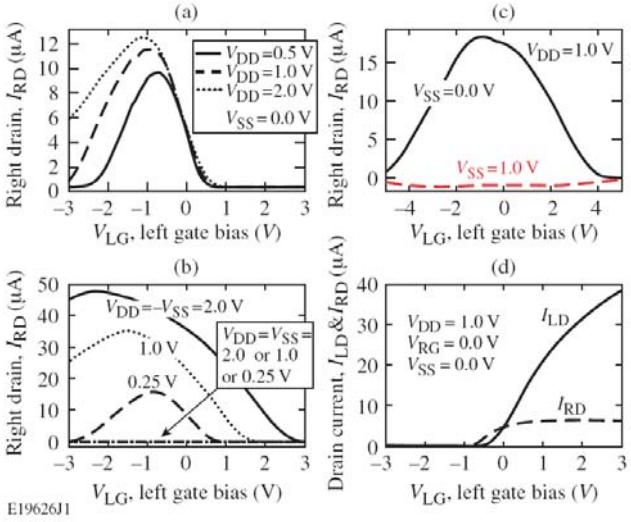

Fig. 4. MC simulations of the effect of bias conditions on performance: (a) drains' bias V_{DD} and (b) source bias V_{SS}. The left drain current exhibits an identical response but is mirrored around the center axis because of the symmetry of our simulated BDT. (c) Experimental ON and OFF state using V_{SS} = 0 V and V_{SS} = 1 V, respectively. (d) MC asymmetric logic configuration (sweeping V_{LG} with V_{RG} = 0 V). Simulations were performed for a BDT with L_C = 350 nm operating at room temperature.

III. Monte Carlo Results

We have recently demonstrated the usefulness of our ensemble MC simulator to evaluate the impact of changing geometric parameters on the BDT performance [24]. The accuracy of this tool has also been validated by closely matching simulation and experimental results in other ballistic devices [30], [31]. Here, we use the MC simulator to explore digital applications by analyzing our two-input NAND gate [25] and the impact of biasing conditions, as well as by providing new simulations of high-performance frequency doubling in a single BDT.

A. Monte Carlo modeling

Our MC tool simulates the electron dynamics self-consistently coupled with a 2-D Poisson solver (finite-differences approach) [32]. The tool contains all the appropriate ingredients for accurate simulations, including models for the ionized impurity, alloy, polar and non-polar optical phonons, acoustic phonons, and inter-valley scattering. We also consider of Γ-L-X non-parabolic spherical valleys, appropriate contact carrier injection techniques, and the effects of the surface charges appearing at the boundaries of the semiconductors in contact with dielectrics (crucial when the size is reduced to nanometer dimensions) [13]. All simulations reported in this paper assumed room-temperature operation of the BDT.

B. NAND gate architecture

The BDT NAND gate described in the previous section was simulated in Ref. [25] using an empirical model based on a BDT equivalent circuit, constructed using piecewise linear voltage–controlled current sources and resistors. This simplistic approach ignored the impact of electron transport and geometry on the device performance, limiting the accuracy for testing designs where no empirical device data were available. Results of our MC simulations are shown in Fig. 3 for all combinations of the inputs A and B. For a separation between BDTs of Δ = 1.6 μm (similar to the fabricated value), the I_{on}/I_{off} values closely match the experiments from Ref. [25]. In the previous empirical model, it was assumed that the drain potentials in both BDTs were properly balanced, which would result in the A = 0/B = 1 and A = 1/B = 0 states having the same output voltage. Unfortunately, that was not the case in experimental results obtained on an actual, fabricated BDT NAND gate [25]. The uneven drain potential in the fabricated prototype increased the amount of incorrectly steered current in BDT 1, such that even when A = 0, a large current (leakage) was found to flow into BDT 2; when B = 1, the same undesired current flow was found to reduce the output voltage, thereby limiting the gate's I_{on}/I_{off} ratio. In contrast, the MC simulation presented by us reproduces the experimental behavior for A = 0/B = 1 (Fig. 3). In addition, we also studied the effect of the parameter Δ, showing, as expected, an increase of the I_{on}/I_{off} ratio for smaller distance between BDTs.

C. Analyzing the impact of biasing on BDT performance

The reference device used for investigating the impact of the bias conditions on the BDT behavior in our MC simulations is the same as in previous works [24]. It has a channel width W_C = 100 nm and length L_C = 350 nm. The trench width W_t between the gates and the 2DEG InGaAs conductive channel is 5 nm (the trenches and the triangular deflector are left unfilled). The surface charge at the semiconductor/air boundaries is $\sigma/q = 0.3\times10^{12}$ cm^{-2}, which leads to a depletion width of 30 nm [33]. Figure 4(a) shows the drain current with the drain bias $V_{TD} = V_{RD} = V_{LD} \equiv V_{DD}$,

V_{SS} = 0 V, and push–pull gate bias $V_{LG} = -V_{RG}$. As observed in experiments [24], the threshold voltage shifts to higher gate voltages when the drain bias is increased; also, as expected, the current increases. So a compromise value of V_{DD} should be selected to obtain a large-enough current with reasonably small values of the gate bias.

It should be noted that in Fig. 4(a) for the simulated BDT operating in the gate push–pull configuration, "logic 1" corresponds to V_{DD} and "logic 0" to $-V_{DD}$. From the logic design perspective, it is desirable to maintain uniform values for the voltages corresponding to logic 1 and logic 0. For instance, with reference to conventional CMOS gates, logic 0 corresponds to a voltage of 0 V, while logic 1 implies voltage equal to the operating V_{DD} of the device. In addition, the logic gates proposed in the next section also use the source terminal as one of the logic inputs. So, first, in Fig. 4(b), we show the impact of varying the values of V_{SS} in the push–pull bias. The use of $V_{SS} = -V_{DD}$ provides, as expected, a huge increase in the current level in comparison to Fig. 4(a), where V_{SS} = 0 V. We can see that when $V_{DD} = V_{SS}$, the current is zero, facilitating an OFF state for logic applications as corroborated by experimental measurements shown in Fig. 4(c). Now we try to explore the logic configuration when logic 1 corresponds to V_{DD} and logic 0 to 0 V, which we will refer to as "asymmetric fashion". Figure 4(d) presents the results for these asymmetric logic conditions (V_{RG} = 0 V and V_{LG} = sweep). For the low state in the left gate V_{LG} = 0 V, both currents are smaller. When V_{LG} = 1 V, however, it can be observed that although the left current is reasonably high, the right-side branch (V_{RG} = 0 V) is not completely pinched off, reducing the noise margin. This analysis is important in characterizing the device behavior over a broad range of bias conditions, making it easier to identify the optimum configuration for the BDT-based circuit implementations.

D. *Verification of sub-THz response*

One of the main advantages of the MC method is its ability to perform time-domain simulations. To check the predicted ultrahigh-frequency limit of the BDT operation, we have performed time-domain MC simulations of the device. As shown in Fig. 5, a push–pull harmonic signal of the frequency f_{in} = 200 GHz was applied to the gates, $V_{RG}(t) = -V_{LG}(t) = V_0\sin(2\pi f_{in}t)$, with V_0 = 0.5 V, over a DC value of V_{RG} = 0.5 V (just at the top of the I_{RD}–V_{RG} characteristics of the BDT). The time evolution of I_{RD} in Fig. 5 shows that although a small delay is detected, the response can be considered as quasi-static since $I_{RD}(t)$ essentially follows the DC dependence with $V_{RG}(t)$. The frequency-doubling action expected from the DC response is also present, confirming an excellent sub-THz (400-GHz) frequency operation. Our picosecond electro-optic sampling setup recently implemented for time-domain response studies of TBJs [22] is now being applied to the BDT characterization, with the intention of corroborating our simulations.

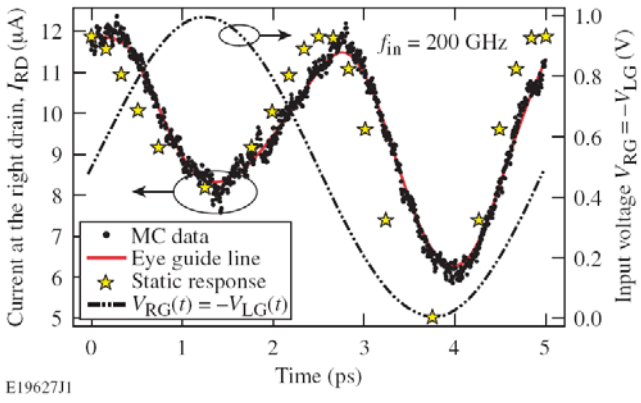

Fig. 5. Time domain response current at the right drain, I_{RD}, for a periodic input signal with an amplitude of 0.5 V over V_{RG} = 0.5 V and 200 GHz. The simulated BDT has L_C = 200 nm and the trenches are filled with an insulator of ε = 10.

IV. New Digital Logic Design Using BDTs

As mentioned in the previous sections, one of the major objectives of the BDT work is to develop high-performance logic gates. One such arrangement, presented in Ref. [25] and shown earlier in Fig. 3, consists of two BDTs rotated 90º with respect to each other. This gate was the BDT's first foray into circuit design applications, but since it had some limitations, we propose here a new arrangement that removes those limitations caused by their simple and symmetric structure. Our novel two-BDT arrangement, as shown in Fig. 6, serves as a generic and flexible logic structure. The structure can be programmed to provide all the desired logic functionalities by appropriately configuring the source and gate terminals of the devices. The two BDTs in this structure have identical orientations, what should lower the design susceptibility to process variations and potentially reduce routing complexity. It should also be noted that in a BDT structure with open side drains, the V_{DD} bias of the top drain allows to feed the in-plane gates of the subsequent BDTs in the various logic gate configurations. This is another motivating factor behind the inclusion of this top terminal in our BDT topology.

A. *Generic 2-BDT logic structure*

Figure 6 is a symbolic representation of the proposed logic gates designed using the two-BDT structure based on the 2:1 multiplexer, where the output is the current in the common arms of the two BDTs. It can be observed that all the gates are designed with an identical BDT arrangement, but still provide various logic functionalities, as indicated in Table I. In the multiplexer, the source terminal of the BDT is fed by the select signal S. When S = logic 1, there is no electron flow in the left BDT since V_{DD} (i.e., the top drain V_{TD}) and V_{SS} are both at logic 1 [see Figs. 4(b)–4(c) for a single BDT and for $V_{SS} = V_{DD}$]. At the same time $\overline{S} = 0$ implies that the electron flow through the right BDT is controlled by the input "in1." The opposite scenario unfolds when the select line S is held

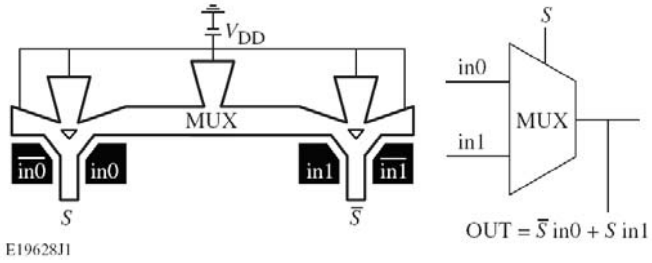

Fig. 6. Two-input logic gate design based on the BDT multiplexer. Output was taken in the middle of the two BDTs.

TABLE I

ALL GATE FUNCTIONALITIES (**A** AND **B** ARE THE INPUTS)

in0	in1	*S*	Logic
B	**1**	**A**	**A** OR **B**
B	**0**	$\overline{A}$	**A** AND **B**
0	$\overline{B}$	$\overline{A}$	**A** NOR **B**
1	$\overline{B}$	**A**	**A** NAND **B**
A	**B**	**B**	**A** XOR **B**
A	$\overline{B}$	$\overline{B}$	**A** XNOR **B**

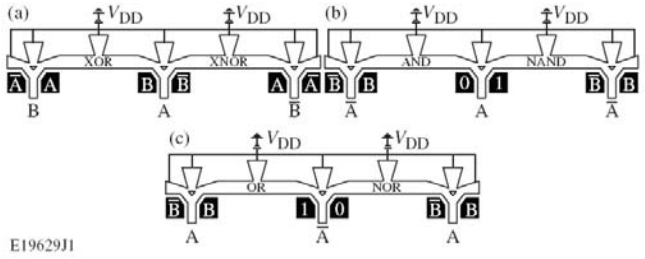

Fig. 7. AND/NAND, OR/NOR, XOR/XNOR gates based on three BDTs.

low. In that case, the device output is controlled by "in0." Therefore, the arrangement indeed works as a 2:1 multiplexer. Truth tables of each of the gates may be generated to verify their functionality, as shown in Table I (A and B are the inputs). Multiplexers can be used to create any logic functionality; consequently, derivation of the other logic functions is a simple exercise in logic design.

The BDT works in a push–pull fashion, which implies that when logic 1 (V_{DD}) is applied to one gate, the other gate is at logic 0 (V_{SS} or $-V_{DD}$). Similar to CMOS-based differential design styles like the Differential Cascode Voltage Swing Logic [34], this could potentially eliminate the need to invert the input signals, by operating the BDT intrinsically as a differential gate. The 2-BDT gates can be extended by adding a third BDT, as shown in Fig. 7, to provide differential AND/NAND, OR/NOR, and XOR/XNOR functionalities, further eliminating the need for extra inverters in the circuit. The initial inverted inputs to the BDT gates can be produced using the V_{DD} and V_{SS} rails. The next subsection presents a study of the gate performance under varying V_{DD} and V_{SS} combinations.

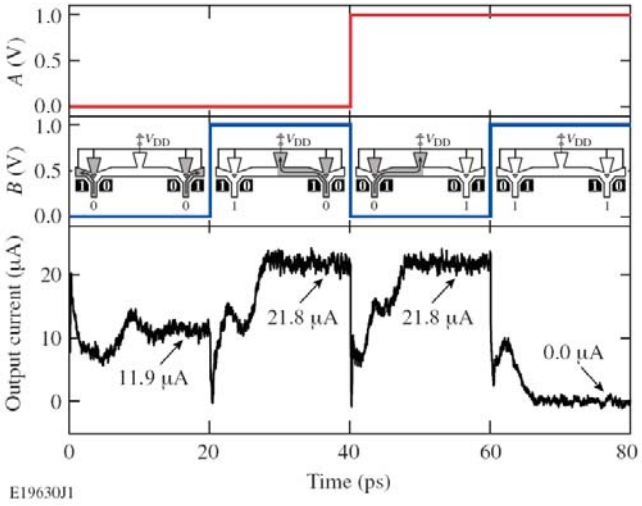

Fig. 8. XOR current-wave form. Insets illustrate the principle of operation, showing in grey the regions where the current flows as a result of the voltages applied to the side gates and source inputs. It should be noted that in terms of input voltages, "logic 1" means V_{DD} and "logic 0" means $-V_{DD}$.

B. Monte Carlo analysis of a two-BDT XOR gate

To verify the predicted behavior of the gates, we have performed dynamic simulations using our MC tool by varying the inputs A and B to undergo the transitions 00, 01, 10, and 11. The time-dependent value of the current was recorded at each femtosecond at the central output of an XOR arrangement, as shown in Fig. 8. The obtained response confirms the XOR functionality with an output current of the order of 22 μA for logic 1 and 12 μA for logic 0. The observed output propagation delay of about 6 ps can be attributed to the redistribution of carriers in the device. It should be noted that this delay implies a potential operating frequency of up to 150 GHz.

Apart from the speed, it is important to analyze the output current of the BDT for its ability to drive multiple logic gates. Ideally, it is desirable to have zero current in the side branches at logic 0. There is, however, always an electron flow into the output since the branches are not completely pinched off. For the BDT to reliably drive multiple fan-out BDTs, it is necessary to increase the current magnitude corresponding to logic 1 along with a simultaneous decrease in the magnitude of the logic-0 current to guarantee high current and large noise margins. To this end, we have analyzed the effect of varying different device parameters and biasing conditions on the output current of the BDT working as the XOR gate. Figure 9 shows a table of the 1 and 0 current magnitudes and the margins achieved during the XOR operation process. First, in Fig. 9(a), we show that increasing the value of VDD significantly increases the current corresponding to the logic-1 state. Also, as expected from Figs. 4(b) and 4(d), the push–pull configuration provides higher output levels than the asymmetric configuration. From Fig. 9(b), it can be observed that decreasing W_C decreases the logic-1 and -0 states because of the reduced available channel width; however, the high-to-

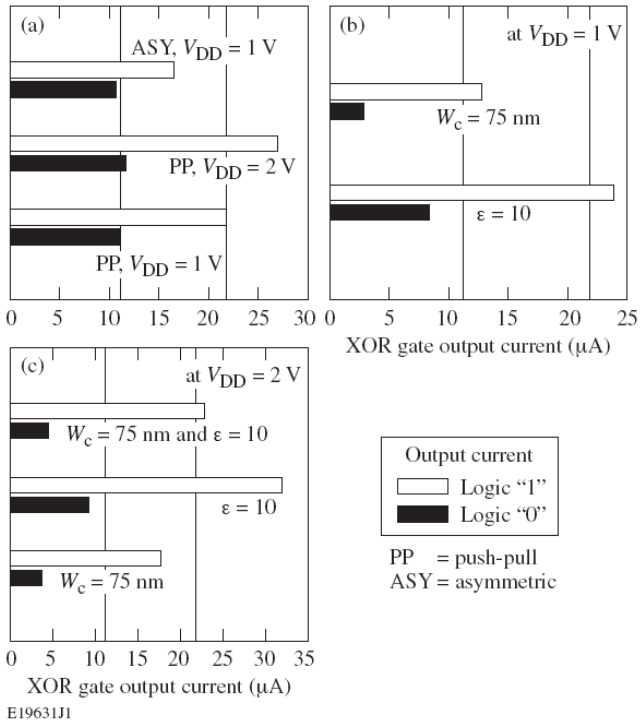

Fig. 9. Variation of XOR gate output current with modifications of the BDT geometry and bias conditions. (a) V_{DD} and bias fashion where push–pull operation means logic 1 = V_{DD} and logic 0 = $-V_{DD}$, while asymmetric operation means logic 1 = V_{DD} and logic 0 = 0 V. (b) Effect of channel width, surface charge, and permittivity for V_{DD} = 1 V and (c) for V_{DD} = 2 V. Vertical lines corresponds to the high and low state for the reference BDT with push–pull V_{DD} = 1 V.

low current margin increases. We also note that performance improves significantly when the trenches are filled with a high-k dielectric because of the enhancement of the gate-to-channel coupling [24]. Finally, Fig. 9(c) presents a similar study to Fig. 9(b) but for V_{DD} = 2 V. This characterization is particularly helpful for establishing guidelines for circuit design using the BDT. It should be noted, however, that in our study the output of the gates are current levels, while the inputs for the logic gates are voltages. So a current-to-voltage converter is necessary to ensure logic level compatibility.

V. Compact Fitting Analytical Model

For any device to be accepted into the mainstream digital circuit design, it is extremely important to extensively simulate its operation and, subsequently, characterize its circuit performance in terms of delay, maximum operating frequency, area, power, etc. We believe that such analysis is necessary not only to validate the device choice but more importantly to help establish early generations of predictive models, which will enable one to more easily integrate the selected device into the overall circuit design flow. Finally, it should allow bridging the gap between the approaches taken by the device physicists and circuit designers by improving understanding of novel device concepts and, simultaneously, accelerating circuit design.

We have used the data obtained from our experiments to develop a simple, compact, predictive model for the BDT. Here a three-parameter Gaussian peak has been selected as the analytical expression model of the device:

$$I_D = a \times \exp\left[-0.5\left(\frac{V_{LG} \pm V_0}{b}\right)^2\right]. \quad (1)$$

In Eq. (1), the drain current I_D (left or right) is calculated using the left-gate voltage V_{LG} as a reference. V_0 is the gate voltage corresponding to the peak current ($+V_0$ for the right drain and $-V_0$ for the left drain). The parameter "*b*" controls the width of the *I*–*V* curve's "bell" shape and is closely related to the full width at half maximum; "*a*" is linked to the height of the curve's peak. To connect these parameters to several physical dimensions and bias conditions of the BDT, we have studied three different devices at room temperature with channel widths of 240, 140, and 100 nm, respectively, and under different bias conditions. Comparisons between the measurements and the analytical model using Eq. (1) are shown in Fig. 10(a) for W_C and in Fig. 10(b) for V_{DD}, respectively.

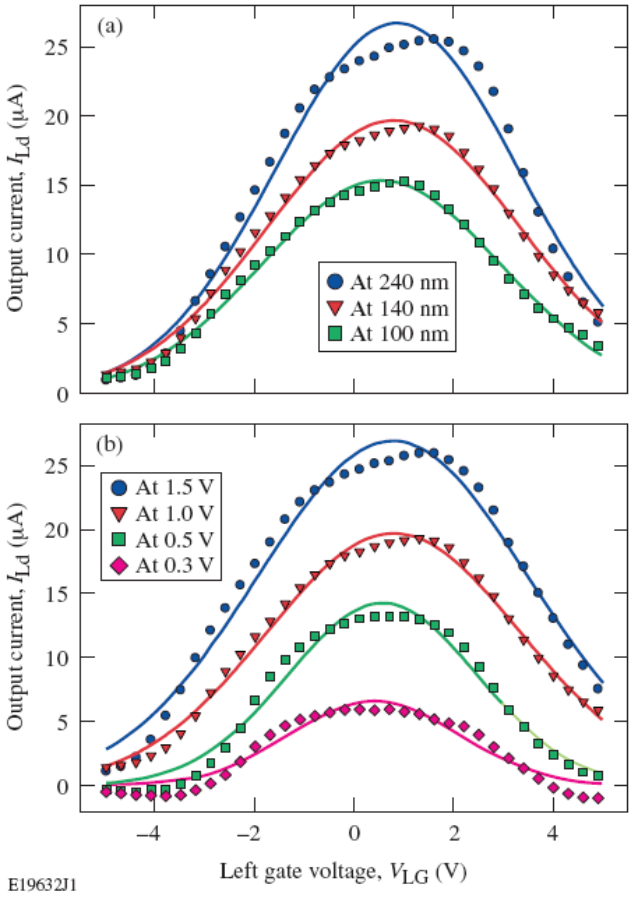

Fig. 10. *I*–*V* curves for (a) three BDTs with different channel widths: 240, 140, and 100 nm, respectively, and (b) different V_{DD} bias: 1.5, 1.0, 0.5, and 0.3, respectively, for the BDT with 140 nm. Symbols represent the experimental values while lines correspond to the compact model using Eq. (1) and parameters from Tables II and III.

A good agreement has been found between our compact model and experiments in I_D versus V_{LG} for all the BDTs. Tables II and III summarize the parameters used for the fitting calculations.

Current levels have been adjusted through the parameter "*a*," increasing from 15.4 μA for the smallest device to 26.7 μA for the largest one, and from 6.6 μA for V_{DD} = 0.3 V to 26.9 μA for V_{DD} = 1.5 V in the BDT with W_C = 140 nm. So the parameter "*a*" is a function of both W_C and V_{DD}. Also, the current peak voltage is clearly dependent, as expected, on the channel width and the drain bias; therefore, the parameter V_0 is also dependent on these values. Finally, the value of "*b*" is only connected to the change in supply voltage.

It is desirable to perform a more-systematic characterization and MC numerical simulation of the device to calibrate the model more precisely by including other possible influences such as gate length and shape, channel length, side channel angle, etc. Such a model, integrated into a behavioral Verilog-A module similar to [35]–[37], will certainly facilitate the exploration of more-complex BD-based structures.

TABLE II

PARAMETERS FOR THE COMPACT MODEL: CHANNEL WIDTH

Channel width (nm)*	*a* (μA)	*b* (V)	V_0 (V)
240	26.765	2.4416	0.8532
140	19.732	2.5557	0.7865
100	15.402	2.4056	0.5330

*Channel width defined in CAD.

TABLE III

PARAMETERS FOR THE COMPACT MODEL: DRAIN BIAS

V_{DD} (V)	*a* (μA)	*b* (V)	V_0 (V)
1.5	26.953	2.7192	0.7681
1.0	19.732	2.5557	0.7865
0.5	14.266	1.9060	0.5617
0.3	6.5988	1.6912	0.4057

VI. CONCLUSION

We have presented our efforts toward developing new logic circuits based on BDT devices. The Boolean logic behavior of the BDT-based gates has been verified through simulations using our custom MC tool. Preliminary evaluations show that the high operating speed and inherent binary behavior of the BDT makes it a viable candidate for extremely high performance in digital circuit applications.

Our study of the BDT has shown that these devices have a great potential to address issues currently faced by the continued scaling of CMOS technology. The challenges facing the BDT (and other emerging devices), however, are significant. Despite interesting properties offered by these devices, much more research and development is needed before they can find applications in mainstream integrated circuit design. Establishing a design flow for high-performance digital circuits using BDTs, similar to the well-established CMOS design flow, will require more efforts directed toward addressing issues like faster-interconnect development, power dissipation, level compatibility, optimum input/output impedance, reduction in routing complexity, better cost-effective (in time and money) fabrication, higher reliability, etc.

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