J Comput Electron (2015) 14:72–86
DOI 10.1007/s10825-014-0653-1

Monte Carlo modelling of noise in advanced III–V HEMTs

J. Mateos · H. Rodilla · B. G. Vasallo · T. González

Received: 27 October 2014 / Accepted: 1 December 2014 / Published online: 10 December 2014
© Springer Science+Business Media New York 2014

Abstract One of the main objectives of modern Microelectronics is the fabrication of devices with increased cutoff frequency and decreased level of noise. At this moment, the best devices for high-frequency, low-noise behavior are High electron mobility transistors (HEMTs) based on InGaAs and InAs channels. In this work, a complete analysis of ultra-short-gate HEMTs has been carried out by using a semi-classical Monte Carlo simulator, paying special attention to the noise performance. The validity of the model has been checked through the comparison of the simulated results with static, dynamic and noise measurements in real HEMTs. In order to reproduce the experimental results, we have included in the model some important real effects such as degeneracy, surface charges, presence of dielectrics and contact parasitics. The cryogenic performance of the HEMTs has also been analyzed. The influence of the parasitic resistances, width of the devices, value of the δ-doping and recess length has been analyzed when scaling down the gate length of the transistors to 50 nm aiming at achieving higher cutoff frequencies and better noise performance. The important effect of the impact ionization mechanisms and the consequent kink effect on the noise in both InGaAs and InAs based HEMTs have also been studied. Finally the advantages of the use of a double gate topology are quantified.

Keywords Noise · Heterojunction devices · HEMTs · Monte Carlo simulations · High frequency devices

J. Mateos (✉) · B. G. Vasallo · T. González
Departamento de Física Aplicada, Universidad de Salamanca, Plaza de la Merced s/n, 37008 Salamanca, Spain
e-mail: javierm@usal.es

H. Rodilla
Department of Microtechnology and Nanoscience, Chalmers University of Technology, Göteborg, Sweden

1 Introduction

One of the main problems found when trying to increase the operating frequency of a given active device is the degradation of the signal-to-noise ratio; in other words, the signal being amplified is hidden by the fluctuations generated by the device [1]. This problem is enhanced when dealing with low amplitude signals, originating from far emitters (as in the case of satellite communications, radio astronomy or remote sensing applications) or limited by power constraints (as in the case of mobile phones). Therefore, the improvement of the frequency performance of the devices must achieve not only the highest possible values of f_t (current gain cutoff frequency) and f_{max} (maximum frequency of oscillation), but also the lowest possible levels of noise. High electron mobility transistors (HEMTs) provide better performances than MESFETs, which in the past were the most popular high-frequency and low-noise devices. The reduction of the gate length is the typical way to enhance the high-frequency performance, and consequently the noise behavior of FETs. In fact, one possible way to diminish the noise figure of the transistors is to increase their cutoff frequency, since both are strongly linked [2]. However, the optimum bias conditions for minimum noise operation (at low current level) are not the same providing the maximum cutoff frequencies, so that, apart from the simple scaling rules, one must think about some alternative optimizations that can also be implemented in order to minimize the noise of the devices.

Important improvements can be obtained by using an adequate material system. The flexibility in the choice of the material composition of HEMTs has been made possible by the progress in material growth techniques, which permit the fabrication not only of high quality lattice matched heterojunctions but also pseudomorphic (strained) layers on both GaAs and InP substrates. Indeed, the cutoff frequencies of

pseudomorphic HEMTs (pHEMTs) using InGaAs channels with increased In content are much higher than those reached by usual lattice matched $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ HEMTs (LM-HEMTs). pHEMTs benefit from the superior mobility of the channel material and the higher energy barrier at the heterojunction, which leads to a stronger carrier confinement in the channel. High mobility narrow bandgap semiconductors such as InAs have also been used as channel materials in AlSb/InAs HEMTs (Sb HEMTs) [3,4], but technological difficulties (mainly related to growth defects and non-perfect heterojunctions) and the intrinsically narrow bandgap of InAs (and the consequent kink effect and gate leakage, associated with the onset of impact ionization mechanisms) have not allowed to outclass the performances obtained by InGaAs/AlInAs HEMTs by now. The best results have been obtained by using composite channels (made up with both InAs and InGaAs), leading to f_{max} above 1 THz [5], f_t of more than 700 GHz [6], and both f_t and f_{max} in excess of 640 GHz [7]. These remarkable results stem from the combination of the improvement of the channel transport properties with aggressive scaling (gate length below 30 nm together with gate to channel distances below 10 nm) and a crucial reduction of parasitics. Efforts are presently being made to improve the cost-competitiveness of HEMT electronics, basically focused on the promising metamorphic technology, in which the standard InGaAs/InAlAs epilayer is grown on GaAs substrates [8].

The impressive performance of Northrop Grumman's HEMTs [5] have allowed the fabrication of MMICs providing low noise amplification at 270 GHz with a noise figure of 7.5 and 11.4 dB gain [9], and almost enter the THz range, with an amplifier at 670 GHz with a noise figure of 13 and 8 dB gain [10]. Remarkable performances have also been obtained at 600 GHz with MMICs based on the 35 nm InGaAs HEMTs fabricated at Fraunhofer Institute [11]. But in spite of the recent technological advances, there are systems, mainly dedicated to radio astronomy, in which the room temperature noise of any present device is not sufficiently low. For such applications, it is necessary the use of cryogenically cooled low noise amplifiers (LNAs) [8,12,13], so that the understanding of the physical mechanisms at the origin of the noise in HEMTs at low temperature is also very important.

Moreover, III–V HEMTs have still some hitch to be removed, like the kink effect: an anomalous increase of drain current I_d at a certain high-enough value of the drain-source voltage (V_{ds}) [14,15]. Apart from a decrease in the gain, this effect emerges accompanied by a significant enhancement in the gate leakage current [16] and consequently poorer noise performance of the transistors [17]. This kink effect intensifies when decreasing the bandgap of the channel material (as happens when increasing the amount of In in InGaAs channels, aiming to reach higher mobility) and when scaling down the gate length of the devices (leading to increased electric fields), which also enhances the short channel effects. As a consequence, in order to optimize the high frequency or the low-noise behavior of the devices (that usually cannot be reached together) not only the gate-to-channel distance must be chosen carefully, but also many other technological parameters (both geometrical and electrical): width of the device, length, depth and position of the recess, thickness and doping of the different layers, etc. Historically, these parameters have been optimized by classical simulation techniques or, when such simulations are not applicable, by the expensive 'test and error' procedure. With the use of computer simulation, the design optimization can be made in a short time and with no money spent. However, classical modelling of electronic devices meets important difficulties when dealing with advanced transistors, mainly due to their small size, and the Monte Carlo (MC) technique appears as the most appropriate choice [18], in spite of requiring intensive computing resources.

In this work we will review the noise modelling of InGaAs and InAs HEMTs performed with a 2D ensemble MC simulator, the validity of which has been checked by means of the comparison with experimental results of static characteristics, small signal behavior and noise performance of fabricated HEMTs [13,19]. Using this MC simulator as analyzing tool, we can optimize the values of some key technological parameters, thus providing some useful design rules for the fabrication of HEMTs aiming to high-frequency and/or low-noise applications [20,21].

2 Monte Carlo simulator

Classical modelling of electronic devices meets important difficulties when dealing with ultra-short gate HEMTs mainly due to the appearance of high electric fields leading to quasi-ballistic transport and hot carrier effects. Moreover, in the case of heterojunction devices, the electron confinement can also give rise to quantum effects such as degeneracy, energy quantization in the channel and tunneling from the channel to the gate. If an exact description were required it would be necessary to self-consistently solve Poisson and Schrödinger equations, which, for the moment, is an unaffordable task in terms of computation time for a realistic dynamic simulation. In order to overcome these difficulties, we will make use of a semiclassical ensemble MC simulator coupled with a two-dimensional Poisson solver without considering neither the quantization of energy levels in the 2DEG, nor the quantum reflection or tunneling through the gate or the barrier at the heterojunction (classical laws of conservation of energy and momentum perpendicular to the heterojunction are used). The only quantum effect taken into account is the Pauli exclusion principle,

considered using the rejection technique described in [22], where the electron heating and nonequilibrium screening effects are introduced by using the local electron temperature [23,24]. Three non-parabolic spherical valleys (Γ, L and X) with ionized impurity, alloy, polar and non-polar optical phonon, acoustic phonon and intervalley scattering mechanisms are taken into account. Material parameters for the $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ heterojunction are reported in Ref. [23] and for InAs/AlSb in [25].

Ohmic boundary conditions [26] are considered at the drain and source contacts, with non-uniform profiles of potential and electron concentration (as if real top electrodes were used) [27,28]. The gate Schottky contact allows carriers to leave the device, but it does not inject them. The Schottky barrier height, V_{Sch}, is not included in our simulations, so it must be introduced externally.

The effect of the surface potential at the cap and recess surfaces of the device is modelled through a fixed negative surface charge (which is a good approximation at low biasing) that provokes carrier depletion in its surroundings [29–31]. The value of the surface charge is not the same in the whole device, since in the bottom of the recess the interface semiconductor is non-doped AlInAs (or AlSb in Sb-HEMTs), while in the rest it is the highly doped cap layer material. These two values of the surface charge will be taken as adjustable parameters that allow the fitting of the experimental I-V characteristics.

State-of-the-art InGaAs and InAs HEMTs are very susceptible to suffer impact ionization processes due to the small bandgap of the channel material and the very high electric fields appearing in the gate-drain region when the device dimensions are shortened to improve the operation frequency. Impact ionization and the subsequent hole dynamics (jointly with recombination processes) are responsible for the kink effect [14,15]. Kink phenomena, not completely understood in short-channel HEMTs, lead also to a large enhancement of the noise in the transistors [17]. We have included in the MC simulator all the processes causing the kink effect, essentially impact ionization and hole recombination. Electron impact ionization is implemented by using the Keldysh approach [32], with a probability per unit time

$$P(E) = \begin{cases} S\left(\frac{E-E_{th}}{E_{th}}\right)^2 & \text{if } E > E_{th} \\ 0 & \text{if } E > E_{th} \end{cases}, \tag{1}$$

where E is the electron kinetic energy, E_{th} the threshold energy and S a measure of the hardness or softness of the threshold. Hole impact ionization is negligible for the considered applied voltages. Typically, E_{th} and S are adjusted to reproduce the ionization coefficients measured experimentally [33,34]. Hole recombination is considered to take place with a characteristic time τ_{rec}, i.e. with a probability $1/\tau_{rec}$.

3 Parasitic elements: small signal equivalent circuit

In order to carry out the comparison of the measured results (extrinsic) with those obtained from the simulation (intrinsic), it is necessary to include in a post-processing stage the parasitic elements that are not present in the MC simulation. First, the source and drain contact resistances (R_s and R_d) must be included analytically in the calculation of the $I_d - V_{ds}$ characteristics [35] (since the simulations are performed at constant intrinsic V_{gs}, it is necessary to interpolate the results to obtain $I_d - V_{ds}$ curves at constant extrinsic V_{gs}). R_g does not affect the static results due to the null mean gate current.

The extrinsic small-signal equivalent circuit that we will use for the RF and noise calculations is shown in Fig. 1. The shaded area corresponds to the intrinsic section, represented by the most commonly used intrinsic equivalent circuit for HEMTs [29,36]. These intrinsic elements are extracted taking as a basis the Y parameters of the HEMT, calculated using the classical MC technique [37] (Fourier-transforming the transient gate/drain current response to voltage steps applied at both gate and drain contacts). For a correct comparison between the intrinsic experimental and simulated equivalent circuits, we have to consider that even when de–embedding the extrinsic parameters from the experimental results, there are still some effects that the MC is not accounting for, such as fringing and cross talk capacitances in the layout. Three extrinsic capacitances, C_{gs}^{ext}, C_{gd}^{ext} and C_{ds}^{ext}, must be added to the MC results to reproduce the effects associated with the topology of the metallic accesses to the devices. The values of these quasi-extrinsic capacitances are determined by fitting the experimental data at zero current, where it remains only the effect of the geometric (extrinsic and intrinsic) capacitances, independent of the biasing. The intrinsic equivalent circuit obtained from the MC simulation together with these additional capacitances correspond to the 'intrinsic' small-signal equivalent circuit from the point of view of exper-

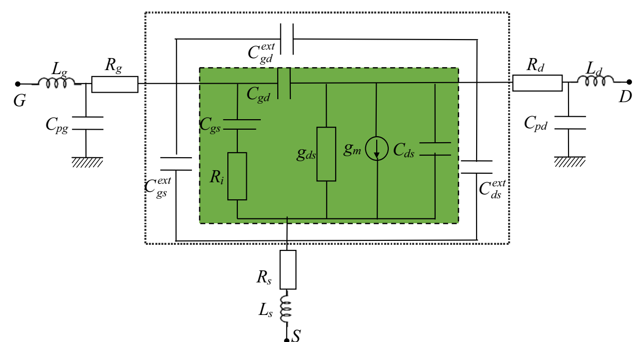

Fig. 1 Equivalent circuit of the devices. The *shaded area* represents the intrinsic elements that are obtained by the MC simulation, while the *dotted box* encloses the 'intrinsic' equivalent circuit from the point of view of experimental measurements (just excluding the contact parasitics)

imental measurements, which is determined excluding the effect of contact resistances, capacitances and inductances [36]. Thus, we must perform the comparison of the measured ‘intrinsic’ equivalent circuit with the coupling of the usual intrinsic circuit obtained from MC simulations and the extrinsic capacitances, which is represented in Fig. 1 inside the dotted box.

The intrinsic Y parameters of the HEMT obtained with the MC simulations, Y^{int}, are then modified as

$$Y'_{11} = Y^{int}_{11} + j\omega\left(C^{ext}_{gs} + C^{ext}_{gd}\right); \quad Y'_{12} = Y^{int}_{12} - j\omega C^{ext}_{gd},$$
$$Y'_{22} = Y^{int}_{22} + j\omega\left(C^{ext}_{ds} + C^{ext}_{gd}\right); \quad Y'_{21} = Y^{int}_{21} - j\omega C^{ext}_{gd}, \tag{2}$$

with ω the angular frequency and j the imaginary unit. At this point, the intrinsic small-signal equivalent circuit obtained from the new Y' parameters can be compared with that extracted experimentally from the measurement of the S parameters of the transistor (taking away the effect of the contact parasitics) [36].

Contact resistances have also been included in the extrinsic equivalent circuit. R_g has an important effect on the high frequency and noise behavior of the HEMTs, since in dynamic regime the gate current takes a significant value (which increases with frequency). In both static and dynamic calculations the values used for R_s, R_g and R_d (only R_s and R_d in DC) are similar to those measured experimentally. The capacitances and inductances of the contacts have not been considered for the noise calculations since they do not affect the noise figure of the device (the only sources of thermal noise are the contact resistances), they just change the optimal admittance for which the minimum noise figure is found.

4 Intrinsic noise parameters: *P*, *R* and *C*

Once the equivalent circuit elements and Y parameters are calculated, the noise characterization of the device can be performed. It requires firstly the calculation of the spectral densities of the drain- and gate-current fluctuations and its complex cross-correlation, S_{id}, S_{ig} and $S_{i_g i_d}$, respectively, by means of the Fourier transform of the corresponding correlation functions obtained from simulations of long current sequences (see Ref. [38]). Then the intrinsic dimensionless noise parameters P, R and C defined by Pucel et. al in [39] are determined as follows [2,40,41]

$$P = \frac{S_{i_d}}{4K_B T_0 |Y_{21}|}, \; R = \frac{S_{i_g}|Y_{21}|}{4K_B T_0 |Y_{11}|^2}, \; C = \frac{\mathrm{Im}\left[S_{i_g i_d}\right]}{\sqrt{S_{i_g} S_{i_d}}}, \tag{3}$$

where K_B is the Boltzmann constant and T_0 the reference temperature of 290 K. P, R and C represent the drain and gate noise sources and their cross-correlation, respectively, and can provide interesting information about the physical origin of the noise of the devices.

5 Practical description of noise: minimum noise figure

Even if the noise spectral densities and P, R and C parameters can provide physical information on the noise of the devices, from the point of view of practical applications it is much more useful to characterize the noise behavior of the transistors through their minimum noise figure, NF_{min}. The noise figure, NF represents the noise added by the device to the signal that it is amplifying, which has an absolute minimum, NF_{min}, when the input admittance is Y_{opt}. However, NF_{min} does not provide all the information about the noise, yet for a complete noise characterization four parameters are needed: NF_{min}, noise resistance, R_n, and the real and imaginary parts of the complex optimum admittance, Y_{opt} (or its corresponding complex reflection coefficient, $\Gamma_{opt} = \left(Y_0 - Y_{opt}\right)/\left(Y_0 + Y_{opt}\right)$, which is the commonly measured quantity, being Z_0=1/Y_0 the characteristic impedance of the system, generally 50 Ω). The intrinsic minimum noise figure, $NF^{\mathrm{int}}_{\mathrm{min}}$, can be calculated following the classic work of Rothe and Dahlke [42]

$$NF^{\mathrm{int}}_{\mathrm{min}} = 1 + 2R_n(Y_{cor} + Y_{opt}), \tag{4}$$

with

$$R_n = \frac{S_{i_d}}{4K_B T_a |Y_{21}|^2}, \quad Y_{cor} = \mathrm{Re}\left[Y_{11} - Y_{21}\frac{S^*_{i_g i_d}}{S_{i_d}}\right],$$
$$Y_{opt} = \sqrt{A - B}$$
$$A = |Y_{21}|^2 \frac{S_{i_g}}{S_{i_d}} + |Y_{11}|^2 - 2\mathrm{Re}\left[Y_{11} Y^*_{21}\frac{S_{i_g i_d}}{S_{i_d}}\right],$$
$$B = \mathrm{Im}^2\left[Y_{11} + Y^*_{21}\frac{S_{i_g i_d}}{S_{i_d}}\right], \tag{5}$$

where *, Re and Im stand for complex conjugate, real part and imaginary part, respectively, of the corresponding complex magnitude; Y_{cor} is the correlation admittance (associated to the correlation between gate and drain noise) and Y_{ij} the extrinsic Y parameters of the HEMT (calculated using the equivalent circuit of Fig. 1).

By determining all four noise parameters, not only the minimum noise figure of the device will be known, but also the admittance one has to connect in parallel to its input to obtain this optimum noise behavior, Y_{opt}. Moreover, the value of the noise resistance R_n informs on how the noise figure, NF, increases when the source admittance, Y_s, is different from Y_{opt} [leading to a reflection coefficient

$\Gamma_s = (Y_0 - Y_s)/(Y_0 + Y_s)$]. The expression for NF is [1]

$$NF = NF_{\min} + \frac{R_n}{\mathrm{Re}(Y_s)} \left| Y_s - Y_{opt} \right|^2 . \quad (6)$$

These four noise parameters are complemented with the associated gain, G_{ass}, which informs on the capability of the device to amplify a signal with minimum noise (with Y_{opt} connected to the input). G_{ass} is therefore the power gain of the configuration corresponding to the minimum noise condition and can be calculated as follows

$$G_{ass} = \frac{P_{out}}{P_{in}} = \frac{\mathrm{Re}(Y_{opt})}{\mathrm{Re}\left(Y_{22} - \frac{Y_{21}Y_{12}}{Y_{opt}+Y_{11}}\right)} \left| \frac{Y_{21}}{Y_{opt} + Y_{11}} \right|^2 . \quad (7)$$

Another important noise parameter from a practical point of view is the noise figure with the input matched ($Y_s = 1/Z_0 = 1/50\,\Omega^{-1}$ or, which is the same, $\Gamma_s = 0$). It is usually called $NF50$ (and $G50$ the corresponding gain)

$$NF50 = NF_{\min} + \frac{4R_n \left|\Gamma_{opt}\right|^2}{50 \left|1 + \Gamma_{opt}\right|^2} . \quad (8)$$

The value of $NF50$ is often employed to experimentally determine the value of R_n [1].

For the determination of the extrinsic noise parameters, in addition to the intrinsic noise sources, the parasitic elements of the equivalent circuit must be considered. The intrinsic noise is represented by means of the spectral densities (or equivalently, by the P, R and C parameters), while the extrinsic noise comes from the thermal fluctuations originated in the contact resistances, R_s, R_g and R_d. The method of extraction of the extrinsic NF_{min}, already presented in [19], is detailed in the work of Greaves and Unwin [43].

6 Monte Carlo versus analytical noise models

In order to better understand the influence of each of the intrinsic and extrinsic noise sources, the use of an analytical model for obtaining the behavior of NF_{min} in HEMTs, mainly at high frequency, would be extremely useful. The semi-empirical Fukui model [44] (with four empirical parameters, providing small insight into the physical origin of the noise) and the Pospieszalski noise model [45] (assuming ambient temperature at the gate resistance and no correlation between gate and drain noise; with only one free parameter, the drain temperature) have been widely used. However, they are not able to provide an accurate description of the noise of HEMTs as a function of the bias, temperature and frequency, as achieved by MC simulations not only under optimum noise tuning conditions but also for every input and output impedances connected to the device. Indeed, the noise behavior of state-of-the-art HEMTs cannot be explained by using simple approximations like those used in classical models for long channel devices, mainly because important elements of the small signal equivalent circuit of the devices (C_{ds}, C_{gd} and g_d) are not considered [2,39].

Following Pucel et al. [39], NF_{min} can be calculated as a power series of the frequency, f, through

$$NF_{\min} = 1 + 2\frac{f}{f_c}\frac{T_a}{T_o}\sqrt{K_g\left[K_r + g_m(R_s + R_g)\right]} + O\left[\left(\frac{f}{f_c}\right)^2\right], \quad (9)$$

with

$$K_g = P + R - 2C\sqrt{PR}, \quad K_r = \frac{PR\left(1 - C^2\right)}{P + R - 2C\sqrt{PR}}. \quad (10)$$

T_a and T_o are the ambient and the reference temperature, respectively, and $f_c = g_m/2\pi C_{gs}$ the intrinsic cutoff frequency. For low frequencies ($f << f_c$) Eq. (9) can be simplified by truncating the series at the first order term. By using $f_c = g_m/2\pi(C_{gs} + C_{gd})$, the results obtained using Eq. (9) agree well with the MC results, but only at low frequency, since more terms would be needed when f approaches f_c. Also, the frequency-dependent values of P, R, C and the elements of the small signal equivalent circuit lead to the failure of the model at high frequency. However, Eq. (9) is useful to understand the influence of both the intrinsic and extrinsic noise sources and helps to identify the qualitative contribution of each of them. For example, it is clear that the higher is C (gate and drain noise sources are more correlated) the lower is NF_{min} due to the cancellation between the drain- and gate-current noise sources, and also that the reduction of both R_s and R_g is of key importance for optimizing the overall noise performance of HEMTs.

Moreover, the use of the MC method has an important advantage over analytical models when dealing with the calculation of noise: no assumption is made about the values, correlation or location of the noise sources. On the contrary, the microscopic noise sources (the individual scattering mechanisms) are intrinsically accounted for. The same applies for the description of the dynamic response. The MC results do not rely on an specific configuration of the equivalent circuit; the values of the S or Y parameters of the transistors (and their frequency dependence) are directly computed from the detailed time-domain response resulting from the microscopically simulated transport processes.

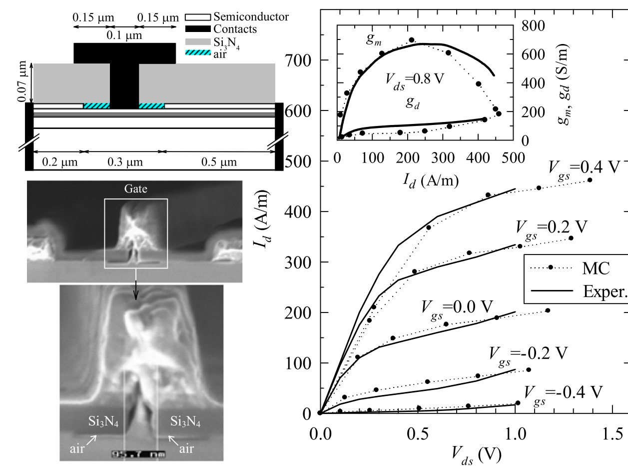

Fig. 2 Comparison of the $I_d - V_{ds}$ characteristics (also the extrinsic g_m and g_d are shown in the *inset* for $V_{ds} = 0.8$ V) measured in a real 100 nm-gate InGaAs HEMT with those obtained from the MC model (whose SEM images and simulated geometry are sketched at the *left*). From Ref. [21]

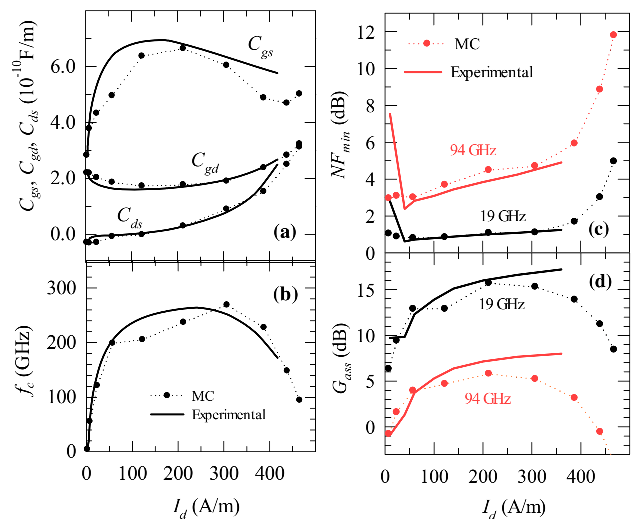

Fig. 3 Experimental measurements of **a** C_{gs}, C_{gd} and C_{ds}, **b** f_c, **c** NF_{min} and **d** G_{ass} at 19 and 94 GHz versus I_d for an extrinsic bias $V_{ds} = 0.8$ compared with the results of MC simulations. From Ref. [21]

7 Comparison with experimental results: 100 nm-gate InGaAs HEMT

Figure 2 shows the SEM images of the cross section of a real 0.1 µm recessed-gate δ-doped HEMT with 2×50 µm width fabricated at the IEMN. The layer structure of this HEMT, which has been considered in the simulations already presented in Refs. [23] and [46], consists of an InP substrate, a 300 nm $Al_{0.48}In_{0.52}As$ buffer followed by a 25 nm thick $In_{0.53}Ga_{0.47}As$ channel, three layers of $Al_{0.48}In_{0.52}As$ (a 5 nm spacer, a 5×10^{12} cm^{-2} δ-doped layer, modelled as a 5 nm layer doped at $N_D = 10^{19}$ cm^{-3} and a 10 nm Schottky layer), and finally a 10 nm thick $In_{0.53}Ga_{0.47}As$ cap layer ($N_D = 5 \times 10^{18}$ cm^{-3}). The simulated devices, sketched in Fig. 2, have exactly the same layer distribution as that of the real HEMT and nearly the same geometry.

By adjusting separately the surface charge at the cap layer and at the bottom of the recess (whose values are $\sigma_c = -6.2 \times 10^{12}$ cm^{-2} and $\sigma_r = -4.3 \times 10^{12}$ cm^{-2}, respectively) and using contact resistances of about 0.4 Ω.mm, the static $I - V$ characteristics of the real HEMT have been reproduced quite closely. The Schottky barrier height is taken to be 0.75 V. In Fig. 2 we can also observe that the kink effect begins to be significant at $V_{ds} > 0.8$ V, increasing the slope of the curves and worsening the agreement with these simulations (where this process is not taken into account). The inset of Fig. 2 presents the values of the extrinsic transconductance, g_m, and drain conductance, g_d, calculated from the I_d-V_{ds} curves, that show also a good agreement with the measurements.

The intrinsic elements of the small-signal equivalent circuit of Fig. 1 have then been extracted with MC simulations and compared with experimental measurements by adding the effect of the quasi-extrinsic capacitances C_{gs}^{ext}, C_{gd}^{ext} and C_{ds}^{ext} (with values of 220, 70 and −30 fF/mm, respectively). Figure 3a shows the experimental and simulated values of C_{gs}, C_{gd} and C_{ds} as a function of the drain current for an extrinsic drain voltage of 0.8 V. The intrinsic current gain cut-off frequency (Fig. 3b), $f_c = g_m/2\pi C_{gs}$, is also shown. A notable agreement between the experimental and simulated values of the equivalent-circuit elements is observed.

The simulated and experimental values of NF_{min} and G_{ass} at 19 and 94 GHz are plotted in Fig. 3c, d, both showing a very good agreement. Absolute minimum noise figure values of $NF_{min} \approx 0.8$ dB with $G_{ass} \approx 12.0$ dB @19 GHz and $NF_{min} \approx 3.0$ dB with $G_{ass} \approx 4.0$ dB @94 GHz are obtained at I_d about 60 A/m. By adjusting the reference plane for the measurements we have also obtained a good fitting for the experimental results of R_n and Γ_{opt} (whose values are strongly dependent on the position of such reference plane), for the first time using MC simulations [21].

8 Cryogenic operation of InGaAs HEMTs

Even if the well-established InP HEMT technology is known to provide the best transistors for cryogenic LNAs, few studies have been done in order to understand the physics at the origin of the improved noise performance of InP HEMTs at cryogenic temperatures [47,48]. Since the noise optimization at room temperature does not always work at cryogenic temperatures, models able to help improving the design at low temperature are extremely useful. As MC simulations intrinsically account for the electronic noise and ballistic or

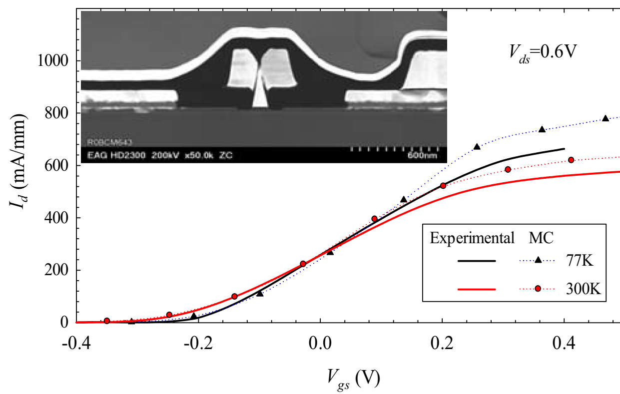

Fig. 4 I_d versus V_{ds} for $V_{ds} = 0.6$ V. Simulated results (*symbols*) versus experimental data (*lines*) at 300 and 77 K and STEM image of the fabricated InP-HEMT. From Ref. [13]

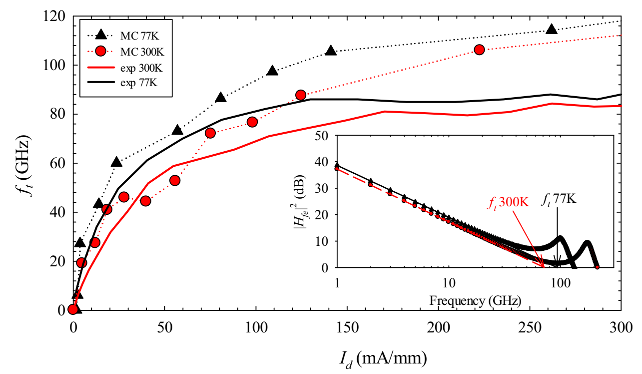

Fig. 5 Simulated (*symbols*, *dotted lines*) and experimental (*solid lines*) f_t versus I_d at 300 and 77 K, both for $V_{ds} = 0.6$ V. *Inset*: simulated $|H_{fe}|^2$ versus frequency at 300 and 77 K. Extrapolated f_t is marked. From Ref. [13]

quasi-ballistic transport, they are the perfect tool to perform the optimization of the noise of HEMTs at low temperature. Even if the usual operating temperature of cryogenic LNAs is 4–15 K, MC simulations have been made at 77 K in order to remain within the validity limits of our semiclassical approach. The study has been performed in a 130 nm-gate InGaAs HEMT fabricated at Chalmers University of Technology with a similar layer structure of that of Fig. 2 (in this case thinner channel and spacer of 15 and 3 nm, respectively, and smaller width of $2 \times 10\,\mu$m). More details are given in [8] and [13]. Using values of $\sigma_c = -5 \times 10^{12}\,\text{cm}^{-2}$ and $\sigma_r = -2.2 \times 10^{12}\,\text{cm}^{-2}$ (satisfying the experimental value of $n_s = 1.4 \times 10^{12}\,\text{cm}^{-2}$, nearly temperature independent), MC simulations reasonably reproduce the I-V curves of such HEMT at both 300 and 77 K, as shown in Fig. 4. Values of $R_s = 0.1\,\Omega$.mm and $R_d = 0.06\,\Omega$.mm have been considered at 300 K and $R_s = 0.05\,\Omega$.mm and $R_d = 0.03\,\Omega$.mm at 77 K. In good agreement with experimental results [8], parasitic resistances are halved when cooled from 300 to 77 K.

Figure 4 shows that for I_d above 300 mA/mm, the agreement between measurements and simulations is not perfect due to the kink appearing in the experiments (more pronounced at 77 K). This kink is not related to impact ionization since it happens for low values of V_{ds} (around 0.4 V) and we attribute it to the presence of traps. This mechanism was not included in the simulations and therefore the kink is not observed in the MC results. On the upside, we are interested in the low noise region, or what is the same, the low current region, not affected by this effect. And the important point is that a significant increase of the transconductance is observed in this region when decreasing temperature from 300 to 77 K. For $I_d = 50$ mA/mm g_m reaches a value of 1,200 mS/mm at 77 K when at 300 Kg_m was only 750 mS/mm.

In order to characterize the extrinsic dynamic performance of the HEMT, the cut off frequency f_t has been experimentally measured and obtained from the simulations (adding to the intrinsic MC results the influence of the parasitic elements shown in Fig. 1), taking as a base the frequency dependent current gain $|H_{fe}|^2$. As can be observed in the inset of Fig. 5, $|H_{fe}|^2$ shows the expected 20 dB/dec decay up to 50 GHz and the value of f_t has been obtained by taking the value for which the extrapolation of this slope goes to 0 dB. Even if MC results overestimate f_t (due to the underestimation of C_{gs} and g_d, mainly for I_d above 100 mA/mm), Fig. 5 shows a good agreement between the simulation results and the experimental measurements in the current range under study. The important result is the moderate increase of f_t when decreasing the temperature from 300 to 77 K (around 20 GHz for $I_d = 100$ mA/mm), mainly due to the enhancement of g_m (partially compensated by an increase of C_{gs}).

Intrinsic noise has been analyzed making use of the P, R and C noise parameters, calculated following Eq. (3) and shown in Fig. 6. It should be bear in mind that simulated values of R and C are not very precise due to the uncertainty in the MC calculation of the gate current fluctuations. The improvement in the intrinsic noise upon cooling is not so high, but a slight decrease of P and R and an increase in C can be observed when comparing the 300 and 77 K results. All of these variations contribute in the good direction for the reduction of the noise figure, shown in Fig. 7.

The minimum noise figure shows the typical U-shape, mainly due to the influence of R_n, which increases at both high (due to the increase of the drain noise, associated with the P parameter, Fig. 6a) and low drain current (due to the decrease of the cut-off frequency). Thus, NF_{min} exhibits a minimum at intermediate gate bias, for low I_d, the so called low-noise bias conditions. A minimum in the simulated NF_{min} of 0.15 dB (corresponding to a noise temperature 10 K) has been observed around 80 mA/mm at 300 K and of 0.05 dB at 20 mA/mm (noise temperature 3.36 K) at 77 K. In good agreement with these results, in the measurements made in a 4–8 GHz LNA, a minimum in the noise figure was observed at $I_d = 75$ mA/mm for 300 K and at $I_d = 15$ mA/mm for 10 K. This confirms that the low tem-

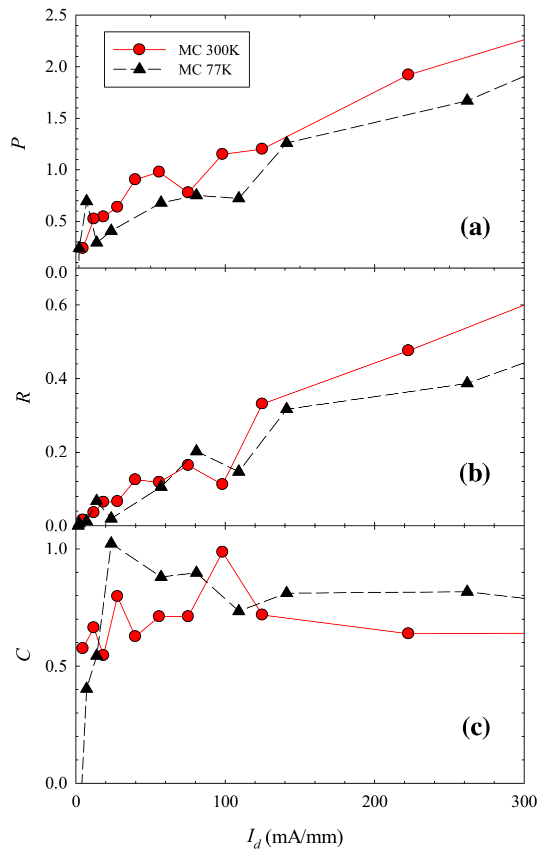

Fig. 6 Simulated intrinsic noise parameters **a** P, **b** R and **c** C as a function of the drain current for 300 and 77 K at $V_{ds} = 0.6$ V. From Ref. [13]

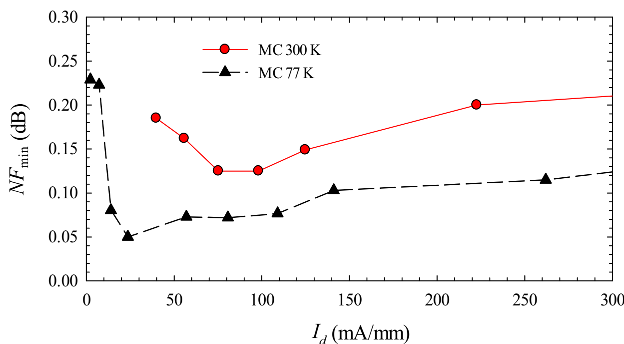

Fig. 7 Simulated minimum noise figure as a function of the drain current at 300 and 77 K @6 GHz at $V_{ds} = 0.6$ V. From Ref. [13]

perature MC simulations capture well the improvement in the noise due to the cooling, and also the optimum bias conditions, obtained for lower I_d, [13].

9 Optimization of the topology of InGaAs HEMTs

The reduction of the gate length, L_g, down to the technological limit (around 20 nm) is the main way to achieve the best

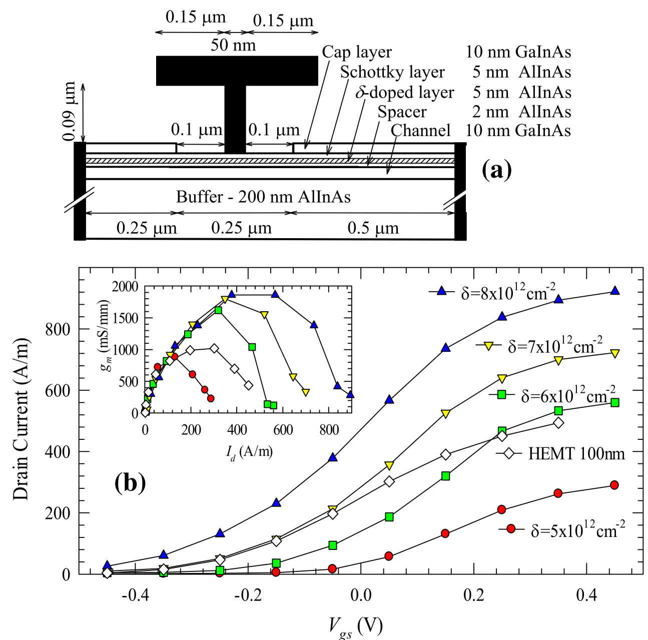

Fig. 8 **a** Schematic topology of the 50 nm LR-HEMTs. **b** I_d versus V_{gs} for the 100 and 50 nm LR-HEMTs with different values of the δ-doping (just 5×10^{12} cm^{-2} for 100 nm). $V_{ds} = 0.5$ V and the Schottky barrier height is taken to be 0.75 V for all of them. The *inset* shows the values of g_m versus I_d

performance of HEMTs. However, some constraints must be taken into account. When reducing the gate length it is convenient to keep constant the aspect ratio (gate length over gate-to-channel distance) in order to limit short-channel effects. This operation can lead to the appearance of other unwanted effects, like the depletion of the channel due to the surface potential or the tunneling of electrons from the channel to the gate. Here we will study the influence of important design parameters like the δ-doping level, the width of the devices and the recess length, in order to obtain their optimum values for maximum frequency and minimum noise operation in the case of 50 nm-gate HEMTs [20,21].

The geometry of the simulated devices, shown in Fig. 8a, is similar to that of the 100 nm-gate HEMT studied in Sect. 7 (see Fig. 2). Only the gate length and the thickness of the different layers are modified. In this case, the thickness of the channel is 10 nm and the gate-to-channel distance 12 nm. The aspect ratio decreases from 5.0 in the 100 nm device to 4.2 in the 50 nm one. Consequently, short channel effects are expected to be more important in the latter. The value of the δ-doped layer doping is a key parameter, since it must be sufficiently low to avoid conduction through it, but high enough to fill up the channel. The charge of the δ-doped layer must also be able to screen the influence of the surface charge placed on the recess, thus avoiding the depletion of the channel, effect which depends also on the gate-to-channel distance. The combination of all these effects can be easily

taken into account through the MC simulation of the transistor. We have performed the simulations with four different values for the δ-doping: 5, 6, 7 and 8×10^{12} cm^{-2}. The recess length has also a significant influence on the electric field profile inside the devices. In order to study its influence on the frequency and noise performance of the devices we have simulated 50 nm-gate HEMTs with a recess of 100 nm (denoted by LR-HEMTs, whose geometry is shown in Fig. 8a) and 20 nm (SR-HEMTs) at each side of the gate.

In Fig. 8b it can be observed that, with the same δ-doping of 5×10^{12} cm^{-2}, the current decreases when the gate length is reduced from 100 to 50 nm, although an increase was expected (due to an enhanced velocity overshoot of the electrons in the channel). The cause for this degradation of the transport properties is the depletion of the channel provoked by the surface charges lying in the bottom of the recess, whose effect is stronger due to a shorter distance to the δ-doped layer. To solve this problem the value of the δ-doping must be raised, thus increasing the current provided by the device. The increase of the current also enhances the transconductance, but has its negative counterpart; high values of the δ-doping lead to conduction through the δ-doped layer (parasitic channel), thus increasing the drain conductance (not shown) and degrading the extrinsic performance of the device. Also the values of C_{gs} and C_{gd} raise with a higher δ-doping, thus worsening the dynamic performance of the devices.

The extrinsic frequency performance of the devices can be characterized, in addition to the use of f_t, through the maximum frequency of oscillation, f_{max}, which corresponds to the frequency where the unilateral power gain, U, goes to unity. In order to obtain U and f_{max} (in parallel with $|H_{fe}|^2$ and f_t), the extrinsic Y parameters of the devices have been obtained with MC simulations by adequately introducing the values of the parasitic elements of the equivalent circuit. The maximum values of f_t and f_{max} for the 100 and 50 nm HEMTs are plotted in Fig. 9, showing that the reduction of the gate length allows improving the frequency performance of the HEMTs due to lower gate capacitances.

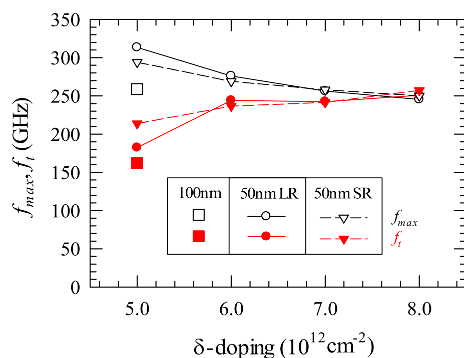

Fig. 9 Maximum value of f_t and f_{max} versus δ-doping for the 100 and 50 nm HEMTs. $V_{ds} = 0.5$ V

Figure 9 also shows that, while f_t increases, f_{max} decreases when increasing the δ-doping. The increase of f_t can easily be explained by the increase of g_m (which is more important than that of C_{gs}). Moreover, following the behavior of g_m, the most important enhancement is obtained when the δ-doping is raised from 5 to 6×10^{12} cm^{-2} (for higher values, both g_m and f_t are only slightly enhanced). The origin of the decrease of f_{max} with the δ-doping is the degradation of the g_m/g_d and C_{gs}/C_{gd} factors, which are important for f_{max} but do not affect the value of f_t. These dependencies were confirmed in [49], where the experimental results obtained in 130 nm gate HEMTs follow the trends predicted by our MC simulations in [20,21].

As concerns the dependence on the recess length, the static characteristics of the SR-HEMTs are practically the same as those shown in Fig. 8b for the LR-HEMTs. However, even if I_d and g_m are similar for both types of devices some slight differences appear: g_d increases and C_{gs} decreases when reducing the recess length (in qualitative agreement with the usual results in experimental devices). The lower C_{gs} leads to a higher f_t in the SR-HEMTs with respect to LR-HEMTs, but f_{max} is lower due to the increase of g_d.

In Fig. 10, NF_{min} at 94 GHz is represented together with G_{ass} as a function of the drain current for the 50 and 100 nm HEMTs. The dependence of the absolute minimum of NF_{min} (and its G_{ass} for the same bias point) on the value of the δ-doping is also shown. Figure 10a shows that for the same δ-doping of 5×10^{12} cm^{-2}, the 50 nm HEMT exhibits an improved NF_{min} with respect to the 100 nm device (2.4 against 3.0 dB), and for a lower current level. Another advan-

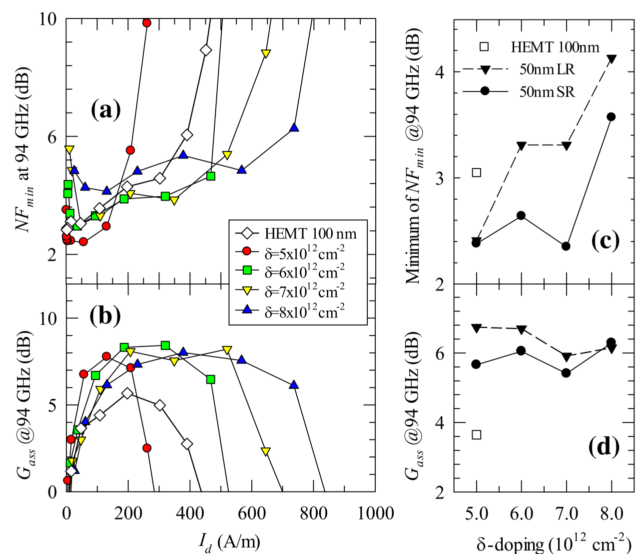

Fig. 10 Comparison of the 100 and 50 nm HEMTs with different δ-doping (just 5×10^{12} cm^{-2} for 100 nm) and recess lengths. **a** NF_{min} and **b** G_{ass} at 94 GHz versus I_d (for the LR-HEMTs with $V_{ds} = 0.5$ V). **c** Absolute minimum of NF_{min} and **d** corresponding G_{ass} (for the bias point of minimum noise) versus δ-doping

tage of reducing the gate length, from the point of view of low-noise operation, is the increase of G_{ass} (Fig. 10a), passing from 4 dB to more than 6 dB (value which is nearly independent of the δ-doping). Figure 10c, shows that a higher δ-doping increases the value of NF_{min}, but it is possible to minimize this degradation by shortening the recess length (due to the reduction of C_{gs}, that has a strong influence on NF_{min}).

The intrinsic MC simulation of the devices does not depend on the device width, W, since the only output parameter is the current, which scales linearly with W (the obtained current density is constant). However, the different dependence on W of the extrinsic elements of the equivalent circuit makes the extrinsic dynamic and noise behavior of the devices to be dependent on W. One can assume that the extrinsic capacitances C_{gs}^{ext} and C_{gd}^{ext} are directly proportional to W. However, for very short W, these geometric capacitances do not actually vanish but reach a certain saturation value due to fringing effects. This offset (the value that the capacitances take for $W = 0$) makes the relative effect of the parasitic capacitance to be more important and leads to a deterioration of f_t, f_{max} and NF_{min}. Figure 11 shows their values obtained with no offset and by considering offset values of 3.0 and 1.0 fF for both capacitances (in the range of the experimental values).

Figure 11a shows how f_{max} increases when decreasing W, reaching a quasi-saturated value when W is lower than 10–20 µm. However, if the correct model for the parasitic capacitances (with offset values) is used, it can be observed that the value of f_{max} first increases when reducing W, but only down to a certain value of W, for which f_{max} begins to decrease. Therefore, the maximum value of f_{max} is obtained for an intermediate value of W, around 50 and 30 µm if the offset is 3.0 and 1 fF, respectively. In the case of f_t, an important decrease is observed for low W when introducing the offset capacitances. In both cases it is more important the influence of the offset of C_{gd}^{ext} than that of C_{gs}^{ext}.

In order to show the dependence of the noise behavior on W, the values of NF_{min} and G_{ass}, together with those of $NF50$ and $G50$ are plotted in Fig. 11b, c. In the figure it can be observed how the reduction of the offset parasitic capacitances is very important for the improvement of the low-noise operation of the HEMTs (decrease of NF_{min} and increase of G_{ass}) mainly when W is lower than 50 µm. Again, the value of W for an optimum noise performance must be chosen as a tradeoff between the small width needed for the reduction of the gate resistance and a sufficiently large one for avoiding the effect of the offset parasitic capacitances and problems of matching. In fact, it is interesting to see that $NF50$ is less affected by the offset capacitances than NF_{min}, but both G_{ass} and $G50$ can be strongly degraded if the value of W is not adequate. From Fig. 11 it can be easily c that the high-frequency and low-noise performances of HEMTs can be much improved not only by adequately choosing its W, but also by reducing the value of the offset parasitic capacitances with an optimum design of the device masks (for example by using single finger gates [40], for which the offset capacitances are lower than with typical multifinger topologies).

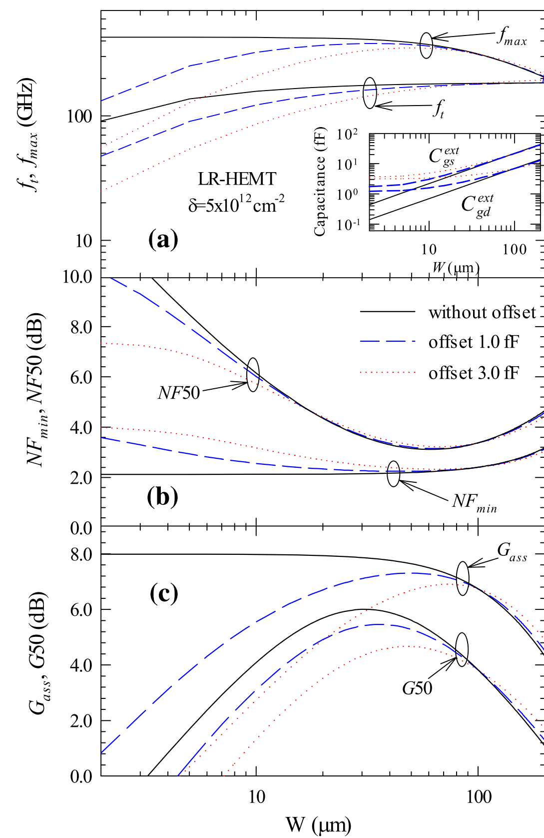

Fig. 11 **a** f_t and f_{max}, **b** $NF50$ and NF_{min}, and **c** $G50$ and G_{ass} at 94 GHz for the 50 nm LR-HEMT with $\delta = 5 \times 10^{12}$ cm^{-2} as a function of the width of the devices. Three different models for the extrinsic capacitances are used, without *offset* (*solid lines*), with *offset* of 1 fF (*dashed lines*) and 3 fF (*dotted lines*). The *inset* shows C_{gs}^{ext} and C_{gd}^{ext} versus W in the different models

10 Kink-effect related noise in InGaAs and InAs HEMTs

MC simulations, by providing information about the microscopic internal quantities of interest in the devices, allow identifying the physical origin of some peculiar behavior of HEMTs. Such is the case of the kink effect, present both in InGaAs and InAs transistors [15,50]. It consists in an anomalous increase in the drain current I_d at sufficiently high drain-to-source voltages V_{ds}, which leads to a reduction in the gain and a rise in the level of noise [17,51].

Even if the influence of kink effect on the DC, AC and noise behavior of the transistors is similar for both InGaAs and InAs technologies, its physical origin exhibits signif-

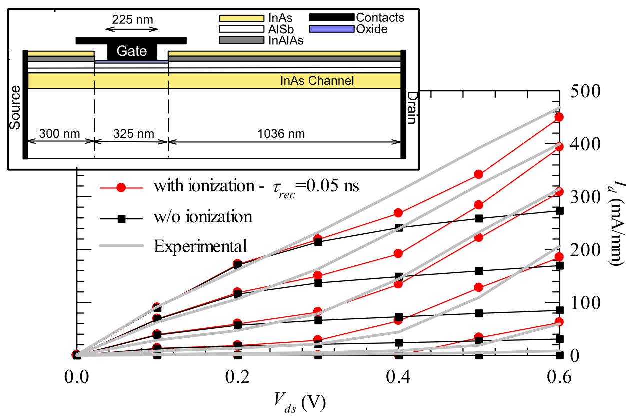

Fig. 12 Comparison between the experimental output characteristics and those obtained with MC simulations with and without impact ionization for the isolated-gate Sb-HEMT whose schematic topology is also shown. From Ref. [50]

icant differences, mainly related to the location inside the device of the holes (generated by impact ionization) at the origin the effect. For the analysis of this phenomenon is therefore essential to include in the model impact ionization events as well as hole recombination, that we consider following the models described in Sect. 2. We have obtained a good agreement between MC simulations and experimental measurements for the case of the 225 nm-gate InAs/AlSb HEMT of Refs. [49,50] (its geometry and output characteristics are shown in Fig. 12), whose gate is isolated in order to avoid the gate leakage. The best fit has been obtained when using contact resistances with values $R_s = 0.13\,\Omega$.mm and $R_s = 0.38\,\Omega$.mm, and setting the impact ionization parameters to $E_{th} = 0.41$ eV, $S = 10^{12}$ s^{-1} and $\tau_{rec} = 0.05$ ns.

MC simulations enable the identification of the physical origin of the kink effect in both InGaAs/InAlAs and InAs/AlSb HEMTs as follows [15,50]. For high enough V_{ds} the holes generated by impact ionization mechanisms, mainly in the gate-drain region, move towards the source contact. This happens for V_{ds} about 0.7 and 0.3 V for InGaAs and InAs HEMTs, respectively, when the gate-to-drain voltage provides the electrons with a kinetic energy similar to the bandgap of the channel semiconductor (0.75 eV for InGaAs and 0.35 for InAs). In the case of InGaAs HEMTs, the generated holes are confined in the channel (type I heterojunction) and tend to pile up under the source side of the gate, Fig. 13a. For the Sb-HEMT, the valence band discontinuity and the electric field benefit the descent of the holes towards the AlSb buffer (type II heterojunction), where they accumulate, mainly under the gate and at the gate-drain region of the transistor, Fig. 13b. Due to this pile-up of positive charge, the potential barrier which controls the passage of electrons through the channel is lowered, thus the channel is further opened and I_d increases, leading to the kink effect in the output characteristics. The rise of I_d is basically due to this

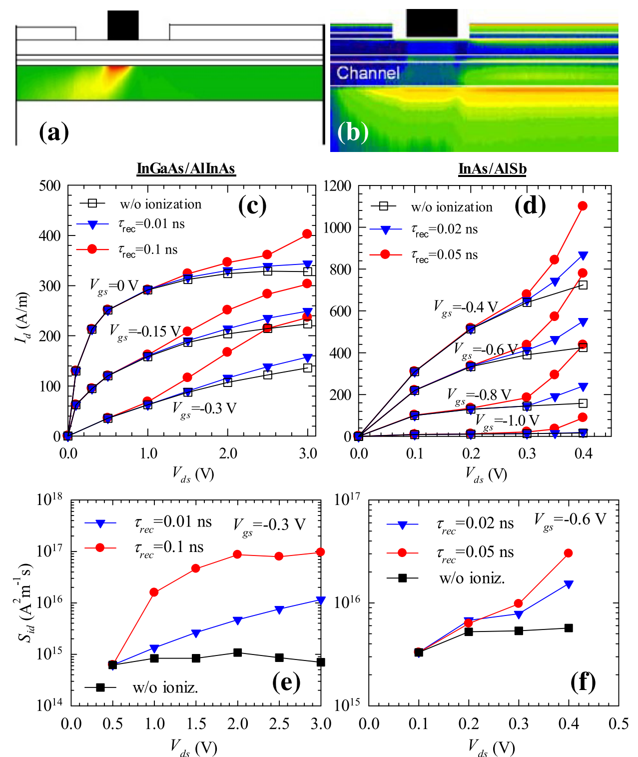

Fig. 13 Hole density map for the **a** InGaAs and **b** InAs HEMTs. MC simulations of the (**c**) and **d** output characteristics and (**e**) and **f** $S_{id}(0)$ versus V_{ds} obtained with and without considering impact ionization mechanisms. **c** and **e** correspond to the InGaAs HEMT, **d** and **f** to the InAs one. Two different values of τ_{rec} have been used: 0.01 and 0.1 ns for the InGaAs HEMT, and 0.02 and 0.05 ns for the Sb-HEMT

enhancement in the electron flow through the channel, since the number of electrons/holes generated by impact ionization is very low so as to provide a significant contribution to I_d.

In InAs HEMTs, the increase of I_d for a fixed V_{ds} due to the appearance of holes grows with V_{gs}. This behavior is the opposite of that found for InGaAs devices, in which the increase of I_d is lower for higher V_{gs}, which occurs because although the electron concentration in the channel is larger when the channel opens, the maximum electron energy is reduced due to the lower gate-to-drain potential. In the case of InAs HEMTs the bandgap is much smaller, thus impact ionization probability still remains significant for higher values of V_{gs}. Besides, impact ionization events take place not only near the maximum of electron energy (under the gate electrode), but all along the drain-side of the channel, where the electron velocity is higher when increasing V_{gs}.

Apart from this static effect, impact ionization and hole recombination lead to fluctuations of the hole concentration in the channel, particularly in the pile-up. Since these charge fluctuations are strongly coupled to the drain-current fluctuations by the high transconductance of the transistor, an important increase of the drain-current noise is expected to take place concurrently with the kink in the $I_d - V_{ds}$ curves.

The low-frequency value of S_{id}, Fig. 13e, f, is found to increase with V_{ds} (due to the higher number of impact ionization events) and τ_{rec}, both enhancing the pile–up of holes under the gate. The charge fluctuations in the hole pile–up are strongly coupled to the drain current fluctuations by the self-consistent potential (due to the strategic position of the holes, Fig. 13a, b), and they enhance $S_{id}(0)$. Indeed, $S_{id}(0)$ depends on V_{ds} and V_{gs} in a similar way to that shown by the kink-related increase of I_d: more pronounced for (i) higher V_{ds} and (ii) lower V_{gs} in InGaAs- and higher V_{gs} in Sb-HEMTs. However, the relative increase of $S_{id}(0)$ with respect to its value when impact ionization is not considered in the simulations is much higher than that of I_d. Thus, in conditions where the kink effect in the $I_d - V_{ds}$ curves is hardly detectable (for example when V_{ds} is just above the onset of impact ionization mechanisms, $V_{ds} = 1.0$ V for the InGaAs HEMT, Fig. 13c, and $V_{ds} = 0.3$ V for the Sb-HEMT Fig. 13d), $S_{id}(0)$ already exhibits a significant increase (Fig. 13e, f). This indicates that when HEMTs are biased in the vicinity of the kink onset, even if the static behavior of the transistors is not perturbed, their noise performance can be severely degraded, since drain noise is extremely sensitive to the dynamics of holes generated by impact ionization.

The cutoff of this excess noise should thus be related to the characteristic time of the fluctuations of the amount of accumulated holes. In fact, Fig. 14, corresponding to the InGaAs transistor, shows how the spectral density of drain-current fluctuations, $S_{id}(f)$, for the applied voltages for which impact ionization events take place ($V_{ds} > 1.0$ V), presents a low-frequency plateau (which is not present when impact ionization is removed from the simulations) whose cutoff frequency is linked to the impact ionization rate and the hole recombination time, thus being of the order of $1/\tau_{rec}$. At higher V_{ds} the level of the plateau increases, since the effect of impact ionization is more pronounced and the increment of I_d is larger, see Fig. 13c.

Within our MC model, which does not include gate tunneling, the gate noise at low frequency is null in the absence of impact ionization. In contrast, in the presence of the kink we find that it exhibits the expected full shot noise behavior; thus $S_{ig}(0)$ is close to $2qI_g$ (not shown) [17], being maximum when the device is near pinch-off, just where optimum noise conditions are obtained. This will lead to a degradation of the noise figure of the transistors due to the increase of both S_{id} and S_{ig}. As a consequence, kink effect must be avoided in order to improve the low-noise performance of HEMTs.

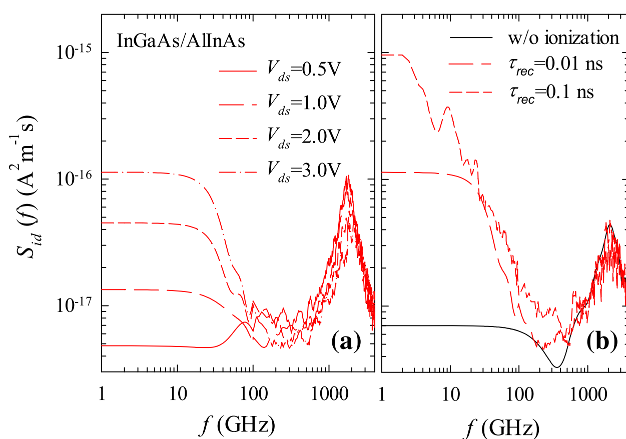

Fig. 14 $S_{id}(f)$ for $V_{gs} = -0.3$ V and **a** τ_{rec}=0.01 ns and different V_{ds}, and **b** $V_{ds} = 3.0$ V and different τ_{rec}, and also in the absence of impact ionization

11 Double gate InGaAs HEMTs

One possible way to enhance the performance of HEMTs is the use of the double-gate (DG) geometry (a gate is placed on each side of the conducting channel, Fig. 15) [52,53]. In spite of the technological difficulties for the fabrication of DG-HEMTs, they offer numerous advantages over conventional single-gate (SG) devices by providing a better charge control. Thus, the DG-device exhibits a better pinch-off behavior, lower g_d and higher g_m. The source and drain parasitic resistances are lower due to the higher electron concentration, and R_g is practically halved (two contacts are used), this leading to a considerably improved extrinsic dynamic behavior (in terms of f_{max}) [53]. Due to all these advances introduced by the DG-architecture, an improvement of the intrinsic and extrinsic noise performance is also expected. These expectations have been confirmed by the MC simulations of the 100 nm-gate DG-HEMT shown in Fig. 15 when compared with its SG counterpart (Fig. 2), see Ref. [53]. Figure 16 shows the good agreement obtained between MC simulations and experimental measurements of $I_d - V_{ds}$ curves (and also for the small signal equivalent circuit elements, before the onset of trapping effects for high V_{gs}).

Even if noise measurements were not performed for the DG-HEMT, the results obtained with MC simulations, Fig. 17, allow us to the compare the noise performance of both kind of topologies. P and R (Fig. 17a, b) take higher values in the SG-device. This happens because carriers in the

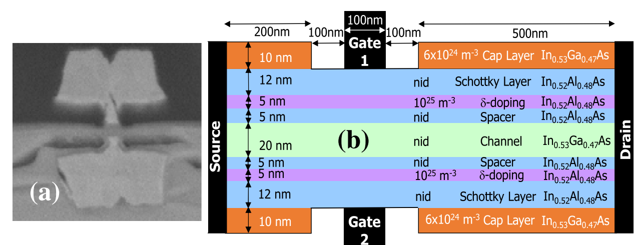

Fig. 15 **a** SEM image of a 100 nm-gate DG-HEMT fabricated at IEMN (Lille, France) and **b** schematic drawing of the simulated device

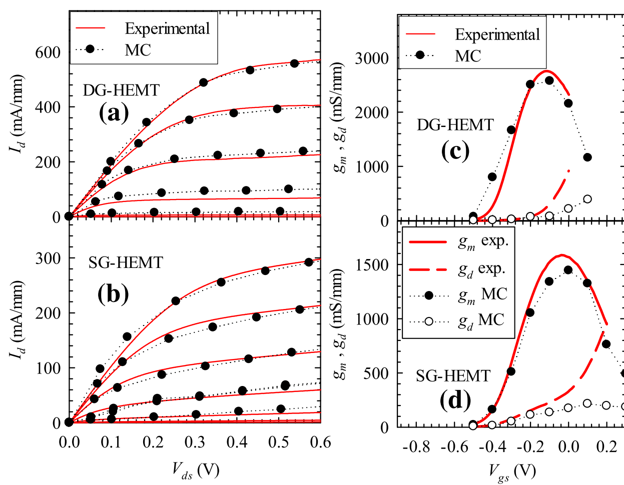

Fig. 16 Experimental and MC values of (**a**), **b** $I_d - V_{ds}$ and (**c**), (**d**) g_m versus V_{gs} (at $V_{ds} = 0.5$V) for the 100 nm-gate (**a**), **c** DG- and (**b**), (**d**) SG-HEMTs. The geometry of the SG-HEMT is the one shown in Fig. 2

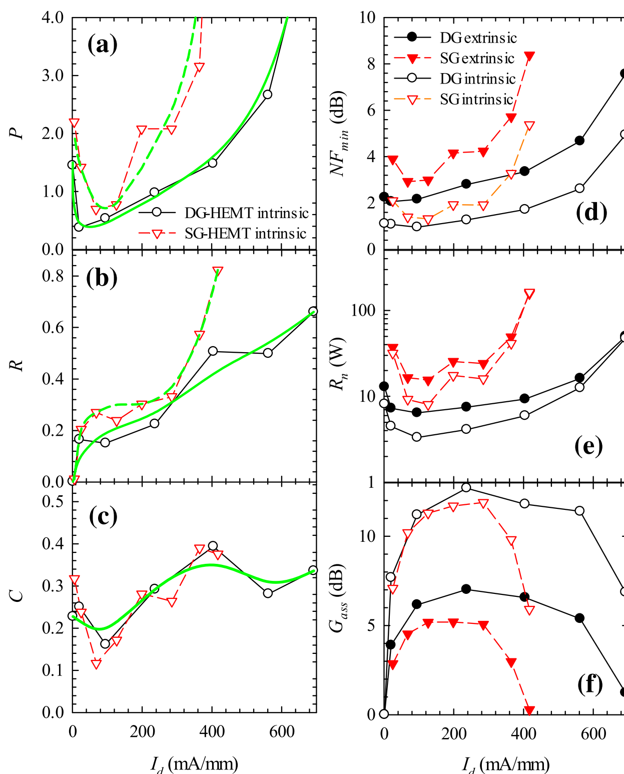

Fig. 17 MC values of the intrinsic **a** P, **b** R and **c** C parameters, and the intrinsic and extrinsic **d** NF_{min}, **e** R_n and **f** G_{ass} versus I_d for the 100 nm-gate DG- and SG-HEMTs. $V_{ds} = 0.5$ V. In (**a**)–(**c**) the corresponding tendency *lines* are also *plotted*

DG-device are completely confined in the channel and the current fluctuations due to electrons injected into the buffer are avoided. The change between low/high horizontal velocity of electrons in the buffer/channel leads to drain current fluctuations, while the associated vertical motion generates an excess of gate current noise. The suppression of these real space transfer processes reduces both drain and gate current noise. On the other hand, C is about the same for both types of devices, Fig. 17c, since the electron dynamics inside the channel and the gate-channel coupling are similar.

The extrinsic noise performance of the devices is described through the parameters NF_{min} and R_n together with G_{ass}. In Fig. 17 we present their MC values @94 GHz for $V_{ds} = 0.5$ V as a function of I_d for both DG- and SG-HEMTs. The corresponding intrinsic values, calculated without considering the parasitic contact resistances R_s, R_d and R_g, are also plotted for comparison. The intrinsic NF_{min} is lower in the DG- than in the SG-HEMT (the minimum values are 1.1 and 1.4 dB, respectively) due to the reduction of the intrinsic drain and gate noise (lower P and R). When the contact resistances are taken into account, the extrinsic NF_{min} is significantly improved by the use of the double gate architecture, not only due to the better intrinsic behavior but also to the lower parasitic contact resistances. The extrinsic R_n and G_{ass} are also much improved in the DG-structure, thus allowing both for a better noise matching and a higher gain at low noise conditions, and, as a consequence, a more flexible MMIC design.

12 Conclusions

We have performed an exhaustive analysis of static, dynamic and noise performance of InGaAs and InAs HEMTs by using a MC simulator whose results have been contrasted with experimental measurements. A very good agreement has been found in the $I_d - V_{ds}$ characteristics, small-signal and noise parameters, thus confirming the validity of the simulation model. The effect of the extrinsic elements of the small-signal equivalent circuit on the noise behavior of the devices has been analyzed, thus obtaining important information that can be used for the optimization of the fabrication process. We have found that the reduction of the gate resistance is the most efficient method for obtaining low-noise devices.

When scaling down the gate length below 100 nm, the simulations show that the noise level is deteriorated with the increase of the δ-doping; therefore, its value must be as low as possible while maintaining a sufficient level of current. A decrease of NF_{min} is observed when reducing the width of the devices, W, with a lower limit imposed by the offset value of the parasitic capacitances, that degrade the low-noise operation for small W. Moreover, the increase of R_n for low W leads to a considerable deterioration of $NF50$, thus being critical to work at the optimum matching conditions in order to achieve a low noise level. We have also confirmed that when reducing the recess length the $I - V$ characteristics of HEMTs are almost unchanged, but a slight degradation of f_{max} (due to the increase of g_d) and an improvement of

NF_{min} and $NF50$ (due to the reduction of C_{gs}) take place (with similar gains).

The effect of the impact ionization processes and the consequent kink effect on the noise of both InGaAs/AlInAs and InAs/AlSb HEMTs have also been studied. The kink is originated by the pile-up of holes that counteract the effect of the gate potential avoiding the channel pinch-off. Due to the different type of heterojunction, the accumulation of holes takes place at the source side of the gate in InGaAs/AlInAs HEMTs, while for Sb-HEMTs they are placed at the AlSb buffer (under the gate and at the gate-drain region). An important increase of the drain-current noise at low frequency takes place in the presence of the kink due to the strong coupling between the fluctuations of hole density in the pile-up and the drain current. The gate current is found to exhibit shot noise related to the hole gate-leakage current, thus taking the highest values near pinch-off, close to the optimum biasing conditions for low noise operation. We conclude that the kink effect strongly degrades the noise performance of HEMTs, even at microwave frequencies, due to the increase of both S_{id} and S_{ig}.

Finally we have confirmed the improvement obtained with the use of the double gate topology. The extrinsic noise behavior (in terms of NF_{min}, G_{ass} and R_n) is significantly enhanced due not only to the better intrinsic noise performance, but also to the lower R_s, R_d and R_g.

As overall conclusion, the MC technique has been shown to be a powerful tool for the analysis of noise in high-frequency semiconductor devices, in particular ultra-short gate HEMTs based on high mobility semiconductors such as InGaAs or InAs.

Acknowledgments The authors dedicate this paper to the memory of our beloved and respected Prof. Daniel Pardo, recently deceased, whose contribution was of key importance not only for the development of the models described here but also for his enthusiastic everyday efforts to push us to improve further. This work was performed in close collaboration with A. Cappy, S. Bollaert, V. Hoel, N. Wichtmann, X. Wallart, Y. Roelens, T. Parenty and F. Danneville (IEMN, France), J. Grahn, J. Schleeh, G. Moschetti, P.Å. Nilsson and N. Wadefalk (Chalmers University of Technology, Sweden) who fabricated the devices, provided the experimental data and contributed to the interpretation of the results. It was supported partially by the Spanish Ministerio de Economía y Competitividad through Project TEC2013-41640-R and by the Consejería de Educación de la Junta de Castilla y León through Project SA052U13.

References

1. Gonzalez, G.: Microwave Transistor Amplifiers, Analysis and Design. Prentice-Hall, Upper Saddle River (1997)
2. Cappy, A.: Noise modelling and measurement techniques. IEEE Trans. Microwave Theory Tech. **36**, 1 (1988)
3. Malmkvist, M., Lefebvre, E., Borg, M., Desplanque, L., Wallart, X., Dambrine, G., Bollaert, S., Grahn, J.: Electrical characterization and small-signal modeling of InAs/AlSb HEMTs for low-noise and high-frequency applications. IEEE Trans. Microw. Theory Tech. **56**, 2685–2691 (2008)
4. Moschetti, G., Wadefalk, N., Nilsson, P.Å., Roelens, Y., Noudeviwa, A., Desplanque, L., Wallart, X., Danneville, F., Dambrine, G., Bollaert, S., Grahn, J.: InAs/AlSb HEMTs for cryogenic LNAs at ultra-low power dissipation. Solid-State Electron. **64**, 47–53 (2011)
5. Lai, R., Mei, X. B., Deal, W. R., Yoshida, W., Kim, Y. M., Liu, P. H., Lee, J., Uyeda, J., Radisic, V., Lange, M., Gaier, T., Samoska, L., Fung, A.: Sub 50 nm InP HEMT device with f_{max} greater than 1 THz. In: Proceedings of the IEEE IEDM Conference of Dig., pp. 609–611. IEEE (2007)
6. Chang, E., Kuo, C., Hsu, H., Chiang, C.Y., Miyamoto, Y.: InAs thin-channel high-electron-mobility transistors with very high current-gain cutoff frequency for emerging submillimeter-wave applications. Appl. Phys. Express **6**, 3 (2013)
7. Kim, D.-H., del Alamo, J.A.: 30 nm InAs pseudomorphic HEMTs on an InP substrate with a current-gain cutoff frequency of 628 GHz. IEEE Electron Device Lett. **29**(8), 830–833 (2008)
8. Schleeh, J., Rodilla, H., Wadefalk, N., Nilsson, P.Å., Grahn, J.: Cryogenic noise performance of InGaAs/InAlAs HEMTs grown on InP and GaAs substrate. Solid-State Electron. **91**, 74 (2014)
9. Gaier, T., Samoska, L., Fung, A., Deal, W.R., Radisic, V., Mei, X.B., Yoshida, W., Liu, P.H., Uyeda, J., Barsky, M., Lai, R.: Measurement of a 270 GHz low noise amplifier with 7.5 dB noise figure. IEEE Microw. Wireless Compon. Lett. **17**(7), 546–548 (2007)
10. Deal, W.R., Mei, X.B., Leong, K., Radisic, V., Sarkozy, S., Gorospe, B., Lee, J., Liu, P.H., Yoshida, W., Zhou, J., Lange, M., Lai, R.: Terahertz monolithic integrated circuits using InP high electron mobility transistors. IEEE Trans. Terahertz Sci. Technol. **1**, 25–32 (2011)
11. Tessmann, A., Leuther, A., Massler, H., Seelmann-Eggebert, M.: A high gain 600 GHz amplifier TMIC using 35 nm metamorphic HEMT technology. In: Proceedings of the IEEE Compound Semiconductor Integrated Circuit Symposium, CSICS 2012, pp. 14–17. IEEE (2012)
12. Murti, M.R., Laskar, J., Nuttinck, S., Yoo, S., Raghavan, A., Bergman, J.I., Bautista, J., Lai, R., Grundbacher, R., Barsky, M., Chin, P., Liu, P.H.: Temperature-dependent small-signal and noise parameter measurements and modeling on InP HEMTs. IEEE Trans. Microw. Theory Tech. **48**, 2579 (2000)
13. Rodilla, H., Schleeh, J., Nilsson, P.Å., Wadefalk, N., Mateos, J., Grahn, J.: Cryogenic performance of low-noise InP HEMTs: a Monte Carlo study. IEEE Trans. Electr. Devices **60**(5), 1625–1631 (2013)
14. Somerville, M.H., Ernst, A., del Alamo, J.A.: A physical model for the kink effect in InAlAs/InGaAs HEMTs. IEEE Trans. Electron Devices **47**, 922–930 (2000)
15. Vasallo, B.G., Mateos, J., Pardo, D., González, T.: Monte Carlo study of the kink effect in short-channel InAlAs/InGaAs high electron mobility transistors. J. Appl. Phys. **94**, 4096–4101 (2003)
16. Kalna, K., Asenov, A.: Role of multiple delta doping in PHEMTs scaled to sub-100 nm dimensions. Solid-State Electron. **48**, 1223–1232 (2004)
17. Vasallo, B.G., Mateos, J., Pardo, D., González, T.: Kink-effect related noise in short-channel InAlAs/InGaAs high electron mobility transistors. J. Appl. Phys. **95**, 8271–8274 (2004)
18. Jacoboni, C., Lugli, P.: The Monte Carlo Method for Semiconductor Device Simulation. Springer, Vienna (1989)
19. Mateos, J., Pardo, D., González, T., Hoel, V., Cappy, A.: Monte Carlo simulator for the design optimization of low-noise HEMTs. IEEE Trans. Electron. Dev. **47**, 1950–1956 (2000)
20. Mateos, J., González, T., Pardo, D., Bollaert, S., Parenty, T., Cappy, A.: Design optimization of AlInAs-GaInAs HEMTs for high-frequency applications. IEEE Trans. Electron Devices **51**(4), 521–528 (2004)

21. Mateos, J., González, T., Pardo, D., Bollaert, S., Parenty, T., Cappy, A.: Design optimization of AlInAs-GaInAs HEMTs for low-noise applications. IEEE Trans. Electron Devices **51**(8), 1228–1233 (2004)
22. Fischetti, M.V., Laux, S.E.: Monte Carlo analysis of electron transport in small semiconductor devices including band-structure and space-charge effects. Phys. Rev. B **38**, 9721 (1988)
23. Mateos, J., González, T., Pardo, D., Hoel, V., Cappy, A.: Improved Monte Carlo algorithm for the simulation of δ-doped AlInAs/GaInAs HEMTs. IEEE Trans. Electron Devices **47**, 250 (2000)
24. Islam, A., Kalna, K.: Monte Carlo simulations of mobility in doped GaAs using self-consistent Fermi–Dirac statistics. Semicond. Sci. Technol., **26**, 055007 (9 pp) (2011)
25. Rodilla, H., González, T., Pardo, D., Mateos, J.: High-Mobility Heterostructures Based on InAs and InSb: a Monte Carlo study. J. Appl. Phys. **105**, 113705 (6 pp), (2009)
26. González, T., Pardo, D.: Physical models of ohmic contact for Monte Carlo device simulation. Solid-State Electron. **39**, 555 (1996)
27. Jensen, G.U., Lund, B., Fjeldly, T.A., Shur, M.: Monte Carlo simulation of short-channel heterostructure field-effect transistors. IEEE Trans. Electron Devices **38**, 840 (1991)
28. Mateos, J., González, T., Pardo, D., Tadyszak, P., Danneville, F., Cappy, A.: Noise and transit time in ungated FET structures. IEEE Trans. Electron Devices **44**, 2128 (1997)
29. Mateos, J., González, T., Pardo, D., Tadyszak, P., Danneville, F., Cappy, A.: Noise analysis of 0.1 μm gate MESFETs and HEMTs. Solid-State Electron. **42**, 79 (1998)
30. Babiker, S., Asenov, A., Cameron, N., Beaumont, S.P., Barker, J.R.: Complete Monte Carlo RF analysis of "real" short channel compound FETs. IEEE Trans. Electron Devices **45**, 1644 (1998)
31. Mateos, J., González, T., Pardo, D., Tadyszak, P., Danneville, F., Cappy, A.: Numerical and experimental analysis of static characteristics and noise in ungated recessed MESFET structures. Solid-State Electron. **39**, 1629 (1996)
32. Fischetti, M.V.: Monte Carlo simulation of transport in technologically significant semiconductors of the diamond and zinc-blende structures-part I: homogeneous transport. IEEE Trans. Electron Devices **38**, 634–649 (1991)
33. Pearsall, T.P.: Impact ionization rates for electrons and holes in Ga0.47In0.53As. Appl. Phys. Lett. **36**, 218–220 (1980)
34. Osaka, F., Mikawa, T., Kaneda, T.: Impact ionization coefficients of electrons and holes in (100)-oriented $Ga_{1-x}In_xAs_yP_{1-y}$. IEEE J. Quantum Electron. **21**, 1326–1338 (1985)
35. Babiker, S., Asenov, A., Cameron, N., Beaumont, S.P.: Simple approach to include external resistances in the Monte Carlo simulation of MESFETs and HEMTs. IEEE Trans. Electron Devices **43**, 2032 (1996)
36. Dambrine, G., Cappy, A., Heliodore, F., Playez, E.: A new method for determining the FET small-signal equivalent circuit. IEEE Trans. Microw. Theory Tech. **32**, 1151 (1988)
37. González, T., Pardo, D.: Monte Carlo determination of the intrinsic small-signal equivalent circuit of MESFETs. IEEE Trans. Electron Devices **42**, 605 (1995)
38. González, T., Pardo, D., Varani, L., Reggiani, L.: Monte Carlo analysis of the behavior and spatial origin of electronic noise in GaAs MESFETs. IEEE Trans. Electron Devices **42**, 991 (1995)
39. Pucel, P.A., Haus, H.A., Statz, H.: Signal and noise properties of gallium arsenide field effect transistors. Adv. Electron. Electron Phys. **38**, 195–265 (1974)
40. Klepser, B.H., Bergamaschi, C., Schefer, M., Diskus, C.G., Patrick, W., Bächtold, W.: Analytical bias dependent noise model for InP HEMTs. IEEE Trans. Electron Devices **42**, 1882 (1995)
41. Danneville, F., Happy, H., Dambrine, G., Belquin, J.M., Cappy, A.: Microscopic noise modeling and macroscopic noise models: how good a connection? IEEE Trans. Electron Devices **41**, 779 (1994)
42. Rothe, H., Dahlke, W.: Theory of noisy fourpoles. In: Proceedings of the IRE, vol. 44, pp. 811–818 (1956)
43. Greaves, S.D., Unwin, R.T.: Accurate noise characterization of short gate length GaAs MESFETs and HEMTs for use in low-noise optical receivers. Microw. Opt. Tech. Lett. **6**, 60 (1993)
44. Fukui, H.: Design of microwave GaAs MESFETs for broadband, low-noise amplifiers. IEEE Trans. Microw. Theory Tech. **MTT–27**, 643–650 (1979)
45. Pospieszalski, M.: Modeling of noise parameters of MESFETs and MODFETs and their frequency and temperature dependence. IEEE Trans. Microw. Theory Tech. **MTT–37**(9), 1340–1350 (1989)
46. Mateos, J., González, T., Pardo, D., Hoel, V., Cappy, A.: Effect of the T-gate on the performance of recessed HEMTs. A Monte Carlo analysis. Semicond. Sci. Technol. **14**, 864 (1999)
47. Pospieszalski, M.W.: Extremely low-noise amplification with cryogenic FETs and HFETs: 1970–2004. IEEE Microw. Mag. **6**(3), 62–75 (2005)
48. Endoh, A., Watanabe, I., Shinohara, K., Awano1z, Y., Hikosaka, K., Matsui, T., Hiyamizu, S., Mimura, T.: Monte Carlo simulations of electron transport in In0.52Al0.48As/In0.75Ga0.25As high electron mobility transistors at 300 and 16 K. Jpn. J. Appl. Phys. **49**, 114301–1–114301–5 (2010)
49. Malmkvist, M., Wang, S., Grahn, J.: Epitaxial optimization of 130-nm gate-length InGaAs/InAlAs/InP HEMTs for high-frequency applications. IEEE Trans. Electron Devices **55**, 268–275 (2008)
50. Vasallo, B.G., Rodilla, H., González, T., Moschetti, G., Grahn, J., Mateos, J.: Monte Carlo study of kink effect in isolated-gate InAs/AlSb high electron mobility transistors. J. Appl. Phys. **108**, 094505–1–094505–5 (2010)
51. Vasallo, B.G., Rodilla, H., González, T., Moschetti, G., Grahn, J., Mateos, J.: Kink effect and noise performance in isolated-gate InAs/AlSb high electron mobility transistors. Semicond. Sci. Technol. **27**, 065018-1–065018-5 (2012)
52. Wichmann, N., Duszynski, I., Wallart, X., Bollaert, S., Cappy, A.: Fabrication and characterization of 100-nm $In_{0.53}Al_{0.47}As$-$In_{0.52}Ga_{0.48}As$ Double-Gate HEMTs with two separate gate controls. IEEE Electron. Device Lett. **26**, 601–603 (2005)
53. Vasallo, B.G., González, T., Pardo, D., Mateos, J., Wichmann, N., Bollaert, S., Roelens, Y., Cappy, A.: Comparison between the dynamic performance of double- and single-gate AlInAs/InGaAs HEMTs. IEEE Trans. Electron Devices **54**, 2815–2822 (2007)