# Impact ionization and band-to-band tunneling in $In_xGa_{1-x}As$ PIN ungated devices: A Monte Carlo analysis

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(Received 3 October 2017; accepted 21 December 2017; published online 16 January 2018)

III-V Impact-ionization (II) metal-oxide-semiconductor FETs (I-MOSFETs) and tunnel FETs (TFETs) are being explored as promising devices for low-power digital applications. To assist the development of these devices from the physical point of view, a Monte Carlo (MC) model which includes impact ionization processes and band-to-band tunneling is presented. The MC simulator reproduces the *I-V* characteristics of experimental ungated $In_{0.53}Ga_{0.47}As$ 100 nm PIN diodes, in which tunneling emerges for lower applied voltages than impact ionization events, thus being appropriate for TFETs. When the structure is enlarged up to 200 nm, the ON-state is achieved by means of impact ionization processes; however, the necessary applied voltage is higher, with the consequent drawback for low-power applications. In InAs PIN ungated structures, the onset of both impact ionization processes and band-to-band tunneling takes place for similar applied voltages, lower than 1 V; thus they are suitable for the design of low-power I-MOSFETs. *Published by AIP Publishing.* https://doi.org/10.1063/1.5007858

## I. INTRODUCTION

Impact-ionization (II) metal-oxide-semiconductor FETs (I-MOSFETs) and tunnel FETs (TFETs) are being explored in order to achieve an improved digital performance in terms of the subthreshold swing (SS), $I_{ON}/I_{OFF}$ ratio, and ON-state drain-to-source voltage $V_{DS}$. While in conventional MOSFETs the SS is limited to ~60 mV/dec at room temperature, Si I-MOSFETs could provide an SS lower than 5 mV/dec.[1–3] However, the required $V_{DS}$ is still too large to be competitive with mainstream MOSFET technology, even when considering more sophisticated designs as in the Schottky-barrier-source I-MOS.[4] Other weak points of these devices are drain-induced barrier thinning and SS degradation due to hot carrier injection into the gate dielectric.[5] III-V materials could be an opportunity to reduce $V_{DS}$. Indeed, III-V MOSFETs can work at $V_{DS}$ lower than 0.5 V and deliver $I_{ON}$ currents near 1 A/mm,[6,7] but with a large value of SS, while reliability is still a drawback due to the degradation of the gate oxide.[8] As an alternative, we explore III-V I-MOSFETs for ultra-low power logic applications, because they can lead to an improvement on the reliability with respect to Si I MOSFETs (by reducing the carrier energy) and to a decrease of $V_{DS}$ due to the higher II coefficient of III-V high-mobility narrow-bandgap materials. However, in III-V structures tunneling tends to appear for lower $V_{DS}$ than II processes, and tunnel-FETs (TFETs)[9–11] are the mainstream approach for ultra-low SS digital applications. Nevertheless, I-MOSFETs, where SS is expected to be lower than the few tens of mV/dec already demonstrated in TFETs, could become a feasible alternative.

In order to assist the design process of III-V I-MOSFETs and TFETs from the physical point of view, this work reports the analysis of the competition between the II and band-to-band tunneling to originate the current onset in ungated $In_xGa_{1-x}As$ structures, with $x$ ranging from 0.53 to 1.0. This competition can be more clearly studied in ungated diodes, where the physics of both processes can be explored at a material level detached from the gating dynamics. To this aim, we make use of a Monte Carlo (MC) model that has been validated by means of a comparison with the experimental *I-V* curve of an $In_{0.53}Ga_{0.47}As$ 100 nm PIN ungated structure.

## II. PHYSICAL MODEL

For the analysis, we make use of an ensemble MC simulator self-consistently coupled with a 2D Poisson solver,[12] which includes a detailed model for the process on the basis of the current emerged in reverse bias conditions, i.e., II processes and band-to-band tunneling.

The model for electron transport includes three non-parabolic spherical valleys (Γ, L, and X) with ionized impurity, alloy, polar, and non-polar optical phonon, acoustic phonon, and intervalley scattering mechanisms. More details are reported in Refs. 12 and 13. The model used for hole dynamics, essentially due to the presence of the P-region, involves a typical spherical non-parabolic valence band structure, with the hole effective mass $m_H^* = \left(m_{HH}^{*\,3/2} - m_{LH}^{*\,3/2}\right)^{2/3}$, taking into account jointly the heavy (H)- and light (L)-hole bands. Ionized impurity, acoustic, polar, and non-polar optical phonon scattering mechanisms are considered.[14,15] The parameters can be found in Refs. 16 and 17. Even if this effective mass model for the conduction and valence band structure is at the limit of validity for the energies involved in impact ionization processes, it is able to fit rather well the experimental results.[16,17] Minority carriers are considered in the simulations by injecting through the contacts those corresponding to the

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intrinsic carrier concentration $n_i$ of the intrinsic region of the PIN diode. The Ramo-Shockley theorem[18] is employed for obtaining the current in each contact.

The simulator incorporates the II processes for both electrons and holes by means of the Keldysh approach,[19,20] where the probability per unit time of having an II event is $P(E) = S\left[(E - E_{th})/E_{th}\right]^2$ when $E > E_{th}$ and 0 otherwise, where $E$ is the carrier kinetic energy, $E_{th} = 1.08 \cdot E_{GAP}$ is the ionization threshold energy, and $S$ is a measure of the softness or hardness of the threshold. $S$ is considered as an adjustable parameter.[16,17,19,20] The model has been calibrated against experimental measurements and widely accepted numerical results of the impact ionization coefficient in bulk materials.[20–23] In our analysis, we consider $S = 10^{12}\,\mathrm{s}^{-1}$, a value for which both electron and hole II coefficients remain within the realistic range for all the materials under analysis.[16,17] Higher precision could be obtained by using more sophisticated (but more computer intensive) approaches like full-band MC models.[24–26]

To take into account band-to-band tunneling, the transmission coefficient $T_C$ at energy $E$ along the longitudinal dimension is determined for each energy following the Wentzel-Kramers-Brillouin (WKB) method,[27] typically used when dealing with direct bandgap semiconductors[10,28]

$$T_C(E) = \exp\left[\frac{-2}{\hbar}\int_{x_1}^{x_2}\sqrt{2m^*[qV(x) - E]}dx\right], \qquad (1)$$

where $\hbar$ is the reduced Planck constant, $m^*$ is the effective mass of the tunneling carriers, and $qV(x)$ is the shape of the energy barrier provided by MC simulations, self-consistently calculated from the potential profile $V(x)$ obtained at each time step ($\Delta t = 0.5$ fs) by solving the Poisson equation.[29–31] $x_1$ and $x_2$ are the classical turning points for $qV(x)$, i.e., the boundaries of the energy barrier, see Fig. 1(a). The consideration of transverse states in the calculation of the tunneling probability is still controversial.[32] They are taken into account in many cases, in particular for gated devices.[33–35] In our case, we neglect the influence of transverse states since the high electric field, small effective mass, and narrow bandgap in the semiconductors under study minimize their role.[32]

In the Y-direction, the 2D MC domain is discretized into $n_r$ rows of thickness $\Delta y_k$. For each row $k$, the tunneling region comprises $j_{max}$ sections along the X-direction, coinciding with the meshes of the MC simulation. The tunneling energy range corresponding to each section $j$ has been discretized into $n_{sb}$ subintervals, as illustrated in Fig. 1(a). The charge per unit length in the non-simulated direction to be tunneled in the energy subinterval $i$ of the section $j$ in the row $k$ is[27]

$$Q_i(j,k) = K \cdot \Delta t \cdot \Delta y_k \cdot T_C(E_i(j)) \cdot [f_{source}(E_i(j)) - f_{drain}(E_i(j))] \cdot N_{source}(E_i(j)) \cdot N_{drain}(E_i(j)) \cdot \Delta E_i(j)$$
$$i = 1, \ldots, n_{sb}; \quad j = 1, \ldots, j_{max}; \quad k = 1, \ldots, n_r. \qquad (2)$$

$f_{source}(E)$ and $f_{drain}(E)$ are the Fermi-Dirac distribution functions in the P-side and the N-side regions, respectively.

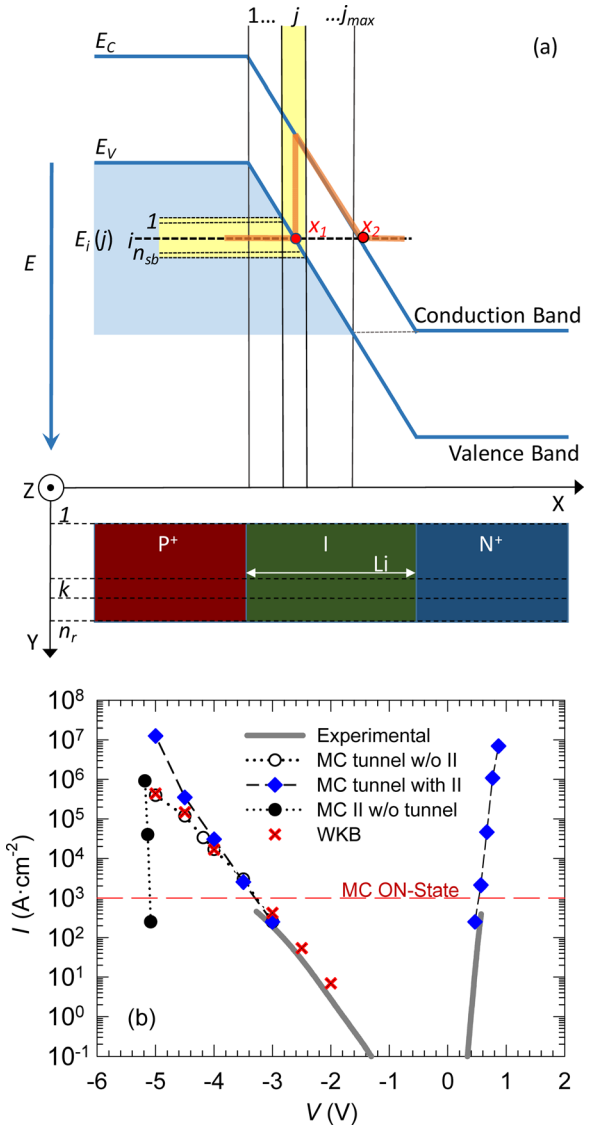


FIG. 1. (a) Schematic drawings of the energy bands with the discretization of the 2D MC domain and energies for the calculation of the tunneled charge ($x_1$ and $x_2$ are the returning points), and a PIN ungated device (Li denotes the length of the intrinsic region). The area in blue corresponds to the energy range where tunneling can take place. (b) Comparison between the experimental and MC $I$–$V$ curves of an $In_{0.53}Ga_{0.47}As$ 100 nm PIN diode. In reverse bias, the MC values obtained considering exclusively impact ionization mechanisms or band-to-band tunneling in the simulations and the theoretical WKB values for band-to-band tunneling have been also plotted.

$N_{source}(E)$ and $N_{drain}(E)$ are the density of states in the P-side and the N-side regions, respectively. $E_i(j)$ is the energy value corresponding to the energy subinterval $i$ in the section $j$, $\Delta E_i(j) = \Delta E_{i+1}(j) - \Delta E_i(j)$. $T_C(E_i(j))$ is the transmission coefficient for the energy $E_i(j)$. According to this discretization, the $x_1$ and $x_2$ coordinates are calculated for every $E_i(j)$ as shown in Fig. 1(a). $K$ is a global proportionality constant that includes, among other quantities, the electron and hole effective masses during the tunnel transmission and the Richardson constant. $K$ is taken as an adjustable parameter to reproduce the experimental $I$–$V$ curves in reverse bias conditions.[29–31] Our model has been calibrated and further validated by comparison of the MC $I$–$V$ characteristic with the experimental $I$–$V$ measured in a similar fabricated

$In_{0.53}Ga_{0.47}As$ 100 nm PIN diode, as will be shown in Sec. III. As a result, a value of $K = 2.2 \times 10^{46}$ A m$^{-2}$s$^{-1}$ is adopted.

The number of particles tunneled at a given $\Delta t$ through the whole structure is[29]

$$N_p = \sum_{k=1}^{n_r} \sum_{j=1}^{j_{max}} \sum_{i=1}^{n_{sb}} n_{p;i}(j,k) = \sum_{k=1}^{n_r} \sum_{j=1}^{j_{max}} \sum_{i=1}^{n_{sb}} \left(\frac{1}{q}\right) Q_i(j,k) \cdot Z, \tag{3}$$

where $n_{p;i}(j,k)$ is the number of pseudo-particles tunneled at the energy subinterval $i$ in section $j$ of row $k$, with $Z$ being the non-simulated dimension.

Poissonian statistics is employed to include the randomness of the tunneling processes by defining the rate $\Gamma = N_p/\Delta t$ used to determine the time between two consecutive tunneled particles as $t_{tunnel} = -\ln(r)/\Gamma$, with $r$ being a random number uniformly distributed between 0 and 1. The specific energy subinterval $m$, section $s$ (with the corresponding $x$-position), and row $l$, where a given particle will emerge after a tunnel process, are determined from the condition[29]

$$\sum_{k=1}^{l} \sum_{j=1}^{s} \sum_{i=1}^{m} n_{p;i}(j,k) \le r' N_p \le \sum_{k=1}^{l} \sum_{j=1}^{s} \sum_{i=1}^{m+1} n_{p;i}(j,k), \tag{4}$$

with $r'$ being a random number uniformly distributed between 0 and 1. The specific $y$ position inside the selected subsection $s$ is determined randomly, considering a uniform probability along the mesh.

From the energy level selected for each tunneled electron, the momentum component parallel to the tunneling direction is considered to be null ($k_x = 0$) and the thermal energy distribution is used to determine $k_y$ and $k_z$. A hole in the valence band of the P-side region of the intrinsic region also emerges with $k_x = 0$ and the thermal energy distributed in $k_y$ and $k_z$.

## III. RESULTS

As mentioned, our model has been calibrated and validated by comparison of the MC results with the experimental *I–V* characteristics of an $In_{0.53}Ga_{0.47}As$ 100 nm PIN diode, as shown in Fig. 1(b). In the case of reverse bias, simulations with and without considering II processes and/or tunneling have been carried out in order to determine the respective influence. The values of the experimental current density are limited to 0.1 A (corresponding to 460 A cm$^{-2}$), too small to be directly compared with the MC results because of the lack of statistical resolution (for such low current densities, a very small number of particles contribute to the current). However, since the dominating current mechanisms at such low current densities are tunneling, even if no particle is tunneled, it is possible to estimate the tunneling current by means of the WKB model from the potential profile provided by MC simulations in the corresponding range of applied voltages. As observed in Fig. 1(b), by using $K = 2.2 \times 10^{46}$ A·m$^{-2}$s$^{-1}$, the agreement between the WKB estimation based on the MC potential profiles and experiments is very good; and also with the MC results calculated from tunneled particles (in the absence of impact ionization) for higher voltages, when enough statistical resolution is achieved. This agreement validates the WKB model.

Figure 1(b) indicates that tunneling is the mechanism leading to the current onset in reverse bias conditions, since II processes are non-existent up to applied voltages $|V| \ge 5.0$ V when they are exclusively considered in the simulation. This occurs because the intrinsic carrier density at room temperature, $n_i = 8.4 \times 10^{11}$ cm$^{-3}$ [see the inset of Fig. 3(c)], is too low to have a significant amount of carriers susceptible of suffering II. As well, $E_{GAP} = 0.74$ eV and $E_{th} \sim 0.8$ eV, leading to a relatively low impact ionization coefficient for low carrier energies, so that II just appears from carriers previously emerged by tunneling, clearly enhancing the current. Gated devices based on $In_{0.53}Ga_{0.47}As$ are then found to be appropriate for TFET structures and not suitable for I-MOSFETs, even if the presence of II could improve the SS thanks to the drastic increase of the current they originate. In direct bias conditions, the expected exponential current is found for voltages below the built-in potential (0.82 V in this case).

Other candidates with higher intrinsic carrier density and narrower bandgap, thus, more prone to II events, have been evaluated. In particular, for $In_{0.7}Ga_{0.3}As$ at room temperature: $n_i = 1.4 \times 10^{13}$ cm$^{-3}$ and $E_{GAP} = 0.59$ eV; and for InAs, $n_i = 1.01 \times 10^{15}$ cm$^{-3}$ and $E_{GAP} = 0.35$ eV. MC simulations considering exclusively II events or tunneling have been performed in order to determine which is the process at the origin of the onset of the current in reverse bias conditions. To this aim, the threshold voltage $V_{th}$ is defined as the applied voltage necessary for $I_{ON} \ge 10^3$ A cm$^{-2}$ [indicated in Fig. 1(b) for clarity]. $V_{th\_II}$ denotes $V_{th}$ when considering exclusively II processes in the simulations and $V_{th\_tunnel}$ when considering exclusively band-to-band tunneling.

The MC values of $V_{th\_II}$ and $V_{th\_tunnel}$ for $In_xGa_{1-x}As$ (for $x = 0.53$, 0.7, and 1.0) when considering (a) 100 nm and (b) 200 nm PIN diodes at room temperature are plotted as a function of the indium mole fraction $x$ in Fig. 2. For the 100 nm PIN structures based on $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$, $V_{th\_II} > V_{th\_tunnel}$ indicating that tunneling is the sole mechanism initiating the ON-state in both cases. Interestingly, the values of $V_{th\_II}$ and $V_{th\_tunnel}$ for the InAs 100 nm structure are low and relatively close. Thus, $I_{ON}$ could be originated by both II processes and tunneling, and the SS could be noticeably enhanced by the strong presence of II events. Gated InAs 100 nm devices can be then used in the design of low-power low-SS I-MOSFETs.

When considering $In_{0.53}Ga_{0.47}As$ 200 nm structures, $V_{th\_II} < V_{th\_tunnel}$, thus allowing designs for I-MOSFETs, but with high values of $V_{th}$ and the consequent drawback for low-power applications. To further illustrate this radical change with respect to the case of 100 nm diodes, the inset of Fig. 2(b) presents the corresponding *I–V* curves when considering II or tunneling separately in the simulations. For $In_{0.7}Ga_{0.3}As$ and InAs structures, $V_{th\_II} \sim V_{th\_tunnel}$. In the particular case of InAs structures, $V_{th}$ takes values under 1 V, being the more suitable candidate for designing I-MOSFETs.

In order to understand in depth the physical behavior of the analyzed structures, Fig. 3 presents the MC values of $V_{th\_II}$ and $V_{th\_tunnel}$ as a function of temperature $T$ for (a)

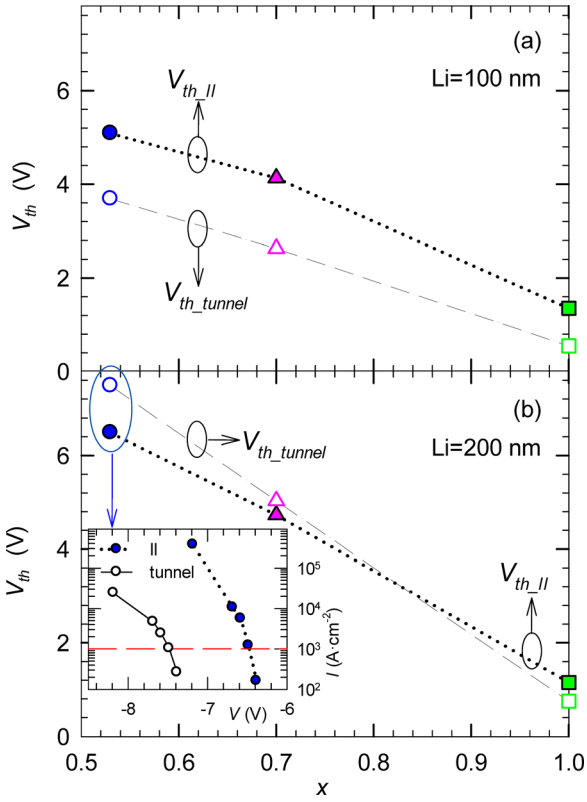


FIG. 2. MC values of $V_{th\_II}$ and $V_{th\_tunnel}$ vs. the In mole fraction $x$ in $In_xGa_{1-x}As$ (a) 100 nm and (b) 200 nm PIN diodes at room temperature. Inset: MC values of the I–V curves when considering exclusively II processes or band-to-band tunneling in the simulations of an $In_{0.53}Ga_{0.47}As$ 200 nm PIN diode at room temperature.

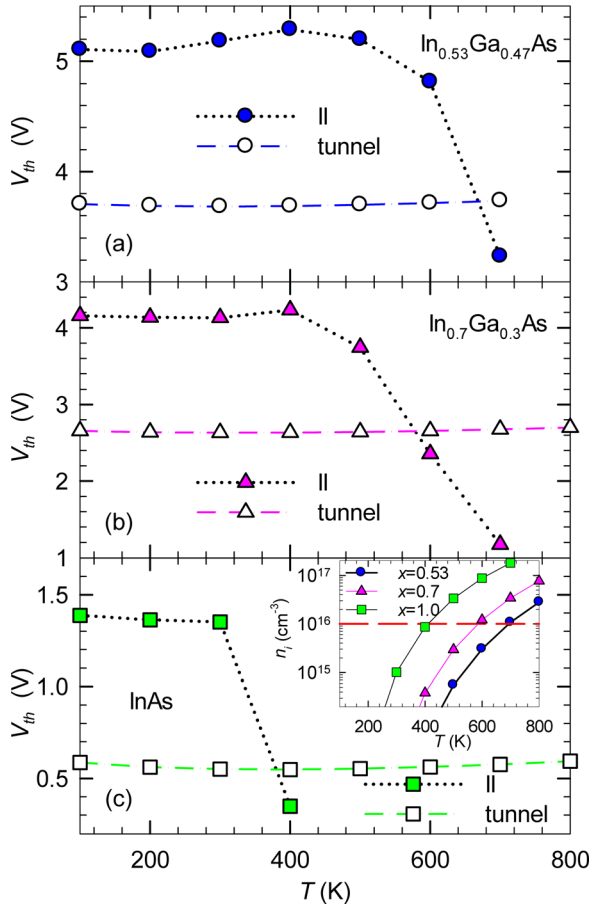


FIG. 3. MC values of $V_{th\_II}$ and $V_{th\_tunnel}$ as a function of $T$ for (a) $In_{0.53}Ga_{0.47}As$, (b) $In_{0.7}Ga_{0.3}As$, and (c) InAs 100 nm PIN diodes. Inset of Fig. 3(c): $n_i$ as a function of $T$ for the three materials.

$In_{0.53}Ga_{0.47}As$, (b) $In_{0.7}Ga_{0.3}As$, and (c) InAs. Notice that a different scale is used in each case according to the decreasing values of both $V_{th}$ when reducing the bandgap. The values of the intrinsic carrier density for the three materials are shown in the inset of Fig. 3(c). As expected and as already shown in Refs. 33 and 36, $V_{th\_tunnel}$ barely depends on $T$ due to the small variations of the different factors that affect the tunneled charge, Eq. (2). Only $T_C$ changes with $T$ (due to the modification of the built-in potential), while $f_{source}$-$f_{drain}$ is practically 1 in the whole active region and the densities of states are invariant with $T$. On the contrary, due to the increase of carrier concentration in the intrinsic region {$n_i$ increases nearly exponentially with $1/T$ [inset of Fig. 3(c)]}, $V_{th\_II}$ strongly decreases above a given temperature ($T > 600$ K, 500 K, and 300 K for $x = 0.53$, 0.7, and 1.0, respectively). This happens because, even if the probability of II processes slightly decreases at higher $T$ due to the lower carrier energy (part of it is lost because of more intense scattering in the transit along the intrinsic region), the number of carriers prone to suffer II strongly increases. Interestingly, in the three cases, $V_{th\_II} \sim V_{th\_tunnel}$ when $n_i$ reaches values around $10^{16}$ cm$^{-3}$. Figure 3 also shows that $V_{th\_II}$ has a maximum at intermediate $T$, softly decreasing when reducing $T$ since even if $n_i$ is lower, the carrier transport approaches a quasiballistic regime. In such a regime, scattering is almost completely suppressed, so that carriers accumulate enough kinetic energy to undergo II at lower voltages. Indeed, the electron temperature is much higher than that of the lattice, mainly in the low $T$ range. The presence of the maximum is more evident in the case of $x = 0.53$ for $T \sim 400$ K, less pronounced in the case of $x = 0.7$, and absent for $x = 1.0$ since transport is essentially ballistic even at high temperatures. The observed increase of $V_{th\_II}$ at low $T$ extends up to higher temperatures for semiconductors with wider bandgap (and lower $n_i$), which would make difficult the experimental observation of the $V_{th\_II}$ drop at high $T$ in the case of widely used semiconductors like Si or SiGe.

## IV. CONCLUSIONS

A MC model, which incorporates impact ionization processes by means of the Keldysh approach and band-to-band tunneling by means of the WKB method, has been employed for the study of narrow bandgap $In_xGa_{1-x}As$ structures in order to support the development of III-V I-MOSFETs and TFETs.

In $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ 100 nm PIN ungated devices, the ON-state in reverse bias conditions is originated by tunneling. At high voltages, when the tunneled carriers suffer from impact ionization, the current is enhanced and finally a drastic breakdown occurs. For longer diodes (200 nm), II could originate the ON-state but at voltages too high for low-power applications. Thus, devices based on $In_{0.53}Ga_{0.47}As$ and $In_{0.7}Ga_{0.3}As$ are found to be more

appropriate for TFET structures than for I-MOSFETs. However, the SS could be significantly enhanced by the presence of II events in addition to tunneling. For devices based on InAs, the onset of the conduction current for both 100 and 200 nm PIN diodes could be originated for applied voltages under 1 V by the joint action of II processes and tunneling. Thus, InAs structures are remarkably interesting for designing low-power low-SS I-MOSFETs and TFETs.

## ACKNOWLEDGMENTS

This work has been supported by the Ministerio de Economía y Competitividad-Dirección General de Investigación through the Project TEC2013-41640-R, the Agence Nationale de la Recherche through the Project ANR-13-JS03-000, and the Junta de Castilla y León through the Project SA022U16.

[1]K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, in *IEEE IEDM Technical Digest* (IEEE, San Francisco, CA, 2002), pp. 289–292.
[2]W. Choi, J. Y. Song, B. Y. Choi, J. D. Lee, Y. J. Park, and B. G. Park, in *IEEE IEDM Technical Digest* (IEEE, San Francisco, CA, 2004), Vol. 4, pp. 203–206.
[3]F. Mayer, C. Le Roger, G. Le Carval, L. Clavelier, and S. Deleonibus, in *ESSDERC* (2006), pp. 303–306.
[4]Q. Huang, R. Huang, Z. Wang, Z. Zhan, and Y. Wang, Appl. Phys. Lett. **99**, 083507 (2011).
[5]K. Gopalakrishnan, R. Woo, C. Jungemann, P. B. Griffin, and J. D. Plummer, IEEE Trans. Electron Devices **52**, 77–84 (2005).
[6]U. Singisetti, M. A. Wistey, G. J. Burek, A. K. Baraskar, B. J. Thibeault, A. C. Thibeault, M. J. W. Rodwell, B. Shin, E. J. Kim, P. C. McIntyre, B. Yu, Y. Yuan, D. Wang, Y. Taur, P. Asbeck, and Y.-J. Lee, IEEE Electron Devices Lett. **30**, 1128–1130 (2009).
[7]J. J. Gu, Y. Q. Wu, and P. D. Ye, J. Appl. Phys. **109**, 053709 (2011).
[8]Y. Lechaux, A. B. Fadjie-Djomkam, S. Bollaert, and N. Wichmann, Appl. Phys. Lett. **109**, 131602 (2016).
[9]W. Y. Choi, J. Y. Song, J. D. Lee, Y. J. Park, and B.-G. Park, in *IEEE IEDM Technical Digest* (IEEE, Washington, DC, 2005), p. 955.
[10]A. M. Ionescu and H. Riel, Nature **479**, 329–337 (2011).
[11]R. Pandey, S. Mookerjea, and S. Datta, IEEE Trans. Circuits - I **63**, 2128–2138 (2016).
[12]J. Mateos, T. González, D. Pardo, V. Hoël, and A. Cappy, IEEE Trans. Electron Devices **47**(10), 250–253 (2000).
[13]H. Rodilla, T. González, D. Pardo, and J. Mateos, J. Appl. Phys. **105**, 113705 (2009).
[14]T. Brudevoll, T. A. Fjeldly, J. Baek, and M. S. Shur, J. Appl. Phys. **67**, 7373–7382 (1990).
[15]M. Costato and L. Reggiani, Phys. Status Solidi B **58**, 471–482 (1973).
[16]B. G. Vasallo, J. Mateos, D. Pardo, and T. González, J. Appl. Phys. **94**, 4096–4101 (2003).
[17]B. G. Vasallo, H. Rodilla, T. González, G. Moschetti, J. Grahn, and J. Mateos, J. Appl. Phys. **108**, 094505 (2010).
[18]H. Kim, H. S. Min, T. W. Tang, and Y. J. Park, Solid-State Electron. **34**, 1251–1253 (1991).
[19]M. V. Fischetti and S. E. Laux, Phys. Rev. B **38**, 9721–9745 (1988).
[20]M. V. Fischetti, IEEE Trans. Electron Devices **38**, 634–649 (1991).
[21]T. P. Pearsall, Appl. Phys. Lett. **36**, 218–220 (1980).
[22]F. Osaka, T. Mikawa, and T. Kaneda, IEEE J. Quantum Electron. **21**, 1326–1338 (1985).
[23]T. Kagawa, Y. Kawamura, H. Asai, M. Naganuma, and O. Mikami, Appl. Phys. Lett. **55**, 993–995 (1989).
[24]N. Sano, T. Aoki, and A. Yoshii, Appl. Phys. Lett. **55**, 1418–1420 (1989).
[25]J. Bude and K. Hess, J. Appl. Phys. **72**, 3554–3561 (1992).
[26]M. V. Fischetti, N. Sano, S. E. Laux, and K. Natori, J. Technol. Comput. Aided Des. TCAD, 1–50 (1996).
[27]S. M. Sze and K. Ng Kwok, *Physics of Semiconductor Devices* (Wiley Intersciences, New Jersey, 2007).
[28]M. Luisier and G. Klimeck, J. Appl. Phys. **107**, 084507 (2010).
[29]D. Moro-Melgar, J. Mateos, T. González, and B. G. Vasallo, J. Appl. Phys. **116**, 234502 (2014).
[30]V. Talbo, J. Mateos, T. González, Y. Lechaux, N. Wichmann, S. Bollaert, and B. G. Vasallo, J. Phys.: Conf. Ser. **647**, 012056 (2015).
[31]B. G. Vasallo, V. Talbo, T. González, Y. Lechaux, N. Wichmann, S. Bollaert, and J. Mateos, in 2017 Spanish Conference on Electron Devices (2017).
[32]A. C. Seabaugh and Q. Zhan, Proc. IEEE **98**, 2095–2110 (2010).
[33]N. Ma and D. Jena, Appl. Phys. Lett. **102**, 132102 (2013).
[34]A. Pan and C. O. Chui, J. Appl. Phys. **116**, 054509 (2014).
[35]A. Relevant, P. Palestri, P. Osgnach, and L. Selmi, Solid-State Electron. **88**, 54–60 (2013).
[36]S. Morkerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, IEEE Electron Device Lett. **31**, 564–566 (2010).